Nonvolatile Ferroelectric P(VDF-TrFE) Memory Transistors Based on Inkjet-Printed Organic Semiconductor

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Nonvolatile ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) memory based on an organic thin-film transistor with inkjet-printed dodecyl-substituted thienylenevinylene-thiophene copolymer (PC12TV12T) as the active layer is developed. The memory window is 4.5 V with a gate voltage sweep of –12.5 V to 12.5 V. The field effect mobility, on/off ratio, and gate leakage current are 0.1 cm^2/Vs, 10^5, and 10^{-10} A, respectively. Although the retention behaviors should be improved and optimized, the obtained characteristics are very promising for future flexible electronics.

Keywords: Inkjet-printing, nonvolatile memory, ferroelectric, P(VDF-TrFE).

I. Introduction

Single-transistor-type memory devices comprising transistors with a ferroelectric gate insulator have been extensively investigated for application in conventional silicon electronics. Indeed, various oxide ferroelectric materials have been tested for their performance as a ferroelectric gate insulator [1]-[3]. However, to realize flexible nonvolatile memory, the use of an oxide ferroelectric gate insulator is unsuitable, owing to the high crystallization temperature.

The overall process temperature should be below 200°C [4]. Polymeric ferroelectric thin films can offer an attractive solution to this problem because their crystallization temperatures are much lower than those of oxide ferroelectrics. Poly(vinylidene fluoride-co-trifluoroethylene) (P[VDF-TrFE]) is the most typical ferroelectric copolymer material [5]. P(VDF-TrFE) thin films can be easily formed by a solution-based spin-coating method, and crystallization can be performed at a low temperature of around 140°C, which is one of the significant merits in realizing a memory device on plastic substrates. To this end, many studies on the fabrication and characterization of nonvolatile memory transistors using P(VDF-TrFE) have been conducted, mainly for realizing all-organic memory transistors with organic semiconducting channel layers [6], [7]. In this study, we develop a low-voltage-operating top-gated ferroelectric polymer transistor memory that can be fabricated using an inkjet-printing method [8]. Our solution-processed ferroelectric memory devices show high charge carrier mobility, high on/off ratio, and a large memory window under relatively low operating voltages.

II. Experiment

Source/drain (S/D) electrodes are fabricated from Au/Ni (15-nm-thick/3-nm-thick) patterns using a conventional

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photolithography procedure. The substrates are cleaned with deionized water, acetone, and isopropanol in an ultrasonic bath for 10 min each. A p-type polymer semiconductor containing dodecyl-substituted thienylenevinylene (TV) and dodecylthiophene (PC12TV12T) is synthesized using a previously published procedure [9] and dissolved in anhydrous p-xylene to obtain approximately 3 mg/ml of solution. A custom-built research inkjet printer (UJ200MF, Unijet) is used to inkjet-print the semiconductor solution. The semiconductor film is thermally annealed at 200°C for 30 min in a N_2-purged glove box. Random copolymer P(VDF-TrFE) (70:30 mol%) is purchased from Solvay SA and dissolved in dimethylsulfoxide to obtain a solution concentration of 50 mg/ml to 70 mg/ml. P(VDF-TrFE) is spin-coated at 2,000 rpm onto PC12TV12T inkjet-patterned substrates. It is then thermally annealed on a hotplate at 70°C for 5 min to remove the residual solvent and subsequently at 140°C for 60 min to enhance the crystallinity of the ferroelectric β-phase of P(VDF-TrFE). The transistors are completed by depositing Al top-gate electrodes (approximately 50 nm) by thermal evaporation using a metal shadow mask.

The capacitance-voltage (*C-V*) characteristics are measured using an impedance analyzer (HP4194A) at a frequency of 1 MHz. The transfer and output characteristics of the thin-film transistors (TFTs) are measured using a semiconductor parameter analyzer (B1500A, Agilent Technologies). Such transistor parameters as charge carrier mobility are calculated in the saturation regime using the standard formalism for field-effect transistors (FETs) [10]. The ferroelectric properties of the films are analyzed in terms of hysteresis by determining the remnant polarization and coercive field with a computer-controlled material analyzer (Precision LC, Radiant Technologies). Each transistor has a channel length of 20 µm and a channel width of 1 mm. The completed organic FET device structure and the molecular structures of the polymer semiconductors and gate dielectric are shown in Fig. 1.

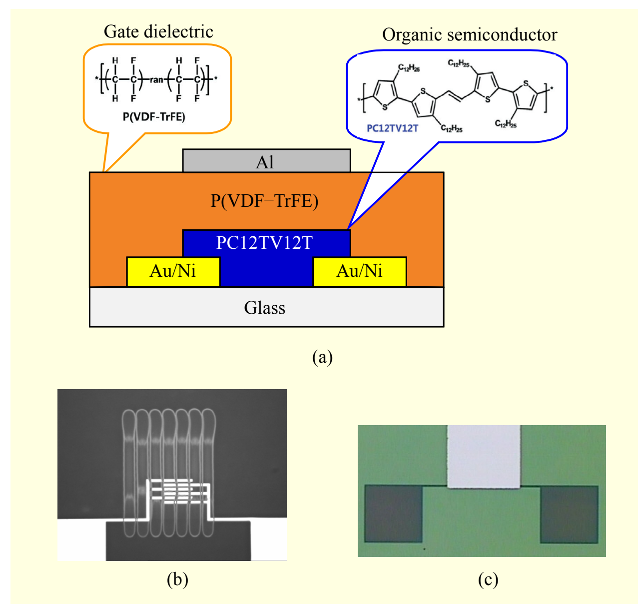

Fig. 1. (a) Top-gate/bottom contact polymer TFT device and molecular structures. (b) CCD camera image of inkjet-printed active feature. (c) Optical microscopy image of TFT.

III. Results and Discussion

To fabricate high-performance top-gated organic TFTs (OTFTs), the selection of a benign gate insulator solvent is important to avoid performance degradation via dissolution or the swelling of a semiconducting layer. In top-gated OTFTs, orthogonal solvent means that solvents dissolve an organic gate insulating layer but do not dissolve an underlaid organic semiconducting layer; thus, it enables the deposition of several organic layers through a solution process without damage to the underlaid layer [8]. In this study, we use the p-xylene and dimethylsulfoxide orthogonal solvents for the semiconductor and insulator layer. In Fig. 1(b), roughness in the inkjet-printed edge region is several tens of nm, and surface roughness in the center region is very smooth with several nm.

The capacitor properties of the P(VDF-TrFE) films are characterized by *C-V* measurement for the Al/P(VDF-TrFE)/Pt structures after thermal annealing at 140°C; the results are plotted in Fig. 2 as a function of the electric field (*E*). The capacitance shows a hysteresis behavior (butterfly shaped) due to the polarization reversal in the film; this result clearly indicates that the P(VDF-TrFE) film exhibits ferroelectric properties. The dielectric constant and voltage window (memory window) of the film are approximately 10.5 and

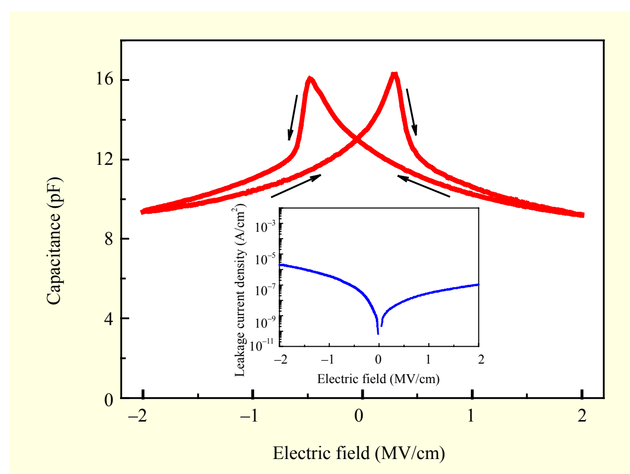

Fig. 2. *C-V* characteristic of metal-ferroelectric-metal (MFM) capacitor with P(VDF-TrFE) film. Inset shows gate leakage-current density and electric field of P(VDF-TrFE) film.

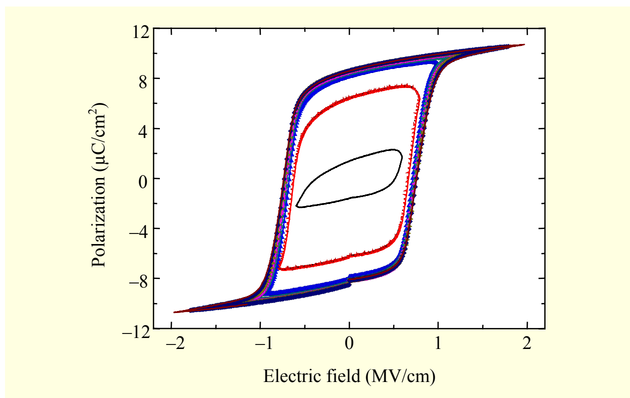

Fig. 3. *P-E* hysteresis loops according to applied voltage of MFM capacitors with Al/P(VDF-TrFE)/Pt structures.

4.5 V, respectively, similar to the results in [5], [6].

The leakage-current density (J_{leak}) of the film at room temperature is relatively low, on the order of 10^{-6} A/cm^2, and no breakdown in the dielectric film occurs within the measurement range (±2 MV/cm) (see inset in Fig. 2). As shown in Fig. 3, the ferroelectric polarization behavior of the P(VDF-TrFE) thin film is also verified using a typical polarization versus the applied electric field (*P-E*) hysteresis loop, with a thickness of approximately 300 nm. The maximum zero-bias polarization (remnant polarization) is measured as being approximately 10 μC/cm^2. The coercive field (E_c) of the P(VDF-TrFE) ferroelectric film is 750 kV/cm, where its hysteresis loop in the *P-E* plot passes zero *P*; this is the minimum field required to reverse the full ferroelectric polarization.

The PC12TV12T TFTs with the P(VDF-TrFE) dielectric exhibited typical p-type transistor properties, a relatively high charge carrier mobility of more than 0.1 cm^2/Vs, and a high on/off current ratio of about 10^5. Figure 4(a) shows the variation in the memory window for various gate voltage (V_G) sweep ranges. The width of the memory window gradually increases from 0 V to 8.5 V when the V_G sweep range increases from ±5 V to ±20 V. The memory window is confirmed to be as wide as about 4.5 V even when the V_G sweep is ±12.5 V. This suggests that our ferroelectric memory TFTs can be operated at a relatively low voltage. The operating voltage of an OTFT depends on the dielectric constant and the thickness of the gate dielectric. A gate dielectric with high permittivity reduces the operating voltage of OTFTs effectively without the need for thickness reduction. This is advantageous because a reduction in thickness can degrade the device reliability and the yield either through electrical shorting via the gate dielectric or via large gate leakage [5], [6].

Moreover, the width of the memory window increases in an almost symmetrical manner toward both positive and negative directions. Fig. 4(b) shows the transfer curves after application of different V_G sweep ranges, where only the negative side increases while the positive side is fixed at 20 V. In these series of measurements, the memory windows are slightly increased toward only the positive direction, while the onset voltage (V_{on}) remains the same. This results from the fact that the off

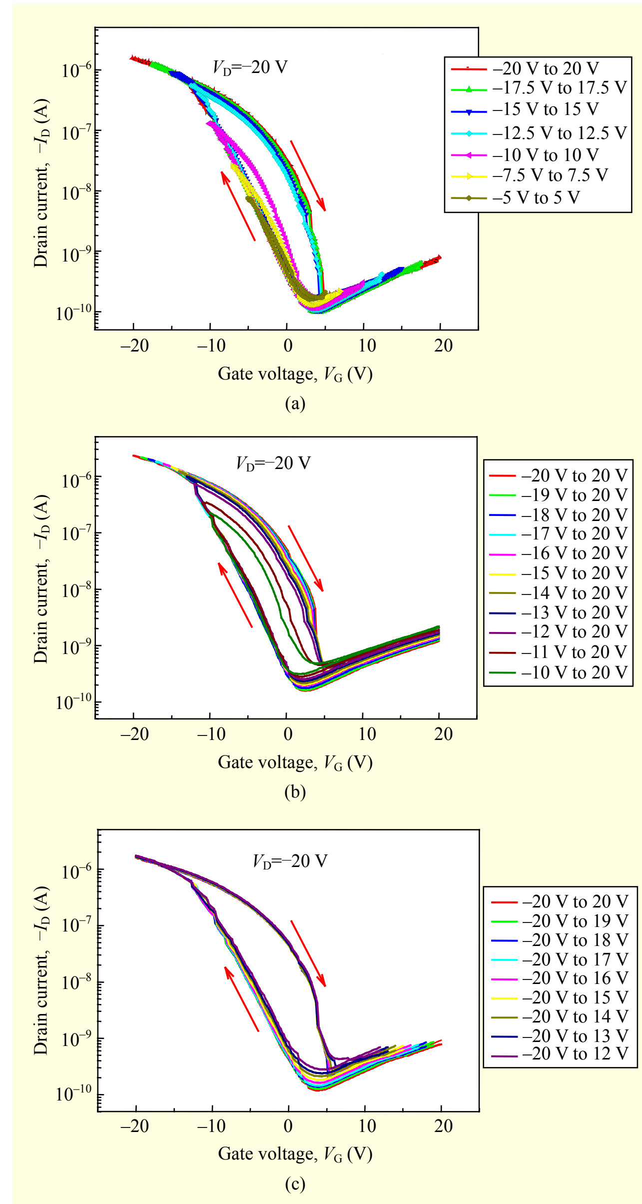

Fig. 4. I_D-V_G transfer curves for fabricated OTFT with ferroelectric P(VDF-TrFE) gate dielectric. (a) Sets of transfer curves when V_G sweep ranges are symmetrically increased from –5 V to 5 V to –20 V to 20 V. (b) Transfer curve variations when only negative side of V_G sweep range is decreased from –20 V to –10 V while maintaining positive side at 20 V. (c) Transfer curve variations when only positive side of V_G sweep range is increased from 12 V to 20 V while maintaining negative side at –20 V.

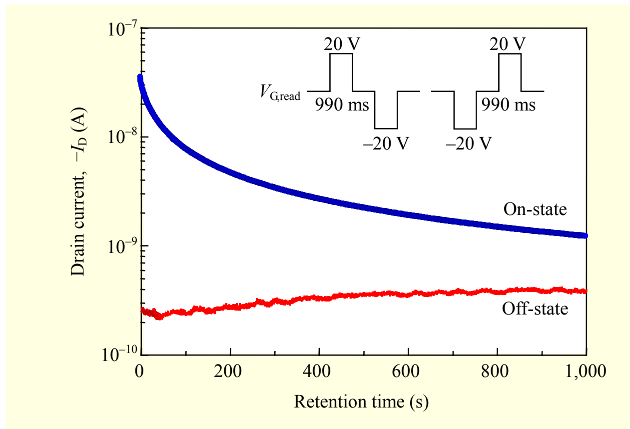

Fig. 5. Variations in I_D programmed into both on-state and off-state with lapse of memory retention time. Inset shows programming pulse sequences for evaluation of memory retention behaviors of ferroelectric memory TFT.

operations are ensured in each measurement by a sufficient positive voltage to program the off state. Figure 4(c) shows the transfer curves after application of different V_G sweep ranges, where only the positive side increases while the negative side is fixed at –20 V. In these series of measurements, the memory windows are slightly increased toward only the negative direction, whereas the V_{on} remains the same [4].

Consequently, we can control and design the operation voltage and corresponding memory behaviors by using the operation schemes shown in Figs. 4(b) and 4(c). The memory retention characteristics are also investigated. The drain current (I_D) both in the on-state and off-state after application of programming and erasing biases (pulse sequences) is shown in Fig. 5.

To program the on-state, a 20-V-high and 990-ms-wide pulse is applied to the gate terminal to initialize ferroelectric polarization in the P(VDF-TrFE) layer, followed by a –20-V-high and 990-ms-wide programming pulse. I_D is measured at a drain voltage (V_D) of 20 V and V_G of 0 V for a given programmed on-state. The off-state is also provided, followed by an opposite sequence (initially, a 20-V-high and 990-ms-wide pulse; then, a –20-V-high and 990-ms-wide pulse) for application of the erasing pulse. The initial on/off-state current ratio is found to be higher than 10^2, and a ratio of more than 10 remains after the lapsed time of 10^3 seconds. The retention time value is considerably smaller than previously reported [4], [7]. Although the reason for this difference in value is not clear at present, in general, the retention characteristics of programmed currents for this type of memory transistor are very sensitive to the read-out conditions of V_G. Although the obtained retention time should be extended, considering the relatively low programming voltage of 12.5 V, we can expect a great potential for the future development of our memory transistor [4].

IV. Conclusion

We fabricated ferroelectric memory TFTs using an inkjet-printed PC12TV12T as the semiconducting layer and P(VDF-TrFE) copolymer as the gate insulator. The transistor devices showed high hole mobility of more than 0.1 cm^2/Vs and the expected clockwise hysteresis of I_D during dual sweeping of V_G. A memory transistor exhibited promising characteristics, such as a memory window of 4.5 V at $V_G = \pm 12.5$ V, an on/off ratio of 10^5, and I_{leak} of $<10^{-10}$ A. Although the retention time should be improved, we expect that the proposed memory TFTs will be one of the most suitable candidates for nonvolatile memory devices that can potentially be used in a variety of future flexible electronics.

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