A Novel Process for Fabricating High Density Trench MOSFETs for DC-DC Converters

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We propose a new process technique for fabricating very high-density trench MOSFETs using 3 mask layers with oxide spacers and a self-aligned technique. This technique reduces the device size in trench width, source, and p-body region with a resulting increase in cell density and current driving capability as well as cost-effective production capability. We were able to obtain a higher breakdown voltage with uniform oxide grown along the trench surface. The channel density of the trench DMOSFET with a cell pitch of 2.3–2.4 μm was 100 Mcell/in^2 and a specific on-resistance of 0.41 mΩ·cm^2 was obtained under a blocking voltage of 43 V.

Manuscript received Jan. 11, 2002; revised May 8, 2002.

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I. INTRODUCTION

Power MOSFETs are an important class of discrete devices used in a variety of power conversion applications for a voltage range of below 200 V, because they have low conduction power loss, high input impedance, and high switching speed [1]-[4]. The increasing popularity of power MOSFETs has led to greater efforts to try to reduce their specific on-resistance, to minimize die sizes, and to reduce cost, especially for low voltages of less than 50 V. This has been largely driven by the increasing demand for portable electronics, such as personal computers and cellular telephones, with high performance, small size, and extended battery life [5].

To optimize the power handling capability for a specified breakdown voltage rating and on-state resistance, it is essential to increase the cell packing density of a power semiconductor device. This has resulted in devices that have very high cell and current densities. The Double diffused MOS (DMOS) transistor has reached a level of development where further increases in the cell densities do not improve the performance significantly. However, the DMOS transistor with a trench gate structure does not suffer from the same limitations as those of the DMOS, and its potential suggests that it will become the dominant technology.

Non-planar power MOSFETs with trench gate structures are known to provide high cell packing densities. In addition to an increased cell packing density, the MOS gates formed along the etched silicon regions result in a reduced on-state resistance per unit cell because they lack the JFET pinching resistance normally present in a silicon DMOSFET structure [1]. Numerous advances in the cell density and fabrication process of trench technology have been reported [6]-[11]. Recent

advances in the anisotropic etching of silicon using a reactive ion plasma provide a means for the controlled formation of silicon etch regions with cell packing densities suitable for VLSI. Despite the high cell density and low on-resistance, the reported device structure made by the conventional fabrication methods have some limitations on further reducing the cell size because of process complexity.

This paper reports on the results we obtained from an extensive theoretical and experimental investigation of low on-resistance power MOSFETs fabricated by our novel scaled fabrication method. To achieve our results, we used a simplified process technique, oxide spacers, and self-aligned techniques [12] in developing the high performance trench gate power MOSFETs.

II. DEVICE DESIGN AND FABRICATION

Figure 1 shows the cross section views of the proposed trench gate DMOSFET structure. In order to minimize the channel resistance, we sought to achieve a very high channel density by using a cellular design topology with a micron trench width and a cell pitch of 2.4 μm. The the proposed trench is less than half the size of a conventional trench, which has a cell pitch of 6.0 to 7.0 μm, because the new fabrication process shrinks the device size by a factor of 3.

The process sequence for fabricating trench DMOSFETs using 3 mask layers (trench, poly, and metal mask) is illustrated in Fig. 2. A phosphorus-doped silicon layer was epitaxially grown on top of 0.004 Ω·cm As-doped <100> silicon substrates. The starting epitaxial region doping density was 2×10^{16} cm^{-3} and its thickness was 5.0 μm for 45 V devices. Following the thermal oxide growth and nitride layer deposition, trench regions were defined using dry etching of the nitride and oxide layers (Fig. 2(a)). An approximately 1.5 μm deep p-base region was formed by boron implantation and driven in to obtain an electrically active boron peak concentration of 7×10^{16} cm^{-3}. TEOS oxide was deposited and etched by RIE to form oxide spacers. Silicon trenches about 1.8 μm deep were defined by plasma etching the opened p-well area (Fig. 2(b)). Following the removal of the oxide spacers, the sacrificial oxide was grown and arsenic ion implantation (about 5.0E15/cm^2) was performed without any

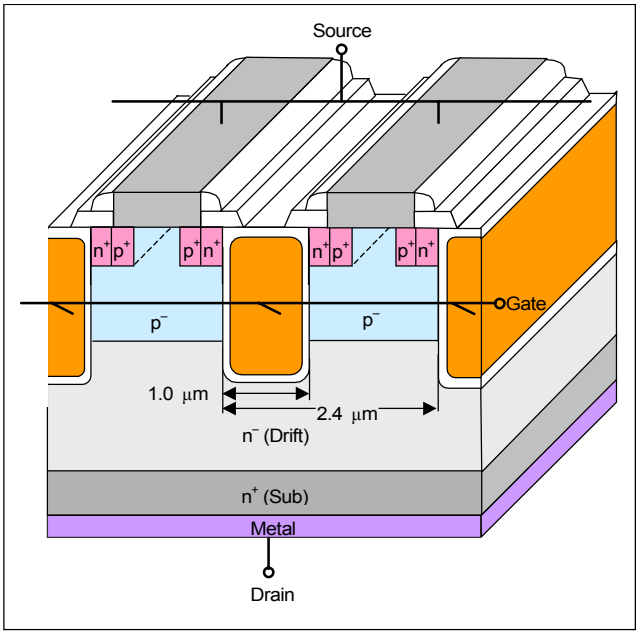

Fig. 1. The cell layout of the proposed trench gate DMOSFET.

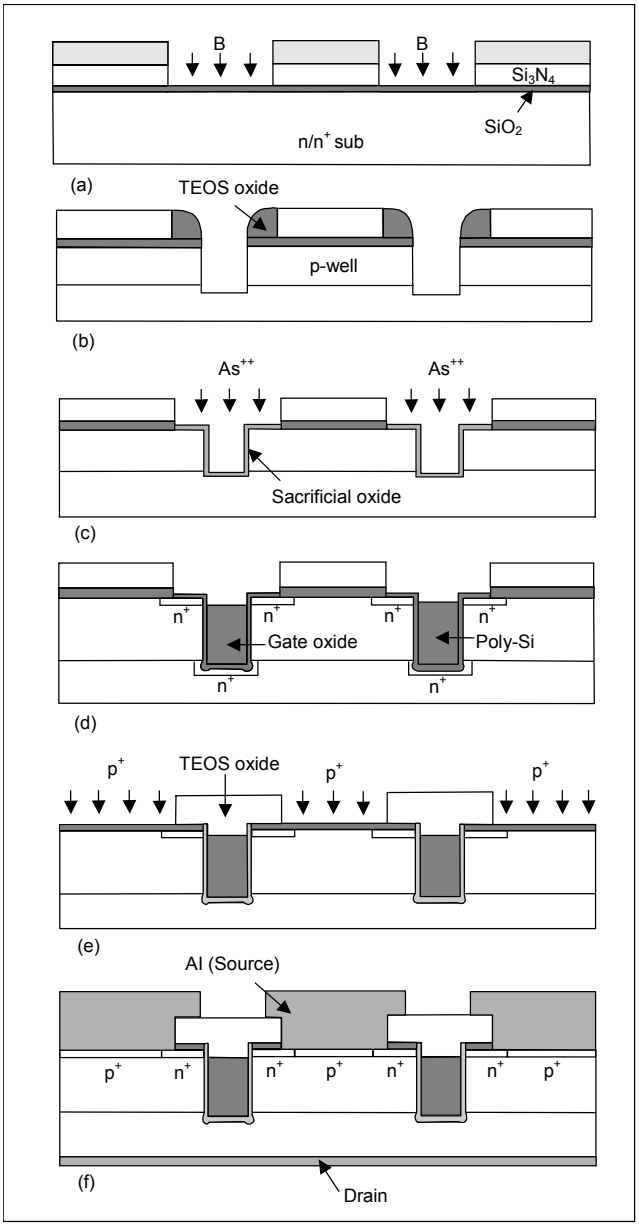

Fig. 2. The process sequence of the proposed technique using oxide spacers, self-aligned methods, and hydrogen annealing.

angle to form sources of the devices. Following a sacrificial oxide etching process to remove impurities distributed at the surface of the trench sidewall and improve the trench surface, gate oxide was grown on the sidewall of the trench (Fig. 2(c)). Immediately following gate oxide formation, LPCVD polysilicon was deposited and $POCl_3$-doped to fill the trench. Etch-back planarization of the doped polysilicon was performed (Fig. 2(d)). O_3-TEOS oxide was deposited and etched back to expose the nitride layer and implant boron ions (about 3.0E15/cm^2) for the p^+ body ohmic contact and source contact that was self-aligned to the trench (Fig. 2(e)). Finally, aluminum was deposited on the front and backside of the substrate and etched to define the sources and drains (Fig. 2(f)).

It is extremely difficult to make sources by oblique ion implantation for deep, narrow trenches with a high aspect ratio. Our technique provides a method of fabricating trench MOSFETs with a narrow trench width by using oxide spacers and a shrinking chip size by self-aligned sources and body ohmic contacts; this results in high-density trench MOSFETs and reduces channel resistance. In addition, the above process flow provides a thicker oxide at the edges and bottom of the trench because these regions have higher doping concentration by As implantation (Fig. 2(c)). The thicker oxide at the edges and bottom of the trench implies that the device has higher breakdown voltage and reliability.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 3 illustrates the formation of a pair of oxide spacers by anisotropical etching of the TEOS oxide layers. The bottom width of each oxide spacer is primarily equal to the thickness (0.4 μm) of the deposited TEOS oxide. Therefore, the thickness of the deposited silicon nitride and TEOS oxide layer is determined by the desired source region and trench width. In Fig. 4, trenches are formed by etching the opened silicon with RIE dry-etching. The oxide spacers are then removed and the

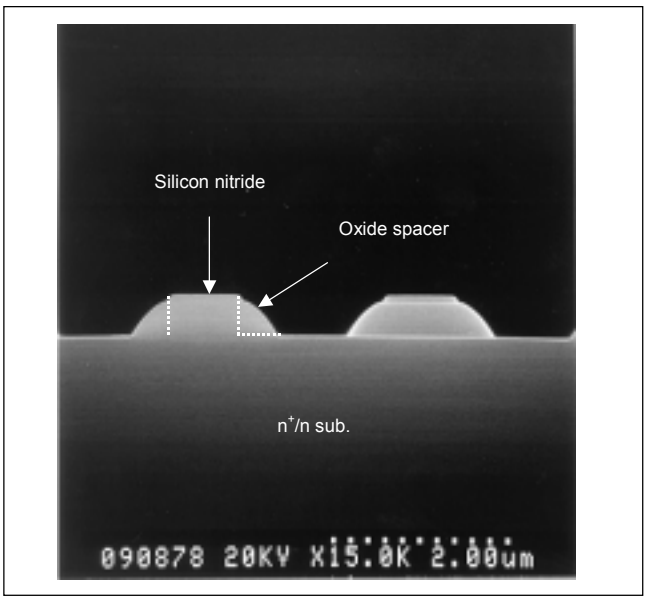

Fig. 3. SEM photograph of the oxide spacer formation.

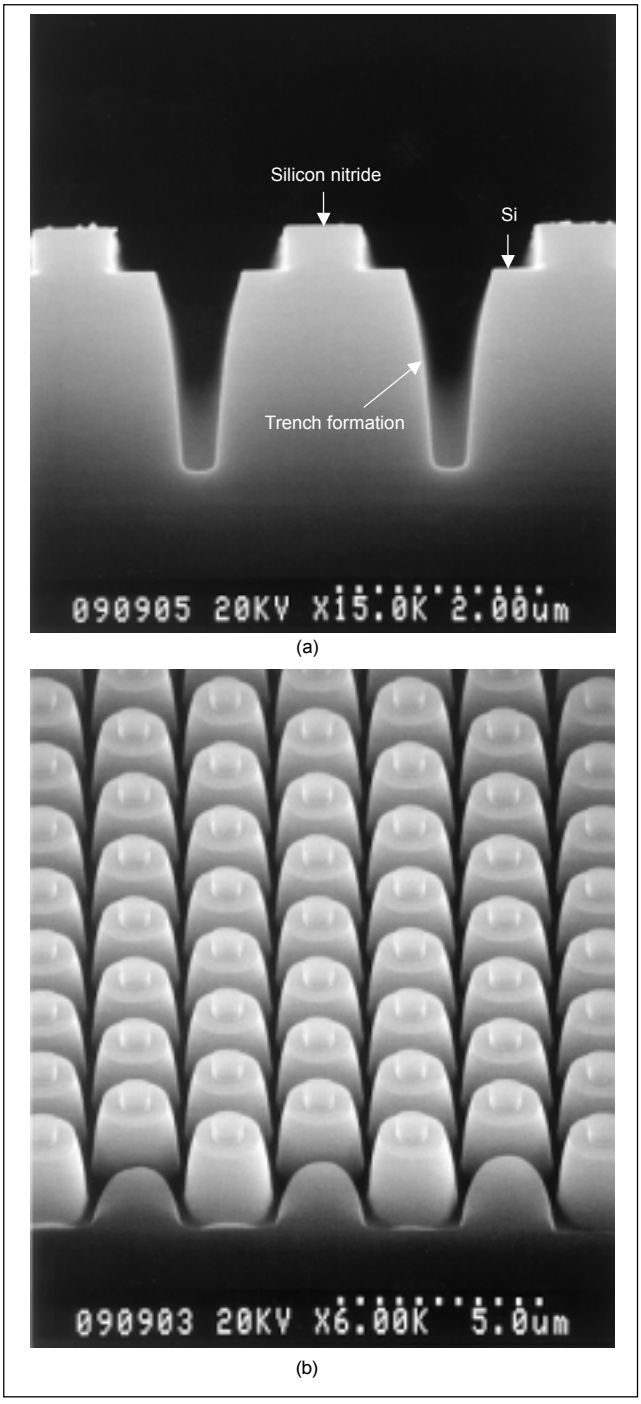

Fig. 4. SEM photograph of structures with nitride layers and etched trenches after oxide spacers for self-aligned ion implantation of sources (a) cross section, (b) top view.

source regions are formed at the bottom of the spacer by blanket implanting As and performing a drive-in diffusion.

The performance of a vertical channel device is highly dependent on the quality of the trench sidewall. It is critical to develop techniques capable of rendering the surface as smooth as possible. This is controlled by the etching and oxidation conditions. A smooth bottom corner in the trench is also desirable for minimizing the added electric field stress in the oxide. We obtained a very smooth trench surface with a surface roughness of 17 Å (an RMS value of 3.1 Å) by using the etching condition of the HBr/CF_4 with 45% in $He\text{-}O_2$ chemistries [6]. This surface roughness of the SiO_2/Si interface is lower than that of the CONCAVE-DMOSFET, which uses LOCOS oxidation [13].

The trench sidewall, corners, gate oxide, silicon nitride layer and poly-silicon filling are depicted in Fig. 5. We observed a unit cell with a cell pitch of 2.3 to 2.4 μm and also good trench sidewalls and smooth corners, which are desirable for minimizing the electric field stress in the gate oxide. By using an oxide spacer, a self-aligned technique, and three mask layers, we have successfully manufactured trench DMOSFETs as shown in Fig. 6. The drain is not shown in this figure because the drain was formed at the back-side of the substrate. The polysilicon layers were defined by the poly mask, such as the center region and edge region, to form a gate pad, while other polysilicon unit cells were etched back to parallel connected to decrease on-resistance of the device. The resulting channel density was 100 Mcell/in^2 and the chip was mounted in a TO-220 package.

In our development of the trench MOS structure, we performed two dimensional DIOS and DESSIS [14] simulations.

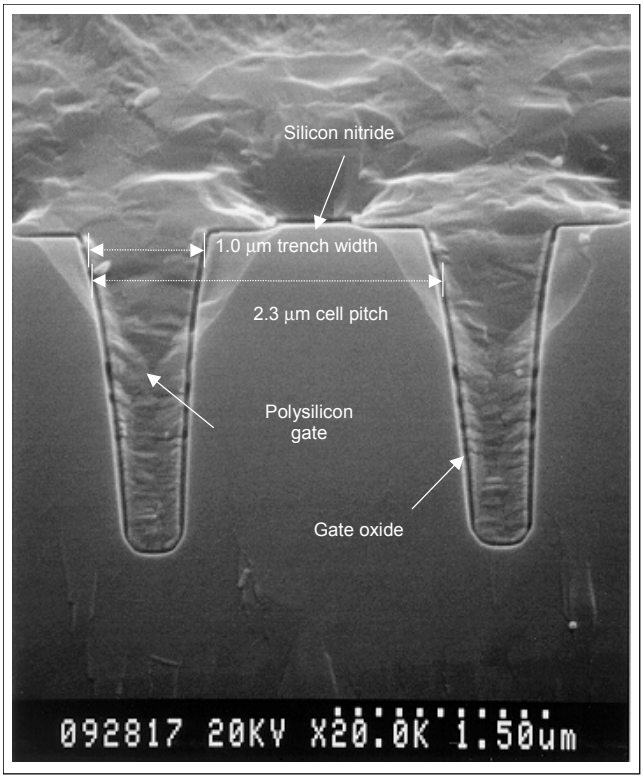

Fig. 5. Trench structure showing gate oxide cell pitch, and width prior to polysilicon etch-back.

We achieved optimized results when the impurity concentrations of the epi-region, the channel region, and the source/drain region were $1\text{-}3\times10^{16}$/ cm^3, $3\text{-}7\times10^{17}$/ cm^3, 5×10^{19} / cm^3. Figure 7 shows the potential contour of the trench MOSFET with a breakdown voltage of about 40 V. The potential was

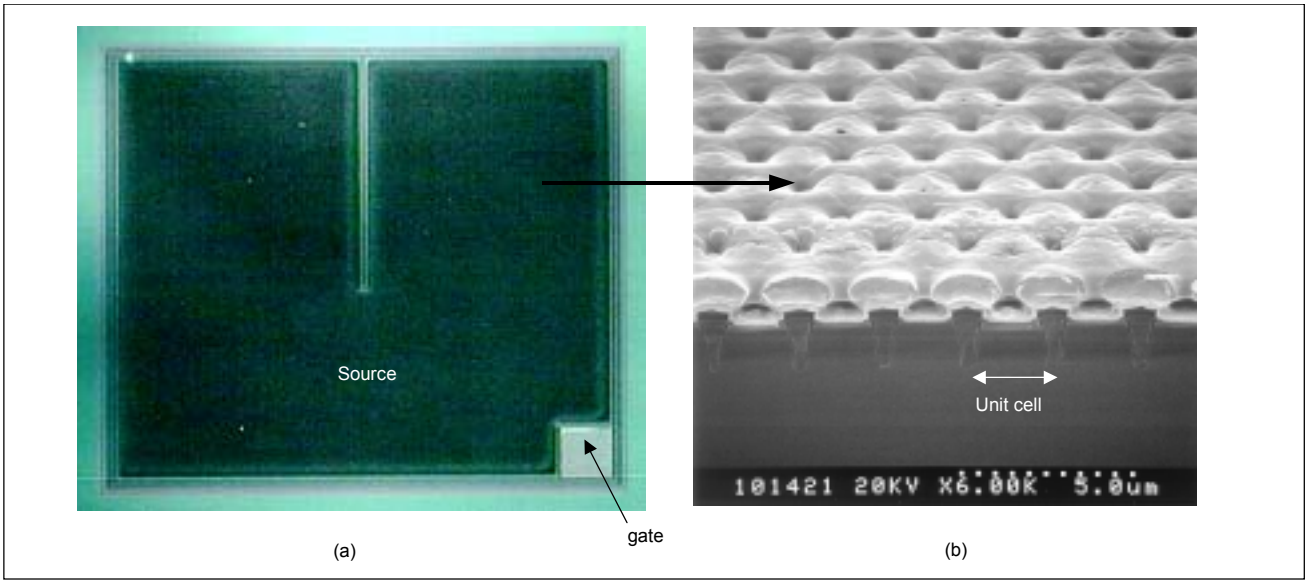

Fig. 6. The final trench DMOSFETs (a) top view and (b) cross-section with a channel density of 100 Mcell/in^2.

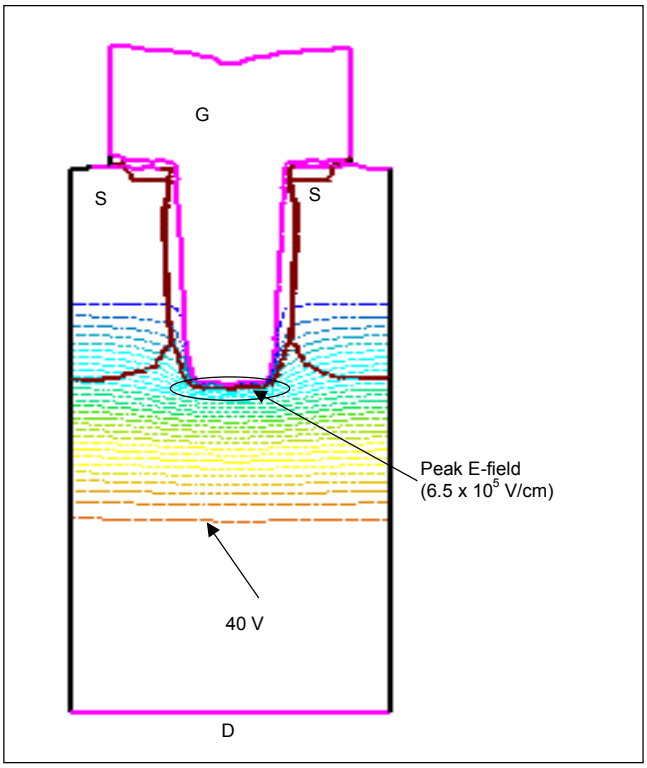

Fig. 7. Potential distribution of the trench MOSFET at the critical field of 6.5×105 V/cm.

much more densely distributed at the corner of the trench bottom, indicating a critical electric field and the value was about 6.5×10^5 V/cm. According to [15], the electric field is increased in the vicinity of the trench gate and p-body to the drain junction by thinning the thickness of gate oxide. This electric field crowding effect leads to a reduction in the breakdown voltage, which is called field plate-induced breakdown. Therefore, the breakdown voltage and maximum gate drive voltage are strongly dependent on the uniformity of the gate oxide at the bottom of the trench. The gate oxide in the trench bottom of the proposed device is thicker than that of conventional ones because we implant arsenic when the source region is formed. This is desirable for diminishing a reduction in breakdown voltage.

The measured threshold voltage was 1 V. The off-state I-V characteristics of the proposed device is illustrated in Fig. 8. The drain breakdown voltage was 43 V, which is consistent with the simulated value of 40 V. The I-V characteristics of the trench DMOSFETs fabricated by the proposed method were compared with those fabricated by the conventional method (Fig. 9) in order to inspect the gate oxide characteristics along the trench surface. The gate current was measured as the gate voltage was increased. The thickness of the gate oxide was about 50 nm. The current started to flow for the gate oxide grown by the proposed method at a gate voltage of 35 V, while

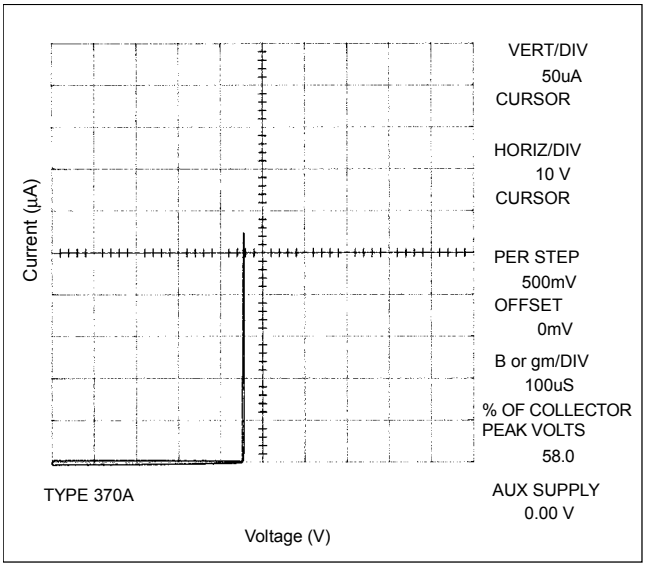

Fig. 8. Breakdown characteristics of the fabricated device.

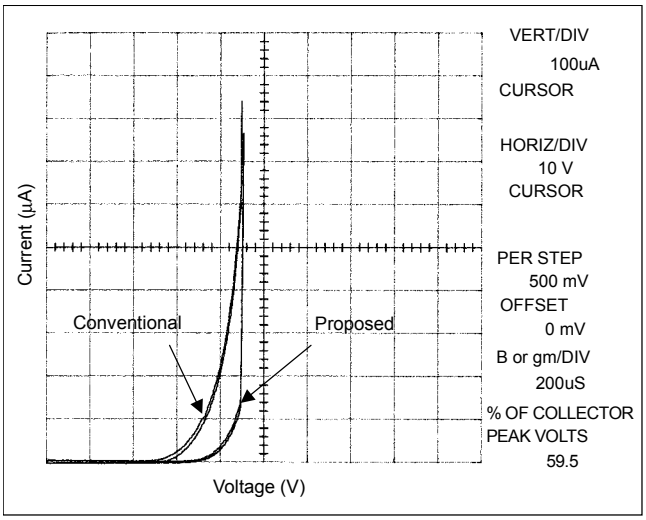

Fig. 9. I-V characteristics of the trench DMOSFETs fabricated by (a) the proposed technique and (b) the conventional technique.

the current started to flow for the gate oxide grown by the conventional method at a gate voltage of 28 V. The results plotted in Fig. 9 reveal that the I-V characteristics of the gate oxide grown by the proposed method are excellent, showing a higher breakdown voltage, because the proposed trench MOSFETs have a more uniform gate oxide along the trench surface. This implies that the proposed process flow provides a thicker oxide at the edges and bottom of the trench because these regions have a higher doping concentration by As implantation than the conventional one.

The typical measured output current-voltage characteristics of a 0.6×1.0 mm^2 chip size are shown in Fig. 10 under pulsed drain bias conditions. An on-resistance of 68 mΩ was obtained

at a gate voltage of 10 V and a 5 A source to drain current. The corresponding specific on-resistance was 0.41 mΩ·cm^2, which is about 50% lower than that of a conventional device, with a cell pitch of 7.4 μm fabricated using 6 mask layers with the same process conditions and chip area.

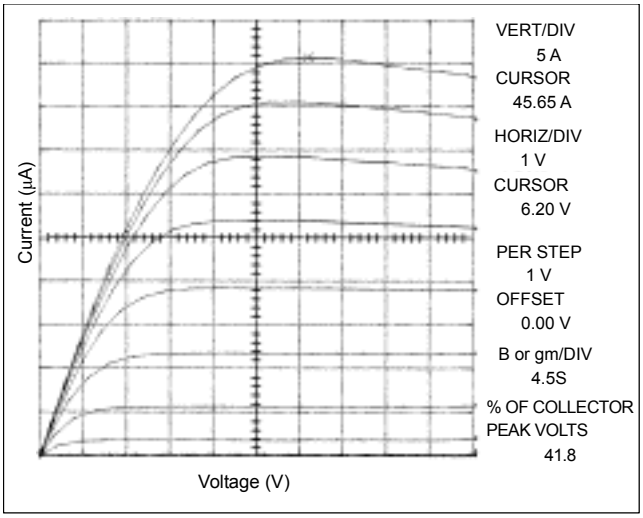

Fig. 10. The forward conduction characteristics of the hydrogen annealed trench DMOSFET subjected to the pulsed drain bias conditions.

IV. CONCLUSION

A new process technique for high-density, low on-resistance trench MOSFETs has been developed using 3 mask layers for DC-DC converter applications. An oxide spacer and self-aligned technique enabled us to realize the proposed technique, which reduces the number of steps in the process, the trench width, and the source and p-body region. These innovations resulted in an increase in cell density and current driving capability, a decrease in on-resistance, and an increase in cost-effective production capability.

We obtained a unit cell with a cell pitch of 2.3-2.4 μm and also good trench sidewalls and smooth corners. The channel density of the trench MOSFET was 100 Mcell/in^2 and the I-V characteristics of the gate oxide fabricated by the proposed method were excellent with higher breakdown voltage, because the proposed trench MOSFET has a more uniform gate oxide along the trench surface. The corresponding specific on-resistance was 0.41 mΩ·cm^2 at a gate voltage of 10 V and a 5 A source to drain current, which is about 50% lower than that of conventional devices fabricated by us with a cell pitch of 7.4 μm fabricated using 6 mask layers with the same process conditions and chip area. This low on-resistance results from a reduction in chip size by a self-aligned process and the higher cell density of the device.

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