Optimization of Selective Epitaxial Growth of Silicon in LPCVD

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Selective epitaxial growth (SEG) of silicon has attracted considerable attention for its good electrical properties and advantages in building microstructures in high-density devices. However, SEG problems, such as an unclear process window, selectivity loss, and nonuniformity have often made application difficult. In our study, we derived processing diagrams for SEG from thermodynamics on gas-phase reactions so that we could predict the SEG process zone for low pressure chemical vapor deposition. In addition, with the help of both the concept of the effective supersaturation ratio and three kinds of E-beam patterns, we evaluated and controlled selectivity loss and non-uniformity in SEG, which is affected by the loading effect. To optimize the SEG process, we propose two practical methods: One deals with cleaning the wafer, and the other involves inserting dummy active patterns into the wide insulator to prevent the silicon from nucleating.

Keywords: Selective epitaxial growth (SEG), loading effect, selectivity, LPCVD.

I. Introduction

Future electronic devices demand an aggressive scale-down of physical dimensions. One of the most critical challenges is to achieve reliable electrical properties in small-size, high-aspect ratio structures [1]. Among the newly spotlighted technologies, selective epitaxial growth (SEG) has shown promise because of the good electrical properties it exhibits in applications to very large scale integrated (VLSI) devices [2]. In spite of the advantages, however, it has processing problems; for example, it has been hard to ensure proper process conditions for good growth uniformity and selectivity during low pressure chemical vapor deposition (LPCVD), because the conditions can easily change with different pattern shapes, materials, and applied-gas systems. Therefore, before we can consider process optimization, we must first address the problem of selectivity loss in an electronic device.

Among methods for achieving stable experimental conditions for SEG, CVD thermodynamics is a potential candidate because thermodynamic variables, such as high temperature, relatively high pressure, and large input gases, act quickly on each other in a complicated way in an LPCVD system [3], [4]. Recently, CVD thermodynamics for SEG were consistent with the experimental data in LPCVD [5]. Hwang et al. proposed an interesting SEG model based on both thermodynamic analysis and electrostatic interactions with charged clusters. This model included three steps, namely, a dynamic equilibrium state by fast homogeneous reactions forming some charged clusters in the gas phase, etching on the surface by the atomic unit, and influx of silicon clusters toward the conducting materials by electrical forces [6], [7]. This suggested that sources for SEG are mainly supplied from the gas phase, not from the surface.

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In our investigation, using CVD thermodynamics for gas-phase reactions, we proposed and experimentally verified processing diagrams for SEG. They not only offered good process guidelines for SEG, but were also helpful in understanding the SEG loading effect. Loading effect means that the silicon growth rate depends on the pattern shape and the ratio of the open silicon area to the total wafer surface at a constant condition. It is closely related to growth uniformity and selectivity loss in LPCVD systems. Experimentally, we examined this effect both according to the concept of the effective supersaturation ratio (ESR) and by three E (electron)-beam patterns. However, what was more important was to discover practical methods for optimizing the SEG process in real devices by suppressing the loading effect. SEG should simultaneously grow uniformly and as fast as possible, without causing silicon nucleation on the insulator. To achieve this, we must uniformly control the supersaturation ratio of the silicon everywhere on the wafer, and in particular, we must increase the limit of the critical driving force for silicon nucleation on the insulator. We considered three methods for this purpose. One was to lower the supersaturation ratio in the experimental condition by increasing the HCl flow, another was to clean the wafer, and the third was to insert dummy active patterns into the wide insulator surface. Because of an increased thermal budget problem in the first method, we chose the other two methods for SEG applications.

II. Experimental

We used two gas systems for SEG tests in LPCVD. We chose an MS(mono-silane, SiH_4)-HCl-H_2 system for its low thermal budget process and a DCS(diclolo-silane, SiH_2Cl_2)-HCl-H_2 system for its good selectivity and stable process control. The SEG tests on the MS system were mainly processed under a low temperature condition of 800 °C and 20 Torr due to enhanced reactivity, while the tests on the DCS system were carried out under a condition of 900 °C and 100 Torr with variable gas ratios in a single wafer reactor, the CENTURA EPI system (AMAT). Thermo-Calc software (version-K) performed the thermodynamic analysis of the chemical reactions in the gas phase [5]-[7].

For this study, we especially prepared three kinds of mask patterns called the E(electron)-beam <1>, <2>, <3>. Oxide (SiO_2, LPCVD) and nitride (Si_3N_4, PECVD and LPCVD) patterns were made by reactive ion etching. For some patterns, we inserted a tungsten layer by sputtering between the nitride layer and the silicon substrate in order to examine the cleaning effect after the metal etch. We determined the SEG thickness and selectivity loss on the wafer by scanning electron microscopy (SEM).

III. Results and Discussion

1. SEG Process Diagrams

In general, SEG in LPCVD proceeds at the relatively high temperature and pressure with large amounts of source gases. If fast gas phase reactions largely govern a certain SEG system without generating any powder-like by-products from halogen elements, such as Cl, Br, and F, SEG may be one of the most promising areas that thermodynamic analysis can be applied to.

To evaluate the trend of the growth rate and selectivity, we

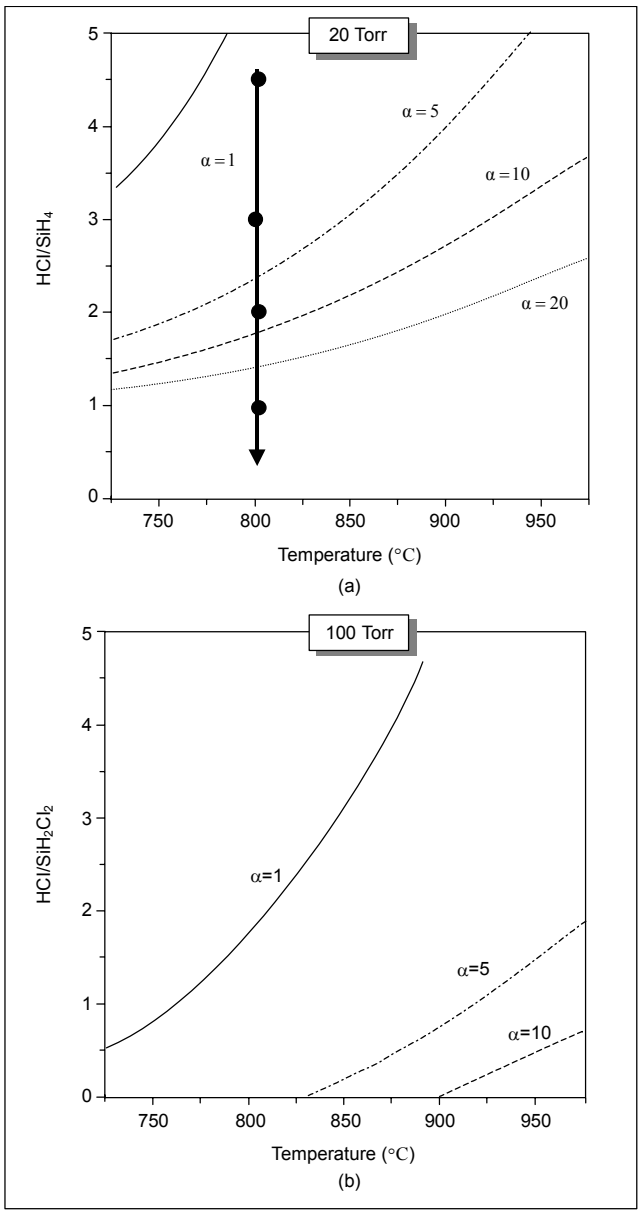

Fig. 1. SEG process diagrams calculated by CVD thermodynamics. (a) MS-HCl-H_2 system, at 20 Torr, MS=0.2, H_2=20 slm, (b) DCS-HCl-H_2 system, at 100 Torr, DCS=0.2, H_2=20 slm (α = supersaturation ratio).

introduced the supersaturation ratio as a reliable barometer for the SEG process. The supersaturation ratio is defined as the ratio of the equilibrium partial pressure in the gas phase to the vapor pressure of the element in the reference state (denoted as 'α'). The method of calculation was shown in [8]. Figures 1(a) and 1(b) are typical SEG process diagrams calculated by CVD thermodynamics. Here, the curved line indicates the iso-supersaturation ratio. Both were obtained from the input gas ratio of the reactant gas (MS, DCS):HCl:H_2 =1:X(0-5):100. Figure 1(a) shows the iso-supersaturation ratio curves for silicon in the MS-HCl-H_2 system when both the temperature and gas ratio change at a constant pressure of 20 Torr. The supersaturation ratio increases with the temperature at a constant gas ratio (HCl/MS). Figure 1(b) shows the iso-supersaturation ratio curves in the DCS-HCl-H_2 system at 100 Torr. We chose the condition of 100 Torr at 900 °C in the DCS system because guaranteeing selectivity on nitride can be favorable at higher pressures when the temperature increases up to about 900 °C. On the other hand, a lower pressure condition can be favorable for obtaining selectivity on the insulator at reduced temperatures as in this MS system.

We made SEG tests to verify the successful SEG zone in the proposed SEG diagrams. Figure 2 shows the results for the MS-HCl-H_2 system, where the experimental conditions were MS=0.2, H_2=20 slm (standand liter per minute), 800 °C, 20 Torr, and 200 seconds, and at various HCl flow rates. Successful SEG on the oxide pattern with a nitride spacer was obtained at the conditions of HCl=0.9 slm (Fig. 2(a)). At HCl=0.6, the selectivity on the oxide surface was ensured, but that on the nitride spacer was lost, that is, poly crystalline silicon was formed on the nitride spacer. Moreover, at HCl=0.4, the selectivity was lost on even the oxide surface, and finally the condition of HCl=0.2 broke epigrowth even on the silicon surface because of an extremely high driving force for growth. The growth rates were 63, 220, 485, and 1370 Å/minute at HCl flow rates of 0.9, 0.6, 0.4, and 0.2 slm, respectively, which proved to be inversely proportional to the trend of selectivity. These results revealed that the reasonable SEG process zone in MS-HCl-H_2 ranged from one to five in the supersaturation ratio. SEG tests in the DCS-HCl-H_2 system resulted in a similar range [5], but did not break the epigrowth. We believe that the DCS system has more halogen atoms than the MS system has, so it has a lower value of driving force for silicon growth. Our results suggest that these kinds of SEG diagrams would be good guidelines for the process, since there are few proper simulation tools for SEG.

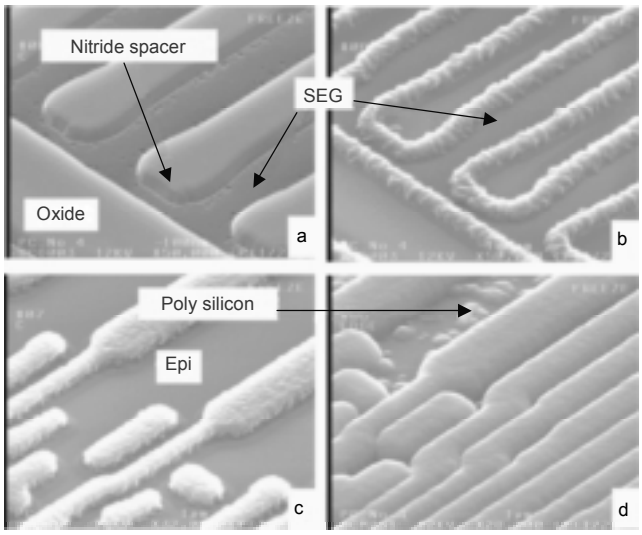

Fig. 2. SEM photographs showing the results tested in the MS-HCl-H_2 system at the conditions of MS=0.2, H_2=20 slm, 800 °C, 20 Torr, for 200 s. (a) HCl=0.9, (b) HCl=0.6, (c) HCl=0.4, and (d) HCl=0.2 slm. As the superasturation ratio increases, the selectivity loss occurs on nitride (b), on oxide (c), even breaking epi-growth (d) in sequence.

2. Loading Effect

In the SEG process, the loading effect may be classified according to two approaches. One is macroloading, which covers hundreds of micrometers. The accumulation of silicon sources from the insulator into the silicon active (opened) area occurs in a wide area, which is strongly dependent upon pattern size and the area fraction of the insulator of the wafer. The other is microloading, which explains the local growing-phenomenon only within an area smaller than about 10 μm and is easily affected by pattern shape and pattern depth (or aspect ratio). Undoubtedly, these two loading effects are governed by the pattern material and SEG process conditions.

We considered it important to verify the macroloading effect, now referred to as the loading effect in this paper, because it can affect both overall selectivity and growth uniformity on a wafer. Recently, [5] suggested that the loading effect be expressed by a deviation parameter (or nonequilibrium factor) in the thermodynamic analysis of SEG. The supersaturation ratio in the left graph in Fig. 3 decreases with the flux of HCl, under the condition of DCS=0.2, H_2=20 slm, 900 °C, and 100 Torr. The right graph in Fig. 3 shows the curves of the effective supersaturation ratio (ESR) at the typical HCl flows, that is, the supersaturation ratio multiplied by the factor 1/(1-*b*) (*b*= the ratio of the insulator area to the total wafer surface). The ESR indicates the supersaturation ratio in a real pattern, expressing the loading effect. In the extremely low active area, for example, 5%, the ESR reached about 100 at an HCl flow of 200 sccm, where the selectivity loss broke out instantly.

We prepared three kinds of E-beam patterns to evaluate the loading effect, or ESR. The E-beam <1> pattern had

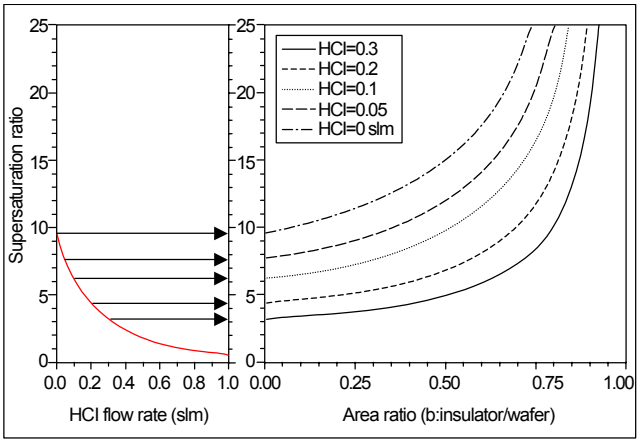

Fig. 3. The effective supersaturation ratio curves at the conditions of DCS=0.2, H_2=20 slm, 900 °C and 100 Torr, with the flux of HCl (0, 0.05, 0.1, 0.2, 0.3slm) as a function of the fraction of the insulator area, showing the loading effect.

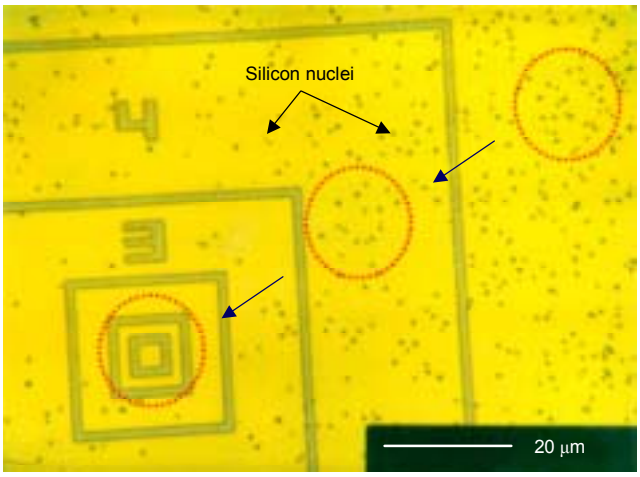

Fig. 4. Photograph showing the overflowing effect of the silicon flux. The density of the silicon nuclei on the nitride decreased remarkably from the edge to the center of E-beam <1> rectangular pattern under the conditions of DCS=0.2, HCl=0.25, H_2=20 slm, 900 °C, 100 Torr, for 250 s.

rectangular insulator patterns with doubly-increased spacing, separated by the same active line with a width of 2 μm. When the test conditions were DCS=0.2, HCl=0.25, H_2=20 slm, 900 °C, 100 Torr, and 250 seconds, the density of the silicon nuclei decreased gradually toward the center of the pattern, expressed as circles in Fig. 4. From the phenomenological point of view, it was necessary to consider the critical insulator distance (or diameter) for nucleation as the macroloading distance (MLD), which is the minimum area on the insulator for nucleation. This means that silicon nuclei will form on the insulator surface larger than the MLD at a certain SEG condition. In the E-beam <1> pattern, however, the MLD could not be exactly analyzed due to the very low fraction of the active area (below about 5%). The small silicon active area could not sufficiently accept the silicon sources produced from nearby gas-phase reactions, so that the silicon sources easily overflowed from one insulator pattern to next, consequently causing nucleation of the silicon on most insulator patterns (ESR reaches one higher than a critical limit for nucleation).

To prevent overflowing of the silicon sources, we designed the E-beam <2> pattern, which had a line-type insulator with a doubly-increased width: 4, 8, 16, 32, 64,…,8192 μm, where the silicon active area width was the same as the insulator, resulting in a 50% active area on the wafer surface. A cross-sectional TEM picture (Fig. 5 (a)) showed SEG at the boundary of the pattern. In the SEM photographs shown in Figs. 5(b), 5(c), and 5(d), the MLD on the nitride patterns (a 3000 Å nitride layer by PECVD, non-metal) under the same SEG conditions as in Fig. 4 reached a value between 512 and 1024 μm. In another test, the MLD on the oxide patterns was about 10 times larger than that on the nitride due to the lower density of surface defects and removal of silicon nuclei by generation of SiO [9].

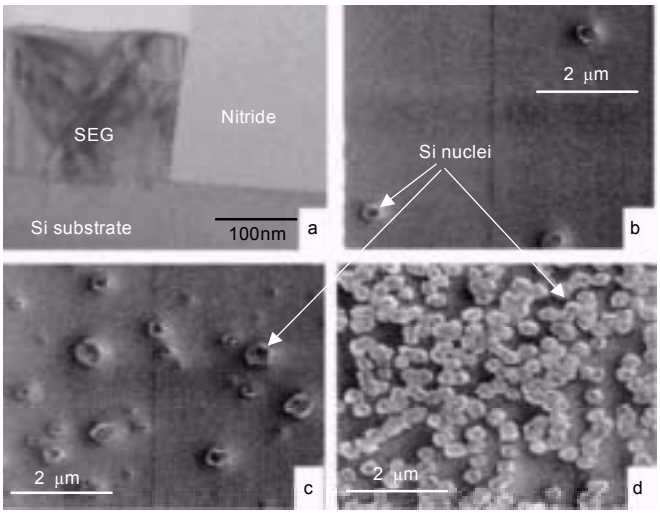

Fig. 5. TEM cross-sectional picture showing SEG and SEM planar photographs showing selectivity loss on the nitride surface of a one-dimensional E-beam <2> pattern, at the same condition as in Fig. 4. (a) pattern boundary, (b) 1024 μm, (c) 2048 μm, (d) 8192 μm. (the nitride surface width).

3. Improvement of Selectivity

Improving selectivity simply requires increasing the MLD. If a wafer has no insulating patterns larger than the MLD at a given condition, selectivity loss will not occur. To achieve this condition, nucleation of the silicon on the insulator must be suppressed. Figure 6 schematically shows the E-beam <2> pattern. The figure shows that the nucleation of the silicon is affected by three decisive parameters, the SEG conditions,

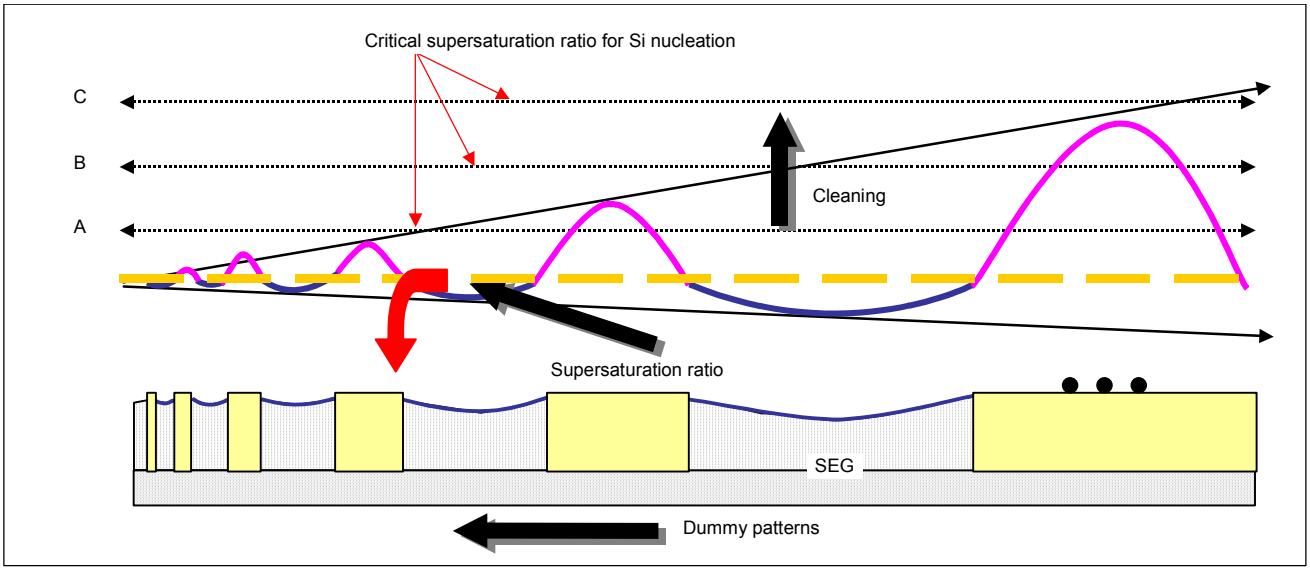

Fig. 6. Schematic description of the E-beam <2> pattern and three decisive factors on the selectivity control. The dotted horizontal bar indicates the critical supersaturation ratio for nucleation, A: for impurities, B: for nitride, C: for oxide. The curved line indicates the effective supersaturation ratio on the patterns.

pattern materials (including contaminants), and pattern width. In the SEG process, reducing the supersaturation ratio by increasing the HCl flow suppresses the nucleation (expressed as the thick dashed line in Fig. 6), but it demands more processing time for SEG because of the reduced growth rate, as verified in Fig. 2. Because a high thermal budget process can degrade device performance in general, SEG in LPCVD should be carried out at a low temperature and as fast as possible [10]. Therefore, this method is undesirable for optimization of SEG.

In the second method, impurities, such as metals and other conducting materials, can promote the nucleation on the insulator. Therefore, good cleaning processes are necessary for a wider MLD, or improvement of selectivity. Figure 7 shows the results obtained at the same experimental conditions as in Fig. 4, using uncleaned E-beam <2> patterns with a different layer stack, where the nitride layer (3000 Å) by PECVD was elevated on the tungsten (W) layer (1000 Å) by sputtering, followed by metal etching, and spacer nitride (300 Å) was formed both by LPCVD and by a blanket RIE process. Silicon nuclei formed even on the shortest insulator pattern, 4 μm wide, and the nucleus density was almost uniform up to the 256 μm surface, which means that the critical supersaturation ratio for nucleation became very low due to W impurities. From the TEM cross-sectional view, polycrystalline silicon grew even on the silicon substrate. However, when an H_2SO_4 solution mixed with H_2O_2 [1:1] was used to clean the wafer after metal etching for 10 minutes at 90 °C [11], the MLD increased to 512 μm.

The third method involves decreasing the pattern width. The insertion of proper dummy patterns into the wide insulator

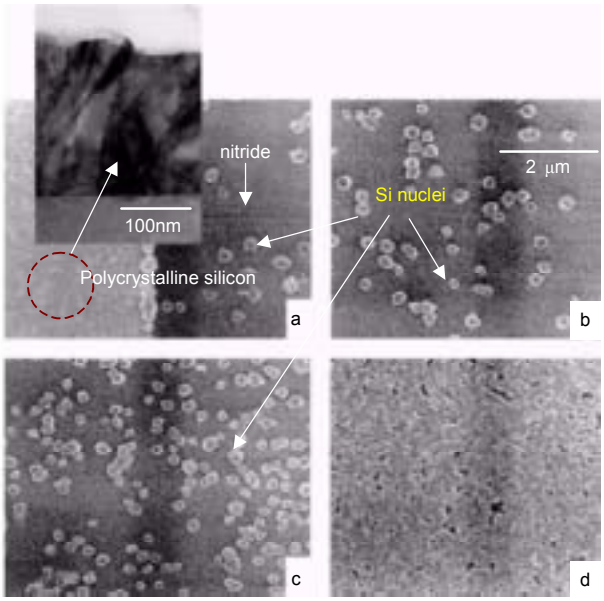

Fig. 7. SEM planar photographs showing the results tested at the same conditions as in Fig. 4 in an uncleaned E-beam <2> pattern with a nitride/tungsten stack. (a) boundary region (4 μm), center position of nitride surface. The circle was enlarged by TEM cross-sectional view, (b) 16 μm, (c) 512 μm, (d) 1024 μm, respectively.

effectively improves the selectivity and growth uniformity. Using an E-beam <3> patterned wafer, we analyzed selectivity and growth uniformity simultaneously as a function of the active area fraction. This pattern included three sections (left, middle, right). The left one was the reference (a 50% active area) to measure the growth uniformity depending on the

middle one, which had various ratios of the active area (10%, 20%, 30%, 40%, and 50%) as dummy patterns. The dimensions of these two sections were the same, namely, the width was 4 mm, and the length 10 mm. We designated the right one to evaluate the MLD using a multistep insulator surface (100, 300, 500, 1000, and 2000 μm widths).

The E-beam <3> patterned wafer was tested under the conditions of DCS=0.2, HCl=0.2, H_2=20slm, 900℃, 100 Torr, and 200 seconds, where the pattern formation process was the same as in Fig. 7, except for the addition of the metal cleaning step. Figure 8 shows the growth uniformity on the reference pattern, where in the middle section of the dummy active 10%, SEG in the boundary between the reference area and the dummy active area grew thicker (by about 20%) than SEG did in the center position of the left section, while the one in the dummy active 50%, SEG grew uniformly all over the patterns. Moreover, from the right section, in the 10% dummy active area, selectivity loss occurred even on the insulator surface with a 100 μm width, while in the 50% dummy active area the selectivity loss occurred on the one with a 500 μm width. This means that only well-inserted dummy patterns can improve the selectivity on a wafer by consuming excessive silicon sources piled up abnormally on a wide insulator. From these results, we induced a dummy generation rule, that is, dummy patterns should be inserted on a wide insulator area with uniform spacing and an active area fraction similar to the main cell patterns. This is the key to optimizing the SEG process for the pattern generation.

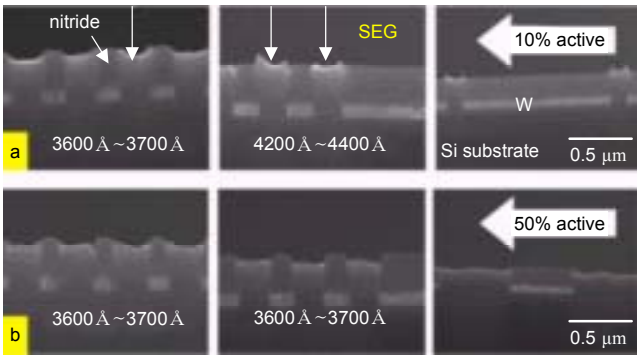

Fig. 8. SEM photographs of SEG grown in the E-beam <3> pattern, under the conditions of DCS=0.2, HCl=0.20, H_2=20 slm, 900 °C, and 100 Torr, 200 s. (a) 10% dummy active region, and (b) 50% dummy active region. The left photographs show the center of the cell pattern, and the middle ones the boundary region between the cell and dummy pattern, and the right ones show the center of the dummy pattern, respectively.

IV. Conclusions

Our study produced SEG process diagrams, derived from the CVD thermodynamics on gas-phase reactions in LPCVD and experimentally evaluated by MS-HCl-H_2 system. These diagrams offer a guideline for a successful SEG process range. The loading effect was the typical SEG phenomenon affecting selectivity and growth uniformity as well as the major problem preventing the successful application of SEG to electronic devices. We verified and controlled the loading effect with the help of both the concept of an effective supersaturating ratio and three kinds of E-beam patterns. More importantly, to optimize the SEG process, we found that it is important both to clean the wafer and to suppress a local increase of the supersaturation ratio by inserting dummy active patterns into a wide insulator.

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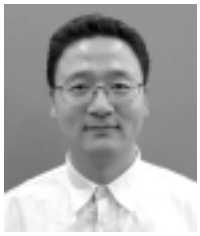

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