A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems

Seok-Bong Hyun, Geum-Young Tak, Sun-Hee Kim,
Byung-Jo Kim, Jinho Ko, and Seong-Su Park

This paper reports on our development of a dual-mode transceiver for a CMOS high-rate Bluetooth system-on-chip solution. The transceiver includes most of the radio building blocks such as an active complex filter, a Gaussian frequency shift keying (GFSK) demodulator, a variable gain amplifier (VGA), a dc offset cancellation circuit, a quadrature local oscillator (LO) generator, and an RF front-end. It is designed for both the normal-rate Bluetooth with an instantaneous bit rate of 1 Mb/s and the high-rate Bluetooth of up to 12 Mb/s. The receiver employs a dual-conversion combined with a baseband dual-path architecture for resolving many problems such as flicker noise, dc offset, and power consumption of the dual-mode system. The transceiver requires none of the external image-rejection and intermediate frequency (IF) channel filters by using an LO of 1.6 GHz and the fifth order on-chip filters. The chip is fabricated on a 6.5-mm^2 die using a standard 0.25-μm CMOS technology. Experimental results show an in-band image-rejection ratio of 40 dB, an IIP3 of -5 dBm, and a sensitivity of -77 dBm for the Bluetooth mode when the losses from the external components are compensated. It consumes 42 mA in receive π/4-diffrential quadrature phase-shift keying (π/4-DQPSK) mode of 8 Mb/s, 35 mA in receive GFSK mode of 1 Mb/s, and 32 mA in transmit mode from a 2.5-V supply. These results indicate that the architecture and circuits are adaptable to the implementation of a low-cost, multi-mode, high-speed wireless personal area network.

Keywords: Radio transceiver, RF integrated circuits, CMOS RF, Bluetooth, wireless personal area network.

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Seok-Bong Hyun (phone: +82 42 860 1274, email: sbhyun@etri.re.kr), Geum-Young Tak (email: gytak@etri.re.kr), Sun-Hee Kim (email: ksh63433@etri.re.kr), Byung-Jo Kim (email: kimbj@etri.re.kr), and Seong-Su Park (email: sspark@etri.re.kr) are with Basic Research Laboratory, ETRI, Daejeon, Korea.

Jinho Ko (email: jhko@phychips.com) is with PhyChips, Daejeon, Korea.

I. Introduction

Short-range wireless transceivers for global standards such as Bluetooth and IEEE 802.11b/a/g wireless local area networks (WLANs) have been extensively developed [1]-[12], and a number of them have recently been commercialized successfully. Further research has continued to implement even lower cost, lower power, higher speed, and multi-standard transceivers for use in a future ubiquitous network. Among the various wireless standards, Bluetooth is adequate for a moderate wireless personal area network (WPAN) and a digital home network because it can support a synchronous connection-oriented link for streaming audio applications. It also supports packet switching protocols, and a number of profiles for most personal devices are readily available [13]. Such versatile and low-power features are strong points compared with WLAN. However, the instantaneous bit rate of 1 Mb/s specified by the current Bluetooth standard is not enough nowadays to satisfy demand for much higher-speed multimedia services and acts as one of the fundamental limiting factors for proliferating Bluetooth. Thus, a new standard called high-rate Bluetooth, or Bluetooth-2 (BT2), has been investigated to improve the data transfer speed while inheriting the merits of the current Bluetooth. Although the BT2 specification is not yet established, and the Bluetooth special interest group responsible for developing the new specification is not active, the special interest group suggests that the BT2 operate in the same band as Bluetooth for backward compatibility. The instantaneous bit rate can be 4, 8, or 12 Mb/s for π/2-differential binary phase shift keying (π/2-DBPSK), π/4-diffrential quadrature PSK (π/4-DQPSK), and 8-DPSK modulation modes, respectively [14].

In this paper, we present the architecture and circuits of a dual-mode CMOS transceiver designed for both normal-rate Bluetooth (BT1) and high-rate Bluetooth. Compared to prior arts and reports, we emphasize the dual-mode functionality, cost, and power consumption in maintaining the advantages of the current Bluetooth. Although a number of Bluetooth or WLAN transceivers have been reported, we are the first to design and test the dual-mode transceiver IC for both BT1 and BT2. We chose the 0.25-μm CMOS process because it has a superior mass productivity and allows the implementation of an ultimate system-on-a-chip including CMOS RF, digital signal processors, memories, and peripherals. Although we employ a dual-conversion architecture, external image-rejection filters and bulky intermediate frequency (IF) filters are not required, and the transmitter and receiver share a single local oscillator (LO), further reducing the cost and power consumption. In section II, we present the proposed transceiver architecture, and in Section III, we describe the circuit details. Section IV summarizes the experimental results.

II. Transceiver Architecture

An overall block diagram of a high-rate Bluetooth system consisting of an RF transmitter, receiver, frequency synthesizer, digital baseband processor, access controller, and external passives is shown in Fig. 1. This paper describes a dual-mode radio transceiver chip integrating RF front-end and baseband analog (BBA) sections, which are shown in Fig. 2. The RF front-end consists of a low noise amplifier (LNA), a quadrature up/down mixer, and a driver amplifier (DA). A frequency synthesizer and an analog-to-digital converter (ADC) are not implemented on-chip due to the limited number of chip pads and a complexity of evaluation. However, we have also fabricated and tested the blocks on separate chips. The proposed receiver employs two different BBA blocks, one for

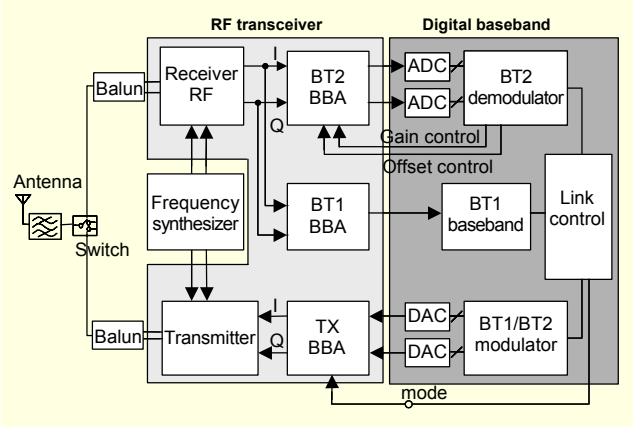

Fig. 1. High-rate Bluetooth system architecture.

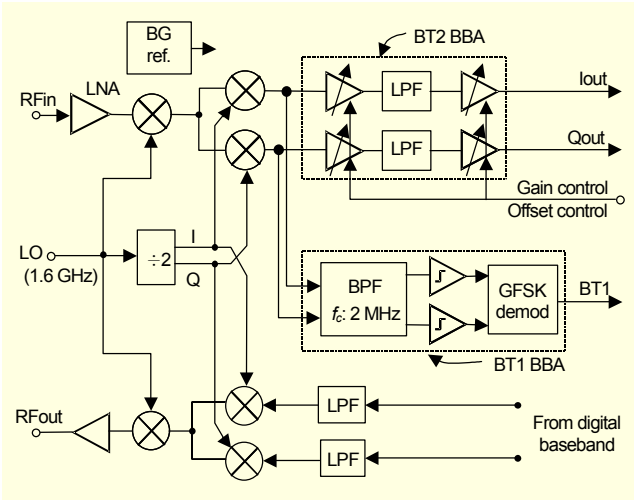

Fig. 2. RF transceiver chip block diagram.

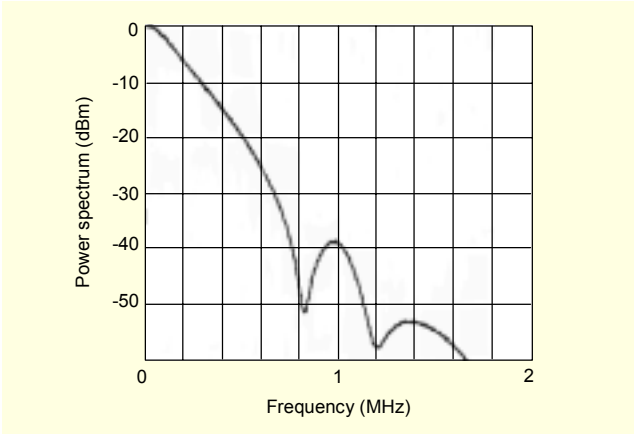

Fig. 3. Power spectrum of a GFSK modulated signal at baseband according to the Bluetooth 1.1 specification.

BT1 and the other for BT2, while sharing most of the radio building blocks such as the RF front-end and frequency synthesizer. We call this architecture a baseband dual-path. We chose this architecture because the baseband spectrum characteristics and corresponding optimal demodulators for BT2 are very different from those for BT1. In a baseband BT1 signal, 99% of the signal power is contained within a dc of up to 500 kHz, as illustrated in Fig. 3, while the power spectrum density of the BT2 signal is uniform over a 2-MHz bandwidth. The effects of these spectrum characteristics will be explained later.

It is well known that the architecture and frequency plan have a great deal of influence on the performance and complexity of an overall system. The RF transceiver described in this paper uses a dual-conversion architecture [1],[2],[11] with a first LO frequency of 1.6 GHz and a second LO frequency of 0.8 GHz, which is simply generated by dividing the first LO by two. On the receiver side, an incoming 2.4-GHz

RF signal is first down-converted to 0.8 GHz by the first LO and then converted to the baseband quadrature signals. The first LO frequency for the BT1 mode is different from that for the BT2 and is given by

$$f_{LO_1} = \frac{2}{3}\left(f_{RF} + 2\,\text{MHz}\right), \quad (1)$$

where f_{RF} is the desired RF carrier frequency. Thus, the carrier frequency after the second down-conversion becomes 2 MHz. We chose a 2-MHz IF because it enables a low current and low complexity implementation [3]. On the other hand, the LO frequency for the BT2 mode is simply two-thirds of the RF frequency. Thus, the carrier frequency after the second down-conversion becomes 0 Hz. The baseband signals are then applied to channel-select, low-pass filters (LPF) for the BT2 mode or band-pass filters (BPF) for the BT1 receive mode.

As shown in Fig. 4, the image signal is located 1.6 GHz away at a 0.8-GHz band. Thus, the image can be easily attenuated using the band-pass characteristics of the RF filter and the LNA. Although a dielectric filter alone can not attenuate the image tone more than 40 dB, we can obtain an overall image rejection of more than 80 dB by using a matching network as an additional high-pass filter. As a result, an image-reject mixer or filter is not required in the receiver. The transmitter up-converts the baseband quadrature signals to 0.8 GHz using a pair of quadrature mixers and subsequently to 2.4 GHz using the RF mixer. The up-converted 2.4-GHz signal is finally transferred to the antenna through a DA, an external switch, and an RF filter. An external notch at 825 MHz between the antenna and switch may be required to reduce the images further since there is a 3-MHz overlap with IS95 for the cellular code division multiple access or GSM800 transmit bands [2]. The frequency of the IS95 CDMA reverse link is 824 to 849 MHz [15], while the image lies in the range of 800 to 827 MHz for a signal band of 2400 to 2480 MHz.

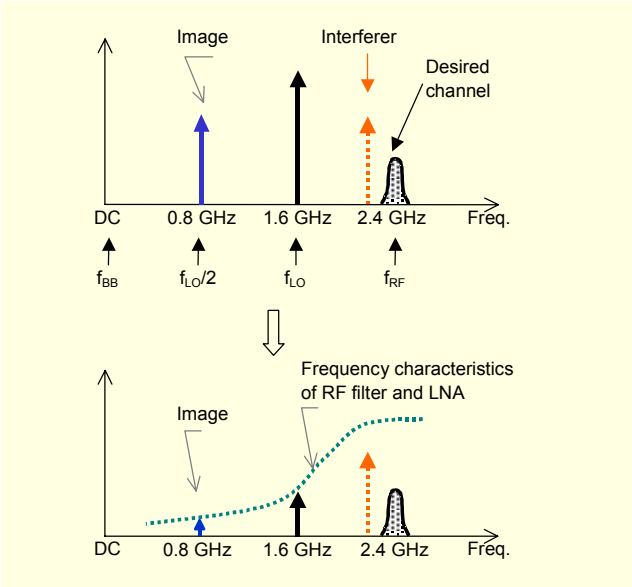

Fig. 4. Receiver frequency plan and image rejection scheme.

While a direct-conversion (Zero-IF) architecture is usually preferred in a fully integrated design these days [4]-[6], [12], one is not used in this design based on the following reasons.

First, a Gaussian frequency shift keying (GFSK) modulated spectrum for BT1 has considerable energy at a 0 Hz dc, as shown in Fig. 2, which is very different from the spectrums of popular modulations such as QPSK orthogonal frequency division multiplexing, wide-band FSK, and so on. Thus, a flicker noise and dc offset problems may be more serious [3]. Note that MOS devices exhibit significantly more 1/f noise than do bipolar junction transistor devices [16], and most commercial direct-conversion chips rely on bipolar junction transistor device technologies [4]-[6] or on the wide-band nature of modulated signals [17], in which the flicker noise effect is not significant.

Second, the direct-conversion receiver may require more power-hungry blocks than the dual-conversion presented in this paper. The 2.4-GHz phase-locked loop frequency synthesizer for the direct-conversion consumes more power than the 1.6-GHz PLL. Polyphase filters used for the generation of quadrature LOs at 2.4 GHz may consume more power than the divide-by-two circuit of 0.8 GHz used in this design. Moreover, a limiting amplifier cannot be used at the BBA stage for the BT1 mode [3]. An automatic gain control (AGC) circuit may solve this problem. However, the AGC consumes more power, which is undesirable for the BT1 mode while acceptable for the BT2 mode. The narrow-band channel selection BPF, the limiting amplifier, and the GFSK demodulator centered at 2 MHz employed in this transceiver consume less power and less chip area. Even an ADC is not necessary for the BT1 mode, since we implemented the demodulation in the BBA section using an analog GFSK demodulation method.

Unlike the case of BT1, it is not efficient to design a complex channel selection BPF and M-ary DPSK demodulator centered at 2 MHz for the BT2 mode due to its much larger bandwidth and increased complexity. Thus, it is preferable to use an LPF for channel selection and a digital demodulator for a wide-band DPSK modulated signal.

Although we employ the dual-conversion in this design, the integration level can equal that of the direct-conversion without the drawback of the well-known dc offset problem. Also, our design requires no external components except the low cost RF filter, balun, and capacitors. The high level of integration allows for a high-impedance interface between the on-chip RF

components [18], which further reduces the currents consumed by the output buffers in each block.

III. Circuit Implementation

1. Receiver RF Front-End

The receiver front-end in the transceiver IC consists of an LNA and dual-conversion mixer. Since typical Bluetooth and WLAN devices do not require high performances while demanding low cost and small form factor implementation, it is common to use a deep sub-micron CMOS or Bipolar CMOS (BiCMOS) technology for short-range applications.

We implement a fully differential receiver to reduce both the undesired coupling through the low resistance substrate and the common mode switching noise from the digital circuits. An external balun is needed for the single-ended to differential conversion of the antenna signal.

Figure 5 shows a simplified schematic of the LNA. The LNA consists of the cascoded differential pairs M1 to M4 with resistive loads R1 and R2. The inductively degenerated common source topology has been widely used for low noise performance [18], [19]. However, since we focus particularly on a dual-mode low cost implementation in this design, we try to avoid the use of on-chip inductors that occupy a lot of area and thereby increase the production cost. Although the source inductors are not used in the LNA, the simulated noise figure (NF), gain, and IIP3 with an external matching circuit are 1.7 dB, 15 dB, and -10.5 dBm, respectively, which meet the block specifications for both the BT2 and BT1 modes. The LNA input is connected to the external 100 Ω balun transformer, and the output is interconnected to the mixer through on-chip coupling capacitors.

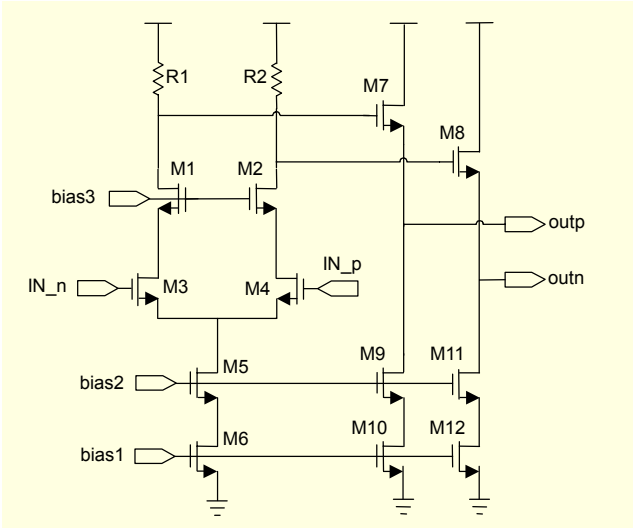

Fig. 5. Simplified schematic of the 2.4-GHz LNA integrated in the BT2 transceiver IC.

The first mixer which down converts the RF signal to an 800 MHz IF is directly interconnected to the second and third quadrature mixers. Figure 6 shows a simplified schematic of the down-conversion mixers. We focus on the voltage conversion gain instead of the power gain because the output of the mixer is directly interconnected to the BBA stage which has a very high input impedance (larger than 1kΩ), and thus there is no need to drive external 50 Ω lines in the highly integrated receiver. We predicted the circuit performance by using simulators such as Spectre and ADS and by relying on the BSIM3v3 device models for the RF MOS transistors provided by the foundry. The measured performance results of the down conversion mixers agree well with the simulations, as shown in Table 1.

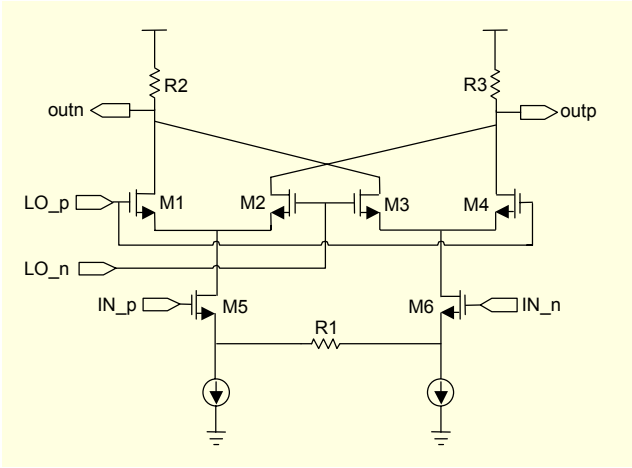

Fig. 6. Simplified schematic of the down-conversion mixers.

Table 1. Measured performance of mixers in the receiver.

Parameters	Simulation	Measurement
Conversion gain (dB)	6.2	5.4
IIP3 (dBm)	0.5	0.4
NF	21.6	-
Current consumption	10.4 mA	10.4 mA
Impedance	Input 100 Ω, Output > 1 kΩ	

2. BBA for Normal-Rate Bluetooth Receiver

The BBA for the BT1 receiver consists of a complex channel selection BPF, a limiting amplifier, a GFSK demodulator, and a slicer.

The complex channel selection band-pass filter is a key building block which replaces the external bulky IF filters and rejects an in-band image signal. For a typical low-IF Bluetooth receiver, the image signal is an in-band Bluetooth-modulated

adjacent channel interferer, which becomes a co-channel interference after down-conversion [3], [8]. Although the receiver in this design employs the dual-conversion, it also uses the in-band image similar to the prior Low-IF receiver. We determined the order of the filter to be fifth in order to meet the adjacent channel interference and in-band image specifications. An image rejection of 30 dB is sufficient to meet the co-channel specification. The image rejection ratio (IRR) of the fifth-order filter is above 80 dB in the simulation. Because of a device mismatch and an LO phase error, the measured IRR is degraded. The phase error of 1° is equal to the IRR degradation of -35 dB [20]. Figure 7 shows the measured frequency response of the complex filter for the signal and image bands. From this figure, the measured image rejection ratio is about 40 dB.

We implemented the complex filter using an active-RC technique with op-amps, as shown in Fig. 8. Five stages are cascaded to build the fifth-order complex filter. The capacitors used in the filter consist of binary weighted capacitors and switching transistors for tuning. The center frequency, 3-dB bandwidth, and pass-band gain of the filter are 2 MHz, 1.1 MHz, and 22.5 dB, respectively.

The selected channel at the filter output is amplified by I- and Q-limiting amplifiers to a well-defined level. Since Bluetooth uses GFSK modulation, in-band linearity is not a major issue. The limiting amplifier consists of four stages of a 13-dB voltage gain in each stage, as shown in Fig. 9. Thus, it provides an overall gain of 52 dB. Each gain stage is ac-coupled to remove the dc offset.

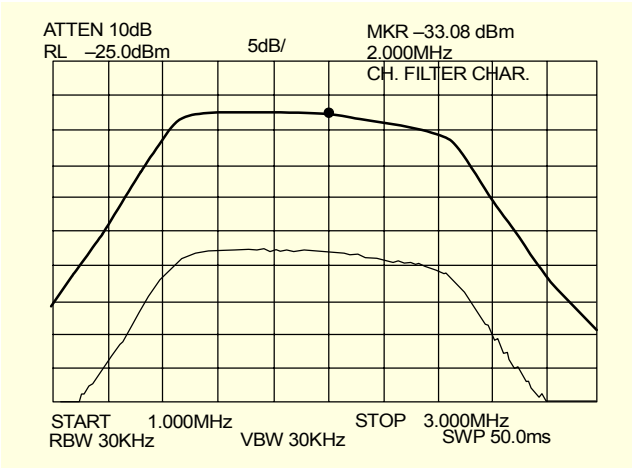

Fig. 7. Measured complex filter frequency response.

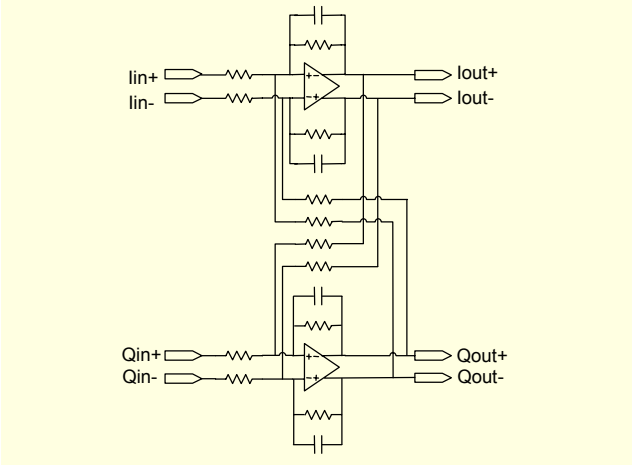

Fig. 8. A circuit which has a single complex pole. Five stages are cascaded to build the fifth order band-pass response.

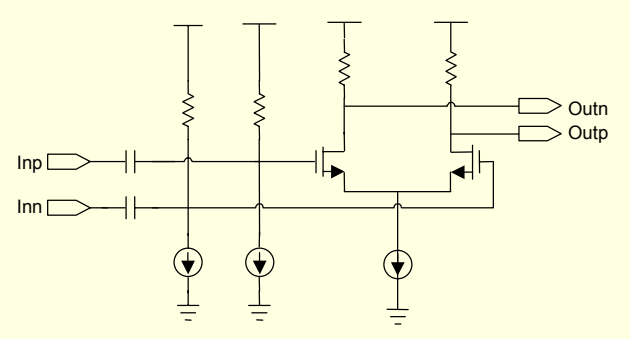

Fig. 9. Circuit of the voltage gain amplifier stage in the limiter.

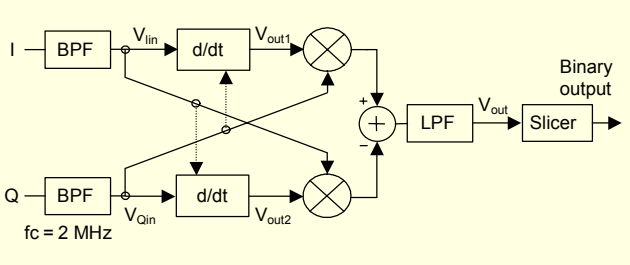

Fig. 10. Block diagram of balanced quadricorrelator for FSK demodulation.

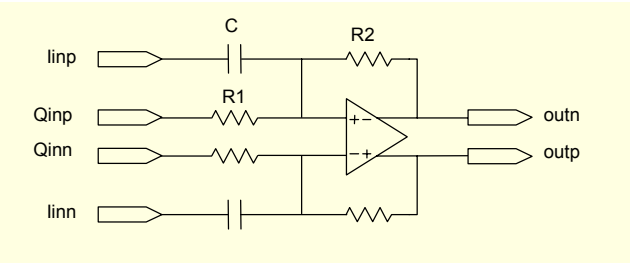

Fig. 11. Schematic of the differentiator in the FSK demodulator.

Following the limiter is an analog FSK demodulator, as shown in Fig 10, which is a well-known balanced quadricorrelator circuit [21]. We choose the demodulator because the topology is well known and simple compared with other implementations [10], [22], and its performance has been

proven sufficiently reliable. A band-pass filter at the input stage rejects the harmonics produced by the limiting amplifiers. The demodulator consists of I and Q differentiators and multipliers. We implemented the differentiator by the active RC technique using an op-amp, as shown in Fig. 11. If the signals at the differentiator inputs are FSK modulated signals given by

$$V_{Iin}(t) = A\cos\left(\omega_{IF}t + \int f(\tau)d\tau\right)$$
$$V_{Qin}(t) = A\sin\left(\omega_{IF}t + \int f(\tau)d\tau\right), \quad (2)$$

where ω_{IF} is the IF frequency of 2 MHz, and $f(t)$ is the baseband data from the transmitter, then the signals at the differentiator outputs will be equal to

$$V_{out1} = AG\,V_{Qin}(t)\,f(t)$$
$$V_{out2} = -AG\,V_{Iin}(t)\,f(t), \quad (3)$$

where G is the differentiator gain. Thus, the signal at the multiplier output V_{out} will be equal to

$$V_{out} = AG\left(V_{Iin}(t)^2 + V_{Qin}(t)^2\right)f(t) = \mathrm{K}\,f(t), \quad (4)$$

where K is a constant. The capacitors in the differentiator consist of binary weighted capacitors and switching transistors to adjust the differentiator center frequency. A low-pass filter rejects the harmonics produced by the multiplier.

Since the LO frequency of a master device is not exactly equal to that of a slave in a Bluetooth pico-net due to a minute difference between the frequencies of each crystal clock [13], a dc offset voltage appears at the demodulator output. For example, if the frequency stability of the crystal clock is ±10 ppm, the frequency shift between the transmitter and receiver is ±24 kHz for the carrier frequency of 2.4 GHz. This frequency offset is converted to a voltage offset by the FSK demodulator. The dc offset can be removed by an analog or digital method [23]. We employ an analog method because it is simple and does not require an ADC, a power-hungry block. In the analog method, a slicer detects the envelopes of each differential pair of the analog output, generates their common mode dc voltage, and subtracts the voltage from each differential pair. Using a sample and hold (S/H) circuit, the dc voltage to be subtracted is tuned during the preamble and sync word period. A capacitor holds the tuned voltage during the rest of the packet period. The control signal of the S/H switch comes from the digital base-band section. Afterwards, we converted the produced signal to a digital bit-stream signal using a comparator.

3. BBA for High-Rate Receiver

The BBA for the BT2 receiver consists of a channel selection LPF and a variable gain amplifier (VGA) with a dc offset cancellation. We performed the M-ary DPSK demodulation in the digital baseband processor through an analog-to-digital conversion.

A VGA with a digital AGC loop is used for amplifying the received signal to a pre-determined amplitude level so that it fully swings in the fixed input range of the ADC. The BT2 receiver requires a VGA with a controllable gain range of 60 dB and a bandwidth of more than 2 MHz. The VGA described here has a continuously variable gain from 6 dB to 72 dB. To obtain such a gain control range, we use three VGA cells that

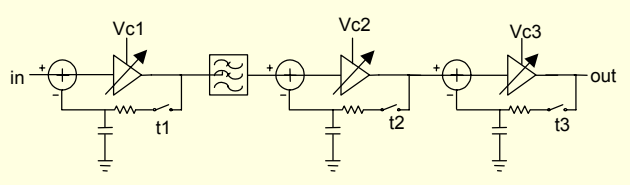

Fig. 12. Block diagram of the 3-stage VGA with DC offset cancellation at each VGA cell and a channel selection filter.

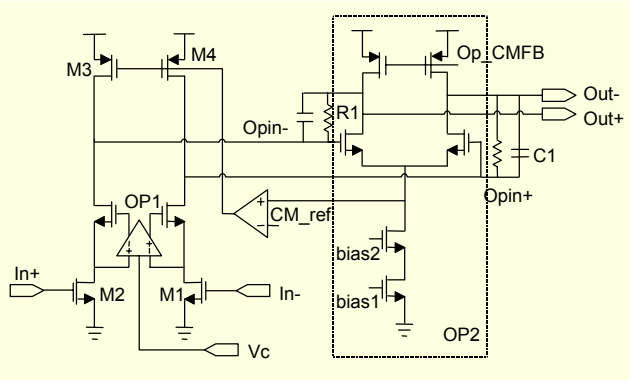

Fig. 13. Schematic of the VGA circuit with high linearity.

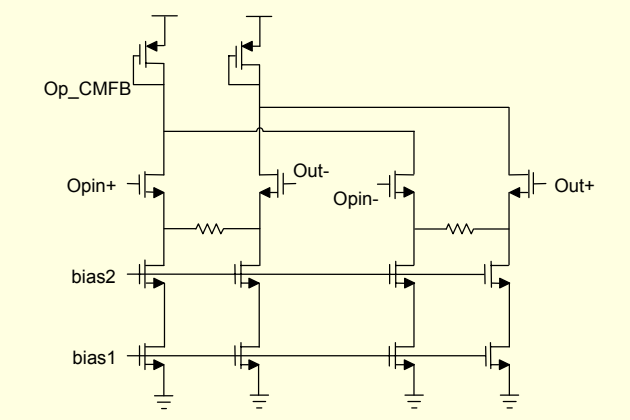

Fig. 14. Schematic of CMFB circuit of OP2 in Fig 13.

are cascaded, and the gain of each VGA is variable from 2 dB to 24 dB. The VGA must also be able to handle much larger signals in adjacent channels because the external high-Q channel selection filter is not used in this design. We inserted an on-chip channel selection filter between the 1st and 2nd stages of the VGA, as shown in Fig. 12. The channel selection filter is an active LPF with a cut-off frequency of 2 MHz and exhibits a large noise figure. The VGA must therefore have low-noise characteristics to reduce the effect of the filter noise.

A schematic of the VGA cell is shown in Figs. 13 and 14. A conventional transconductor [24] is used to obtain a variable gain and a highly linear characteristic. Different from the typical differential pair of transistors with a tail current source, this type of transconductor saves one drain-source saturation voltage for the tail current source and has the potential to achieve a wide linear input range. These characteristics are appropriate for a low supply voltage operation. The NMOS transistors M1 and M2 operate in the triode region, and the transconductance is proportional to drain to source voltage (V_{ds1}). A differential operation removes the V_{ds1}^2 term in the output current and the transconductor becomes highly linear [24], [25]. The gain of the VGA is proportional to the control voltage, V_{ds1}. To determine V_{ds1}, a differential operational amplifier, OP1, is used. The V_{ds1} of M1 and M2 is kept equal by OP1, and the common-mode of the V_{ds1} is determined by the common-mode feed-back (CMFB) of OP1.

The main limiting factor of the linearity of the transconductor is a finite output resistance of M3 and M4 current sources [25]. We can consider a typical cascode structure to improve the linearity performance. However, the cascode structure requires a higher supply voltage. In addition, although the range of the available gate bias voltage of the current source becomes narrow in the cascode topology, the variation range of the common mode current must be larger than 10 dB. These will lead to larger output current source dimensions and an increase in noise. Moreover, a stability of the CMFB loop is difficult to obtain because of the high common mode gain of the cascode structure. Therefore, instead of the cascode structure, the operational amplifier OP2 is used to form a virtual ground at the output of the transconductor in order to improve linearity. The V_{ds} of M3 and M4 are kept constant by OP2 and a virtual ground is formed. This is similar to a g_m-C operational transconductance amplifier technique in a filter application [29]. The CMFB of OP2 is shown in Fig. 14. The Op-CMFB bias is determined so that the output common mode voltage is equal to the input common mode voltage.

We placed capacitor C1 in the first stage VGA to generate a one real pole for a fifth order 2MHz cut-off low-pass response. The filter placed after the first VGA has the remaining four complex poles. The 3 dB bandwidth of the VGA is about 8 MHz and is constant across the entire gain range without C1. The combination of the filter and VGA has a frequency response dominated by that of the filter alone.

To remove the dc offset, we use the circuit shown in Fig. 12. While the switches t1, t2 and t3 are on, the low-pass filtered output signal is subtracted from the input signal, and the circuit has a high-pass ac response. When the period of a BT2 preamble ends, the switches are off and the capacitors hold the tuned voltage. The switch control signal comes from the digital base-band.

For a constant settling time of the AGC loop at whatever the input signal level, the VGA is designed to have an exponential gain characteristic with respect to the control voltage, Vc [26]. Because the gain of each stage described here is in linear relation to the control voltages Vc1, Vc2, and Vc3, a control circuit that generates an exponential voltage output is used to convert Vc into Vc1, Vc2 and Vc3. To implement the exponential function, a short channel transistor biased in the sub-threshold exponential region is used in the control circuit [27], and the output voltages Vc1, Vc2 and Vc3 are varied according to the scheme, as shown in Fig. 15. The measured VGA gain versus the control voltage is shown in Fig. 16.

To minimize the noise figure across the entire gain control range, the first stage has priority in gain assignment. The output noise across the VGA gain range is compared with the 3rd-order intermodulation products created by two in-band tones, as shown in Fig.17 [28]. The peak voltage at the VGA output

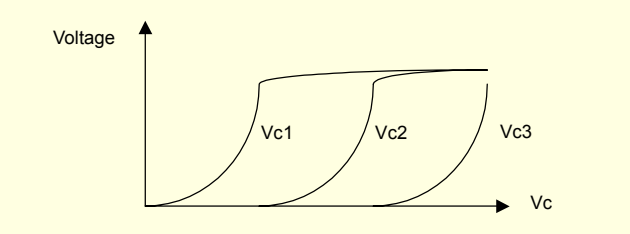

Fig. 15. Operation of the gain control circuit of the VGA.

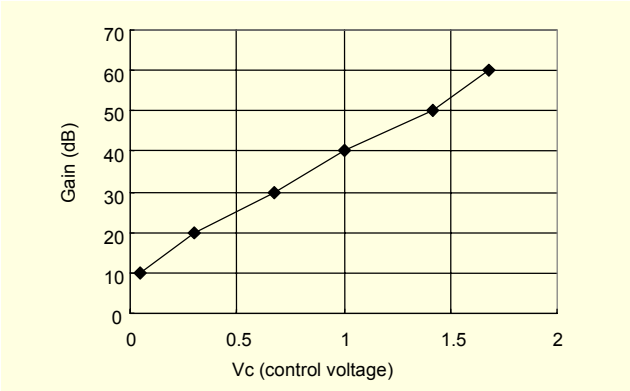

Fig. 16. Measured gain versus control voltage of the VGA.

is kept constant at a 1-V peak-to-peak differential. Although there is a trade-off between NF and linearity in the VGA, the output IM3 is smaller than the output noise voltage at any gain setting, and the output noise level is sufficiently lower (-20 dB) than the output signal voltage. Thus, the NF and linearity of the VGA meet the requirements.

The channel selection LPF has a fifth-order Butterworth response with a cutoff frequency of 2 MHz. The LPF is implemented based on an active-RC Sallen & Key structure, and has four complex poles using a bi-quad structure comprised of op-amps. One real pole is in the VGA. Due to the process variation of the on-chip resistors, the cut-off frequency could vary up to ±10% with a simple tuning circuit. However, this deviation is small enough not to affect the overall receiver performance because the offset frequency of the adjacent channel BT1 modulated interference is 4.5 MHz [14], which is much larger than the cut-off frequency of the filter. When the cutoff frequency is reduced to 1.6 MHz, an inter-symbol interference occurs and the sensitivity is degraded. We estimated the effects of the cut-off frequency variation in detail using the system level simulators such as ADS and MATLAB, although we did not present the results. The measured frequency response of the LPF is shown in Fig. 18, where the current consumption is 4.2 mA from a 2.5 V supply.

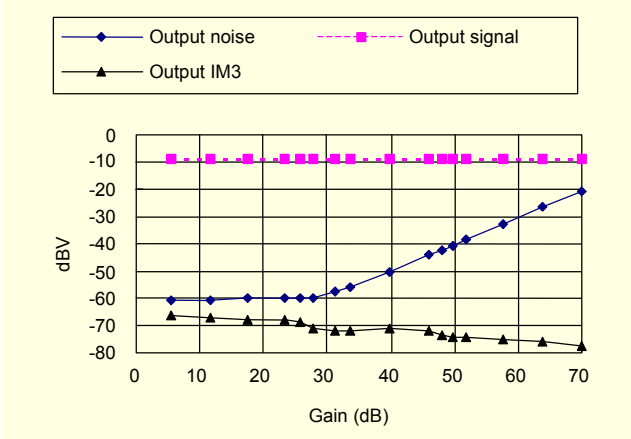

Fig. 17. Simulated output RMS noise voltage (noise bandwidth is 2 MHz) and in-band two-tone intermodulation products.

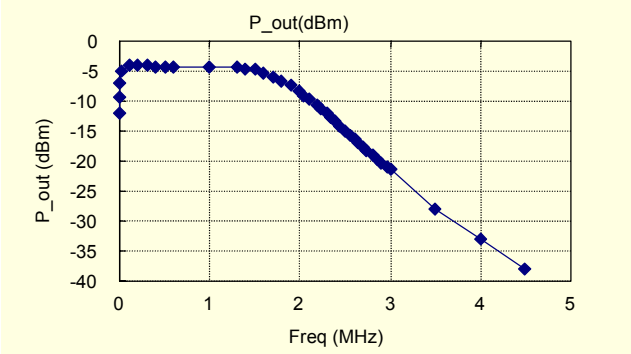

Fig. 18. Measured frequency response of the LPF for BT2.

4. Transmitter

The transmitter consists of an anti-aliasing LPF, a quadrature up-conversion mixer, and a DA. Since the baseband modulations are performed in the digital part and the noise is not a matter of concern in the transmitter, we employ a single BBA path.

Power efficiency and linearity are major concerns in a typical transmitter design. However, the Bluetooth and the high-rate Bluetooth transmitter do not demand high linearity because GFSK modulated signals exhibit a constant envelope waveform and can therefore be amplified by nonlinear amplifiers with no spectral re-growth [30]. DPSK modulations also have smaller phase changes, and the transmit power level is low (-1.25dBm) for the high-rate Bluetooth [14]. Thus, the output P1dB requirement is determined to be 3 dBm, which is not a difficult target. The DA, as shown in Fig. 19, is a fully differential cascoded circuit loaded by external inductors, which are used as a matching element. The simulated output

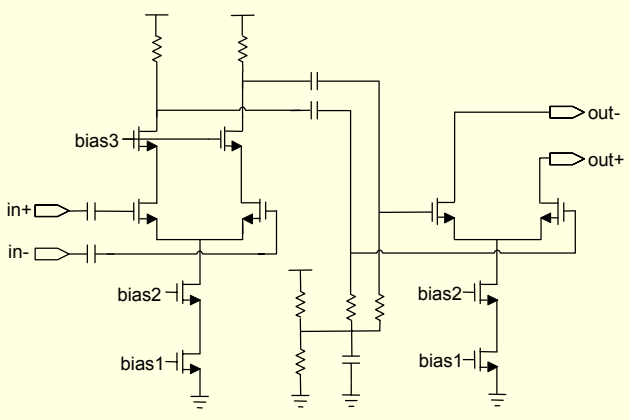

Fig. 19. Simplified schematic of the driver amplifier.

Table 2. Measured performance of transmitter excluding DA.

Parameters	Simulation	Measurement
Output power (dBm)	-15	-19
Carrier feed-through (dBc)	-	-20
Sideband rejection		-30
Tx LPF BW (BT1) (kHz)	800	750
Tx LPF BW (BT2) (MHz)	2	1.9
Current consumption (mA)	18	18

P1dB, power gain, stability, and current consumption of the DA are 1.5 dBm, 21 dB, larger than 6, and 14 mA, respectively. The measured and simulated performances of the transmitter excluding the DA are summarized in Table 2.

IV. Experimental Results

This transceiver was fabricated in a 0.25-μm, single-poly, five-metal CMOS technology. The die photograph is shown in Fig. 20. It occupies a core area of 6.5 mm^2 and is packaged in a 64-pin LQFP plastic package. The receiver chain dissipates 42 mA for the high-rate Bluetooth mode, and the transmitter consumes 32 mA from a 2.5-V power supply.

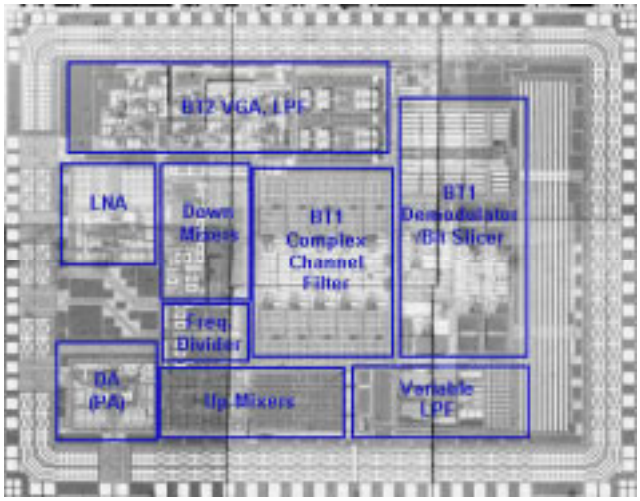

Fig. 20. Die photograph of transceiver.

Since we designed the input/output interface between each building block without a traditional 50-Ω matching circuit or output buffer, it is not possible to measure directly the characteristics of certain blocks such as the NF of LNA by themselves. Instead, we indirectly estimated the RF performance using the overall transceiver measurements. An unexpected loss of the external balun transformers used in the input stage of the LNA occurred during the measurements. The problem is caused by the facts that the manufacturer does not provide the equivalent circuit model of the balun and the scattering parameters of the balun are severely affected by the package parasitic and assembly condition. In order to avoid the uncertainty of the balun, we measure the RF front-end with a single-ended configuration; that is, one of the differential input ports of the LNA is grounded. Although this operation also degrades the performance, the measured voltage conversion gain of 16 dB and the IIP3 of -4 dBm for the cascaded stage from the input of the LNA to the output of the final mixer agree well with the simulation, as shown in Fig. 21.

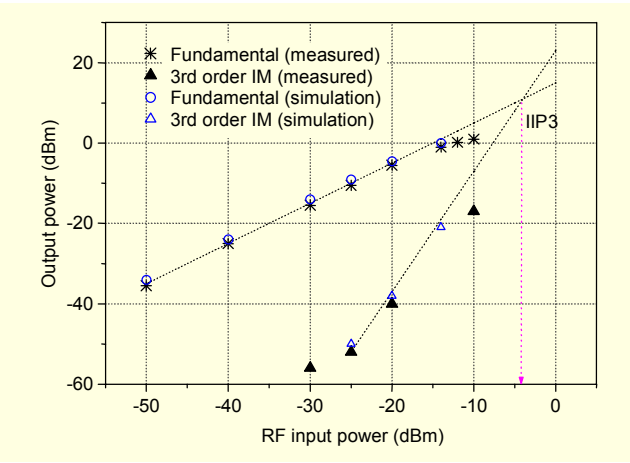

Fig. 21. Measured IIP3 of the receiver front-end.

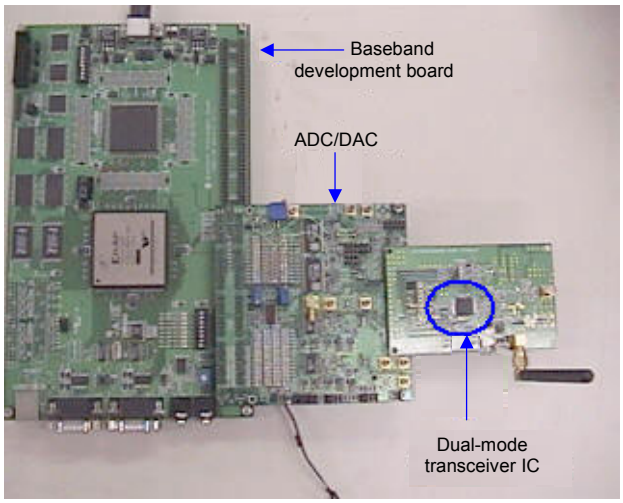

Fig. 22. File transfer test setup for 2.4-GHz high-rate Bluetooth using implemented transceiver chip.

The measured results of several building blocks such as the mixers, filters, and VGA are presented in the previous section. The complex filters for the Bluetooth mode determine the in-band adjacent channel image rejection, which is measured to be about 40 dB, as shown in Fig. 7. The measured ac response of the channel-select filter for the high-rate mode, as shown in Fig. 18, exactly meets the desired characteristics. To properly drive the first down-conversion stage and the frequency divider, an input power of about 0 dBm on the LO port is required. Thus, an off-chip matching network and LO buffers, which consume about 2 mA, are required in the implementation. We expect that the current consumption of the LO buffers can be further reduced by integrating the frequency synthesizer in the next redesign process.

The transceiver has been incorporated with the digital baseband processor to form a high-rate Bluetooth wireless system.

Table 3. Performance summary.

Parameter	T. Cho [11]		Y. Jung [12]		This design	
	BT1	802.11b	BT1	802.11b	BT1	BT2
Architecture	Dual-conv.	Dual-conv.	Direct-conv.	Direct-conv.	Dual-conv.	Dual-conv.
Filter bandwidth (3dB)	1MHz (BPF)	7.5MHz (LPF)	700kHz (LPF)	6MHz (LPF)	1.1MHz (BPF)	2MHz (LPF)
Sensitivity (dBm)	-80	-92*	-87	-86	-77	-75
IIP3 (dBm)	-12	-12	-15	-15	-5	-5
Rx active current (mA)	60	60	50	65	35	42
Technology / Vdd	0.18-μm CMOS / 1.8 V		0.25-μm CMOS / 2.7 V		0.25-μm CMOS / 2.5 V	
Die area (mm^2)	16 (including pads)		8.4 (including pads)		6.5 (without synthesizer)	
Channel select filter	Programmable		Programmable		Separate	
FSK demodulator	Not included		Not included		Included	
Freq. synthesizer	Not included		Included		Not included	
ADC	Not included		Not included		Not included (not necessary for BT1)	

Table 4. Summary of Bluetooth performance.

Specification	Measurement results	Bluetooth requirement
Frequency band	2.4–2.48 GHz	2.4–2.48 GHz
Sensitivity	-77 dBm	< -70 dBm
IIP3	> -5 dBm	> -16.5 dBm
Image rejection	40 dB	> 29 dB
Rx current drain	35 mA	Not specified
Tx current drain	32 mA	Not specified
Package	64-pin LQFP	Not specified

Table 5. Distribution of current consumption.

LNA	14 mA	BT1 & BT2
1st down converter	5.4 mA	BT1 & BT2
2nd down converter	2.5 mA	BT1 & BT2
Channel select filter	4.2 mA	BT2 Rx only
VGA	7.2 mA	BT2 Rx only
Complex channel filter	2.5 mA	BT1 Rx only
Limiter	0.42 mA	BT1 Rx only
Demodulator	1.9 mA	BT1 Rx only
Driver amplifier (DA)	14 mA	BT1 & BT2 Tx
Up converters and filters	12 mA	BT1 & BT2 Tx
Miscellaneous circuits	6 mA	BT1 & BT2

Figure 22 shows an experimental setup for the wireless file transfer test using the implemented high-rate Bluetooth chips. The initial measurement results indicate a satisfactory function of all implemented analog and digital blocks. The ADC in the digital baseband for the BT2 mode receiver shows a performance of 8-bit resolution and 40 MSPS. Successful bi-directional data transfers between the transceiver and other Bluetooth commercial modules, as well as the high-speed transfers comparable to an IEEE 802.11b-compliant Wireless LAN of 11 Mb/s, indicate the functioning of the proposed architecture. An accurate measurement of the bit error rate for the BT2 mode is not easy because the measuring equipment does not yet support an analysis of the BT2 mode signals. From a file transfer experiment using the setup shown in Fig. 22, we could estimate a bit error rate of 0.01% for the input BT2 signal power of about -75 dBm.

Table 3 presents a performance summary for this design as well as the previously published dual-mode 802.11b(WiFi)/Bluetooth radio [11], [12]. Table 4 summarizes the transceiver performance and compares it to the Bluetooth requirements. The experimental results show an IIP3 of -5 dBm and a sensitivity of -77 dBm when the losses from the external components are compensated. Table 5 shows the distribution of the current consumption.

V. Conclusion

In this paper, we presented a low-cost dual-mode concept for a CMOS system-on-chip high-rate Bluetooth solution. The dual-mode 2.4-GHz transceiver fabricated in a 0.25-μm CMOS technology meets the requirements for a data-rate of up

to 12 Mb/s as well as most of the current Bluetooth specifications. Although there is a little degradation due to parasitic components of the package and the external baluns, this degradation is easily removed by modifying the package and on-chip matching circuits in the next redesign process.

A dual-conversion using a single 1.6-GHz local oscillator architecture and a baseband dual-path architecture resolves many issues in a conventional direct-conversion or Low-IF transceiver. The flicker noise and dc offset problems, which complicate a CMOS implementation of a narrow-band receiver, are avoided by offsetting the baseband frequency and using a complex BPF. Although the dual-conversion is employed, the design requires no external image-rejection or IF channel filters. The image problem is resolved by locating the image frequency far from the desired frequency and using the band-pass characteristics of the RF filters and circuits. Furthermore, the reduced frequency of the single LO allows easier implementation of the frequency synthesizer with less power consumption and less noise. The transceiver consumes no more than 42 mA from a 2.5-V supply when the operating mode is set up to the π/4-DQPSK modulation of 8 Mb/s. This CMOS transceiver shows feasibility as a low-cost and low-power single-chip solution for a future high-rate wireless personal area network, ubiquitous network nodes and Bluetooth systems.

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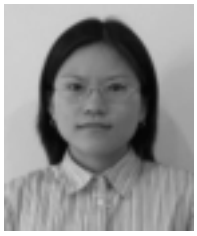
Seok-Bong Hyun received the BS, MS, and PhD degrees in physics from the Korea Advanced Institute of Science and Technology (KAIST) in 1991, 1993, and 1998, respectively. He was with the electrical engineering department, KAIST, as a Post Doctorial Research Fellow from March 1998 to June 1999. In 1999 he joined Electronics and Telecommunications Research Institute (ETRI), Korea, where he has been involved in the design of RF and analog integrated circuits for short-range wireless communication systems and Bluetooth. His research interests include the design of mixed signal IC and very high speed wireless network system.

Geum-Young Tak received the BS and MS degrees from Seoul National University, Korea, in 2000 and 2002, respectively. Since he joined ETRI in 2002, he has been involved in CMOS RF IC design for short-range wireless communication modules. His research interests include CMOS analog circuits and communication ICs.



Sun-Hee Kim received the BS and MS degrees from EWHA Womans University, Korea, in February 2000 and 2002, respectively. Since 2002, she has been with the Communication Device Module Team, ETRI, where she is a Member of Research Staff. Her research interests are in the areas of digital communication system design and VLSI.

Byung-Jo Kim received the BS degree in Electronic Engineering from Yonsei University in 1999 and the MS degree at KAIST in 2001. Since 2001, he has been with the High-speed SoC Division, ETRI, where he is a Member of Research staff. His research interests are in the area of short range wireless communication systems and advanced digital communication transceivers, especially, for WPAN (wireless personal area networks).

Jinho Ko received the BS and MS degree in electrical engineering from KAIST, Daejeon, Korea, in 1994 and 1996, respectively, where he is currently working toward the PhD degree. His doctoral research focuses on the design of a low-power CMOS RF-IC. From 1996 to 1998, he worked at SK Telecom on baseband analog circuit design. From 1999 to 2002, he was with the Havin' Co. Ltd. He founded PHYCHIPS Inc., Daejeon, Korea in 2002.

Seong-Su Park received the BS degrees in metallurgy from Yonsei University, Korea, in 1984, and the MS and PhD degrees in materials science from KAIST, Korea, in 1986 and 1992, respectively. In 1993, he joined ETRI, Korea, where he is now a Team Manager. Until 1998, his research area was MMICs and high speed optical devices packaging such as 5GHz amplifier module, 10Gbps laser diode module, etc. Since 1999, he has been in charge of development of Bluetooth chips.