Thermal Characteristics of a Laser Diode Integrated on a Silica-Terraced PLC Platform

Duk-Jun Kim, Young-Tak Han, Yoon-Jung Park, Sang-Ho Park,
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ABSTRACT—A spot-size converted Fabry-Perot laser diode (LD) was flip-chip bonded to a silica-terraced planar lightwave circuit (PLC) platform to examine the effect of the silica terrace on the heat dissipation of the LD module. From the measurement of the light-current characteristics, it was discovered that the silica terrace itself is not a strong thermal barrier, but the encapsulation of the integrated LD with an index-matching polymer resin more or less deteriorates the heat dissipation.

Keywords—Hybrid integration, silica terrace, PLC platform, heat dissipation.

I. Introduction

Hybrid integration of semiconductor optoelectronic devices on a planar lightwave circuit (PLC) platform by passive alignment has long been paid attention to because of its potential for reducing the fabrication cost of the optical transceiver modules for a subscriber network [1]. Generally, the heat-generating laser diodes (LDs) are flip-chip bonded to the PLC platforms with the highly thermal-conductive silicon terraces, and the dielectric passivation film on the terraces is thin enough not to prevent the heat flow from the LD. However, this thin dielectric film frequently causes the restriction of the operational bandwidth of the LD modules since the parasitic capacitance between the silicon terrace and the electrical wiring including metal solders and electrodes is not so small [2]. It seems that the introduction of a silica terrace instead of silicon one is an easy way to decrease the parasitic capacitance, but the report relevant to the silica terrace is rare in the literature, which is probably for fear of the heat dissipation problem. In this work, a spot-size converted (SSC) Fabry-Perot LD was integrated with a silica-terraced PLC platform, and the high temperature characteristics of the LD module were examined together with the effect of the polymer resin encapsulation over the LD.

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II. Fabrication and Results

Figure 1(a) shows our PLC platform structure in which the LD chip is mounted on silica terraces. The fabrication of the platform begins with the formation of the silica PLC on a 1 mm thick silicon substrate, and ends with the patterning of a Au-Sn solder and Cr-Ni-Au electrode, or under bump metallurgy, after applying our unique two-step etching technique [3] for the silica terrace. The PLC was made from the conventional flame hydrolysis deposition process. The relative refractive index difference between the silica waveguide core and cladding, the core size, and the thickness of the under-cladding were designed to be 1.5%, 4.5 μm × 4.5 μm, and 15 μm, respectively.

The first step to realize the silica terraces is to form a silica trench by etching only the LD-mounting region out of the silica film down below the core. The second step is to additionally etch the region other than the terraces in the trench to make room for the solders. As the etching depth is critical to the vertical alignment and bonding of the LD, we carefully controlled the reactive ion etching process after confirming the PLC and LD dimensional parameters. As it appears in Fig. 1(b), the top view of the PLC platform, there exist fifteen circular solders with the diameter of 70 or 80 μm at the region

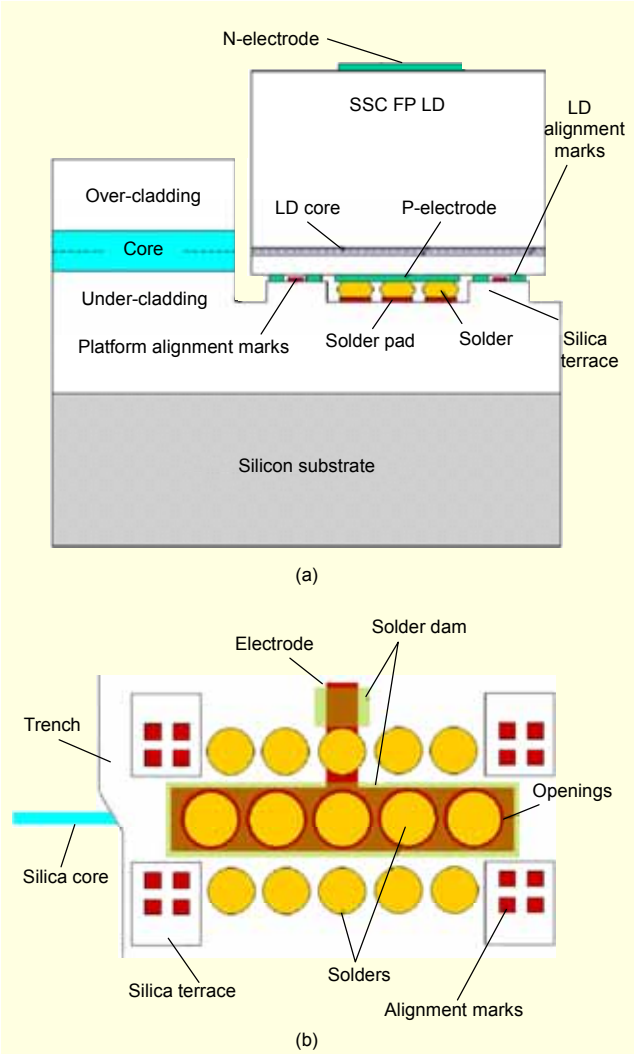

Fig. 1. Schematic (a) cross-sectional and (b) top views of the silica-terraced PLC platform.

surrounded with four rectangular terraces in three rows. To maximize the heat dissipation through the solders, the solder area was increased while the terrace area was decreased as much as possible. The number, size, thickness, and configuration of the solders were chosen in consideration of bonding strength as well as heat dissipation. Additionally, the etched facet of the straight silica waveguide, which is 20 μm apart from the flip-chip bonded LD, was 45° angled to the axis of the LD waveguide to divert the light reflected from the facet. A detailed description of our silica-terraced platform was given elsewhere [3].

The LD chip used in this work is the 1310 nm InGaAsP/InP LD with a laterally tapered SSC section and has the dimension of 600 μm (L) × 300 μm (W) × 120 μm (H) [4]. The divergence angles are about 10° and 13° in the horizontal and vertical directions, respectively. The optical coupling loss between the LD and PLC waveguides is calculated to be about 1.5 dB when the refractive index of the optical path is matched to 1.5 at the wavelength. Figure 2 shows the output characteristics of the LD, which were obtained at the heat-sink temperatures of 25°C and 85°C under continuous-wave operation. For 25°C, above the threshold current of 8 mA, the output power almost linearly increases with a rate of 0.27 mW/mA. For 85°C, such linearity is maintained at the low injection current region just above the threshold current of 30 mA, but the increasing rate gradually decreases with the increase of the current. This gradual decrease in the slope efficiency is due to the LD temperature rise arising from the insufficient heat dissipation.

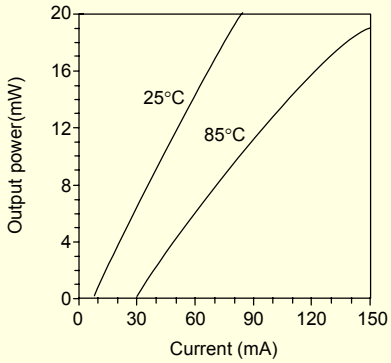

Fig. 2. Light-current characteristics of the bare LD chip.

Table 1. Thermal conductivity of the materials involved in the LD module fabrication.

Material	Conductivity (W/m.K)
InP	68
GaAs	44
Au-Sn (eutectic)	250
SiO_2	1.4
Si	168
FR4 (PCB)	0.23
Acrylate resin	0.19

As shown in Table 1, the eutectic Au-Sn and silica have the largest and smallest thermal conductivity values among the materials used, respectively, excepting the acrylate resin for the polymer encapsulation and the FR4 for the printed circuit board. So, the maximization of the solder area is desirable for the heat transfer from the LD through the silica terrace film with a fixed thickness. Thermal analysis based on the finite element method was conducted to estimate the heat dissipation capability of our platform structure in which the 3 μm thick

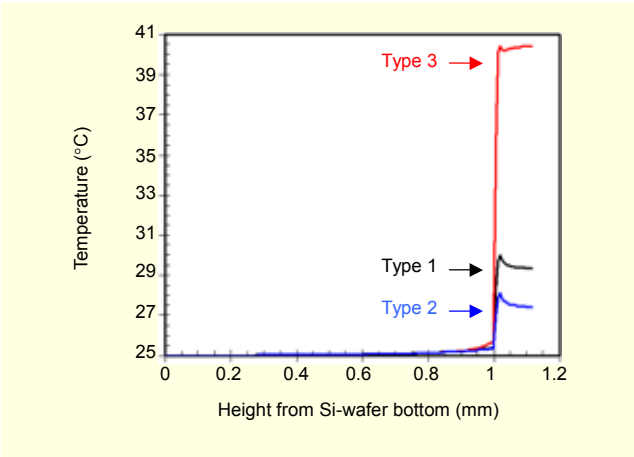

Fig. 3. Thermal analysis result for the silica-terraced PLC platform.

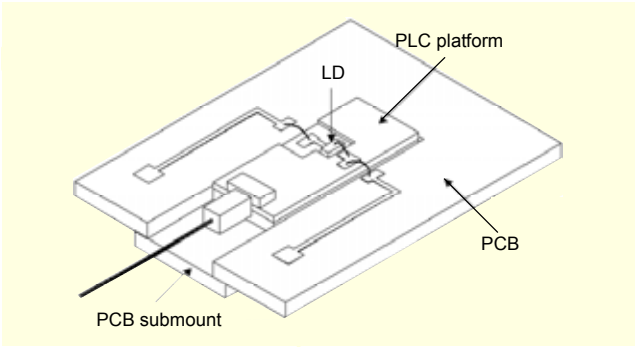

Fig. 4. Schematic diagram of the LD module.

solders occupy the area of 64,000 μm^2 (type 1). The analysis was also conducted for the extreme case where only one solder with the same thickness is applied, but its area is as large as 180,000 μm^2 (type 2), which corresponds to the LD size, or as small as 10,000 μm^2 (type 3). The results under the constant heat generation of 50 mW are presented in Fig. 3. As expected, the type 2 and 3 solders produced the smallest and largest LD temperatures, respectively. And the temperature difference between them is as much as 13°C. For the type 1 solder, the temperature rise is about 4.5°C; that is 2°C higher than that for the type 2 solder. The LD temperature difference between the type 1 and 2 solders is not so much in spite of the very large difference in solder area, which implies that the underlying silica film or trench, rather than the metal solders, more governs the heat flow from the LD to the silicon substrate as the solder area approaches the LD size. The temperature rise of 4.5°C is a little higher compared with that for the general silicon-terraced platform [2]. It is considered that the thinning of the silica under-cladding up to the thickness permitted for the respect of the parasitic capacitance and optical/electrical wave propagation loss will help to reduce the temperature rise [2], [5].

The above mentioned LD was flip-chip bonded to the silica-terraced PLC platform 18 mm × 8 mm in size, and the platform was then mounted on a printed circuit board (PCB), as shown in the schematic diagram of Fig. 4, in order to measure the light-current characteristics of the integrated LD in a temperature-controllable chamber. This measurement was first performed in the absence of the index-matching substances between the LD and PLC waveguide facet, and repeated after encapsulating the LD with a UV-curable acrylate resin (OA9352HT; Luvantix, Korea), which is generally used for joining the optical paths and fixing in optical devices. It is known that the refractive index of the cured resin is 1.48 at 1550 nm and the thermo-optic coefficient of such acrylate resin ranges in value from -1.6×10^{-4}/°C to -2.3×10^{-4}/°C [6]. As known from the data for the first measurement in Fig. 5(a), the output power is extremely small compared with that for the bare LD irrespective of the temperature, which is due to the angled silica waveguide facet of Fig. 1(b), while the threshold current and the output power behavior to the injection current are nearly the same although the slope efficiency for 85°C starts to decrease at the lower current. This implies that the silica film under the LD is not a strong barrier to the heat flow. The encapsulation makes the resin come to fill the gap between the LD and silica waveguide facets. As a result, the optical coupling between the LD and silica waveguides enhances, as seen in Fig. 5(b). Nevertheless, the power level is still over three times lower than that for the bare LD chip.

Comparing the two 25°C data of Figs. 5(a) and 5(b), we can see that the power linearity of the latter is not as good as that of the former. Moreover, such a deviation from linearity exists even for the very low temperature of –30°C and enlarges accompanying the threshold current increase as it goes to 85°C. From the data of 25°C and 85°C, we can also see that the encapsulation changes the threshold current values that are initially 8 mA and 31 mA to 10 mA and 37 mA, respectively. This threshold current increase might be explained with a change in the reflectivity of the LD facet. The reflectivity value at the low reflectivity side was designed as 30% but comes to be reduced to about 15% by the contact of the facet with the resin. Generally, such reflectivity decrease gives rise to the improvement of the LD slope efficiency without worsening the output power linearity [7]. In this regard, it is thought that the power non-linearity is due to the insufficient heat dissipation caused by the resin encapsulation. On the other hand, it is hard to explain why the output power level is three times lower than the bare LD chip only with the heat dissipation because the power level for the injection current regions where the power linearity is well maintained is similarly low. It is believed that the LD misalignment during the flip-chip bonding is the main cause of the low output power level.

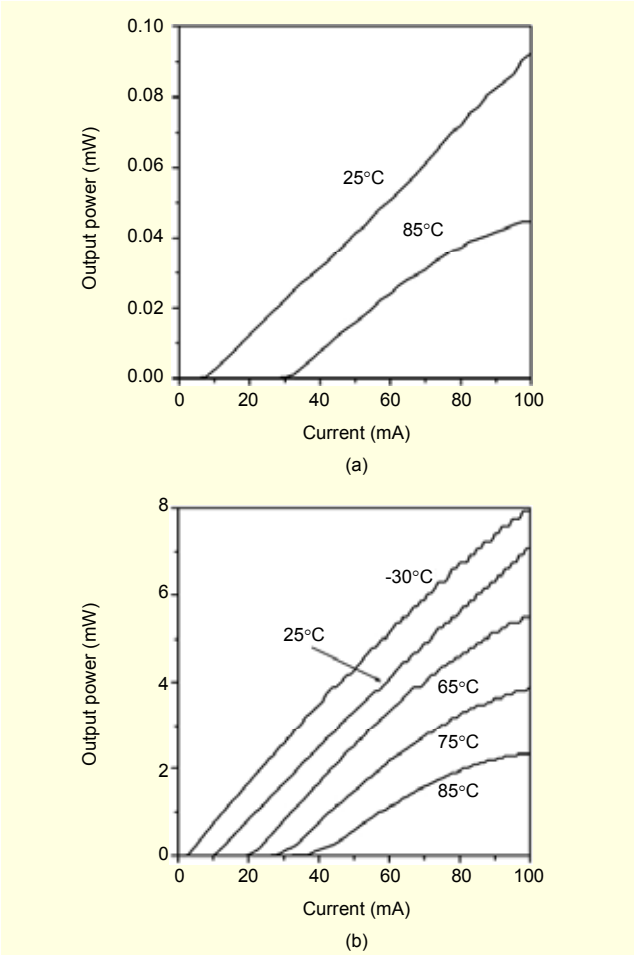

Fig. 5. Light-current characteristics of the LD module (a) before and (b) after the resin encapsulation.

III. Conclusion

From the above investigation, it is concluded that the silica-terraced platform itself has the capability to dissipate the heat generated from the integrated LD, which is acceptable for the low power transceiver modules, but the capability is more or less reduced by the resin encapsulation. For the cost-effective plastic packaging of the modules, it will be helpful to apply the transparent index-matching resin only to the small region encompassing the optical path of the LD and a special resin with the higher thermal conductivity to the other region. In addition, the replacement of the PCB submount for the PLC platform with a metal one will improve the thermal characteristics of the LD modules.

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