

# Monolithic SiGe Up-/Down-Conversion Mixers with Active Baluns

Sang-Heung Lee, Seung-Yun Lee, Hyun-Cheol Bae, Ja-Yol Lee, Sang-Hoon Kim, Bo Woo Kim, and Jin-Yeong Kang

The purpose of this paper is to describe the implementation of monolithically matching circuits, interface circuits, and RF core circuits to the same substrate. We designed and fabricated on-chip 1 to 6 GHz up-conversion and 1 to 8 GHz down-conversion mixers using a 0.8  $\mu\text{m}$  SiGe hetero-junction bipolar transistor (HBT) process technology. To fabricate a SiGe HBT, we used a reduced pressure chemical vapor deposition (RPCVD) system to grow a base epitaxial layer, and we adopted local oxidation of silicon (LOCOS) isolation to separate the device terminals. An up-conversion mixer was implemented on-chip using an intermediate frequency (IF) matching circuit, local oscillator (LO)/radio frequency (RF) wideband matching circuits, LO/IF input balun circuits, and an RF output balun circuit. The measured results of the fabricated up-conversion mixer show a positive power conversion gain from 1 to 6 GHz and a bandwidth of about 4.5 GHz. Also, the down-conversion mixer was implemented on-chip using LO/RF wideband matching circuits, LO/RF input balun circuits, and an IF output balun circuit. The measured results of the fabricated down-conversion mixer show a positive power conversion gain from 1 to 8 GHz and a bandwidth of about 4.5 GHz.

**Keywords:** SiGe, HBT, mixer, active balun.

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## I. Introduction

The rapid growth of wireless communication services has now been extended to higher frequencies and is creating an increasing demand for low-cost, low-power, and high-integration RF sub-systems in different types of communication systems.

The SiGe hetero-junction bipolar transistor (HBT) has been considered to be more suitable for RF integrated circuits than the Si bipolar junction transistor (BJT) because its electrical properties, such as current gain, power consumption, and small-signal unity-gain frequency are superior to those of the Si BJT. SiGe HBTs are playing a greater role in a variety of applications such as RF integrated chips, networking chips, and so on [1]-[6].

Up-conversion mixers, which convert an intermediate frequency (IF) signal to a radio frequency (RF) signal, and down-conversion mixers, which convert an RF signal to an IF signal, are very important building blocks within a radio system. Their performance affects the performance requirements of the entire system as well as the performance requirements of other building blocks [7]. Also, for a monolithic microwave integrated circuit (MMIC), it is necessary that the balun and matching circuits are integrated on an RF chip [8]. The balun, which converts a single-ended signal into balanced signals, or balanced signals into a single-ended signal, has been used to match the source and amplifier circuits. The balun can be divided into active, transmission-line, and passive types. The baluns of transmission-line and passive types are not adequate to an MMIC circuit because they require a large area. They also cannot be applied to a wideband MMIC circuit because the length of a passive device according to the changing of frequency cannot be tunable. However, an active

balun can obtain signal gain and can be applied to a wideband MMIC circuit because the balun can change phases between  $0^\circ$  and  $180^\circ$  despite the changing of frequency.

The purpose of this paper is to describe the implementation of monolithically matching circuits, interface circuits, and RF core circuits to the same substrate. In this paper, a 1 to 6 GHz up-conversion mixer including an IF matching circuit, local oscillator (LO)/RF wideband matching circuits, LO/IF input balun circuits, and an RF output balun circuit for a wireless communication system is designed and fabricated on-chip, using the ETRI SiGe HBT process technology. Also, a 1 to 8 GHz down-conversion mixer including LO/RF wideband matching circuits, LO/RF input balun circuits, and an IF output balun circuit is designed and fabricated on-chip.

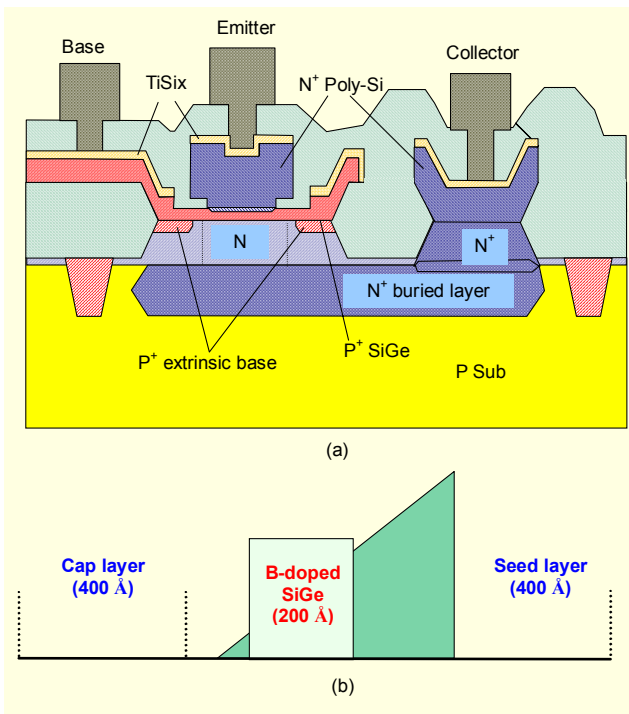


Fig. 1. (a) Schematic of a fabricated SiGe HBT, and (b) the standard base profile used.

## II. Characteristics of SiGe HBT and Passive Elements

Performance parameters of a SiGe HBT such as cut-off frequency ( $f_T$ ), maximum oscillation frequency ( $f_{max}$ ), and minimum noise figure ( $NF_{min}$ ), decisively depend on the base structure as well as on the fabrication process [9]. In general, an ultra-high-vacuum chemical vapor deposition (UHV-CVD) process has been adopted for SiGe research because of purity-assisted improvements in the device characteristics. However, the low throughput and high cost of UHV-CVD has become a barrier from an industrial point of view, giving a chance to use

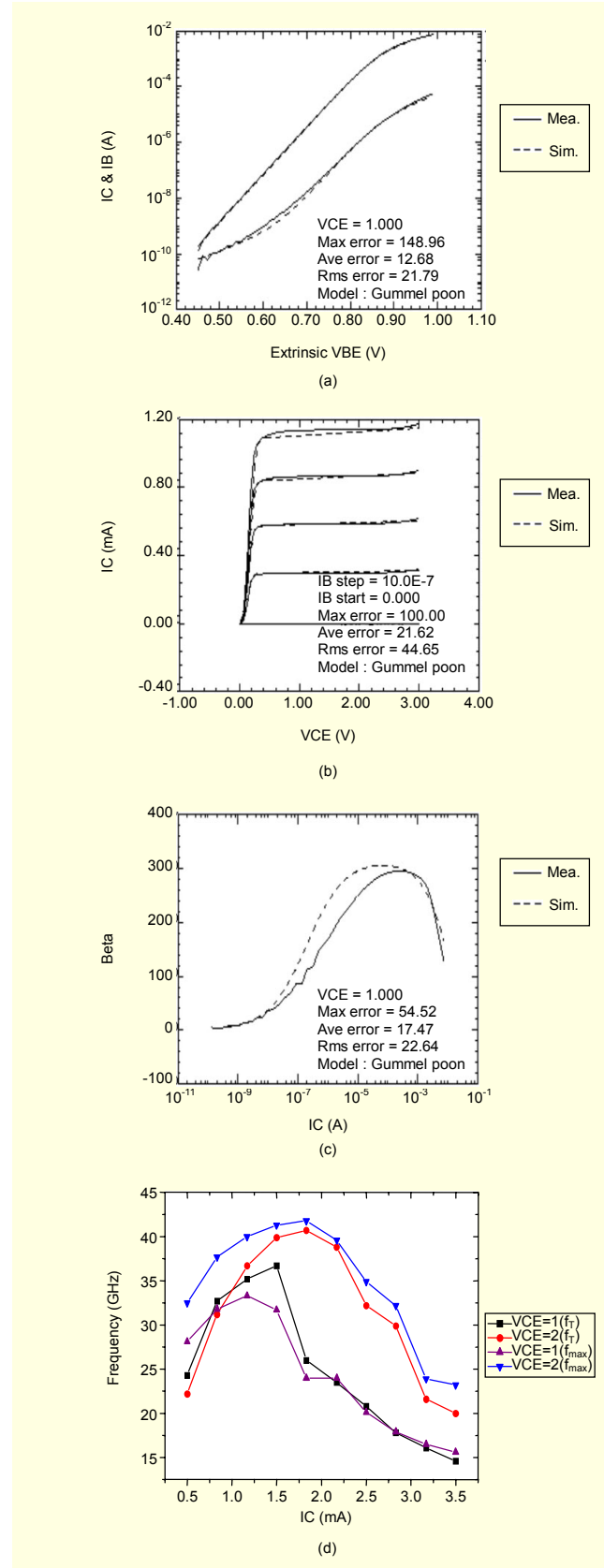


Fig. 2. (a) Gummel plot, (b) I-V characteristics, (c) DC current gain, and (d)  $f_T$  and  $f_{max}$ , with  $A_E=0.5 \times 6.0 \mu m^2$ .

Table 1. SiGe HBT DC and AC characteristics.

Emitter area ( $\mu\text{m}^2$ )	0.5 × 6.0
DC current gain	296
BVEBO (V)	0.95
BVCBO (V)	10.7
BVCEO (V)	3.5
RC ( $\Omega$ )	61
RE ( $\Omega$ )	30
$f_T$ (GHz)	41
$f_{\text{max}}$ (GHz)	42

reduced-pressure CVD (RPCVD) as an alternative. It is also well known that the base structure features of SiGe HBTs, such as the thickness and Ge profile, influence the device characteristics to a great extent [10].

We used the RPCVD system to grow a base epitaxial layer and adopted local oxidation of silicon (LOCOS) isolation to separate the device and device terminals. A standard SiGe HBT is shown in Fig. 1(a) [8]. The thickness of the collector was 8000 Å on the thick and highly doped sub-collector. A standard base profile is shown in Fig. 1(b). In the standard base profile, the total Ge thickness was 400 Å with a 200 Å rectangular layer of Boron. The base growth was followed by Ti-silicidation ( $\text{C54-TiSi}_2$ ), which is critical to the extrinsic base resistance between the base terminal and the intrinsic base-emitter junction. The  $\text{C54-TiSi}_2$  was obtained using a rapid thermal anneal at 850 °C for 30 seconds with no harm to the base profile. The maximum  $f_T$  and  $f_{\text{max}}$  values of a SiGe HBT with a  $0.5 \times 6.0 \mu\text{m}^2$  emitter area were 41 and 42 GHz at  $V_{\text{CE}} = 2\text{V}$  and  $I_{\text{C}} = 1.83 \text{mA}$ , respectively, as shown in Fig. 2(d). The measured DC and AC parameters of a SiGe HBT with a  $0.5 \times 6.0 \mu\text{m}^2$  emitter area were summarized in Table 1. In addition, passive elements used for MMIC were an MIM (metal-insulator-metal) capacitor with a 75 nm thickness of isolator  $\text{SiO}_x\text{Ny}$ , parallel-branch spiral inductor, and resistors composed of metal, emitter poly-silicon, and base poly-silicon. In particular, a parallel-branch inductor implemented by branching the inductor in parallel with the same direction [11] brings on a reduction of the series resistance and an addition of inductance and parasitic capacitance. Finally, the frequency of the peak quality factor ( $f_{\text{Qmax}}$ ) of the inductor is possible to be tuned, and a higher quality factor can be obtained.

### III. Monolithic SiGe Mixer Design

The chip architectures of an up-conversion mixer and down-conversion mixer are shown in Fig. 3. The blocks consist of

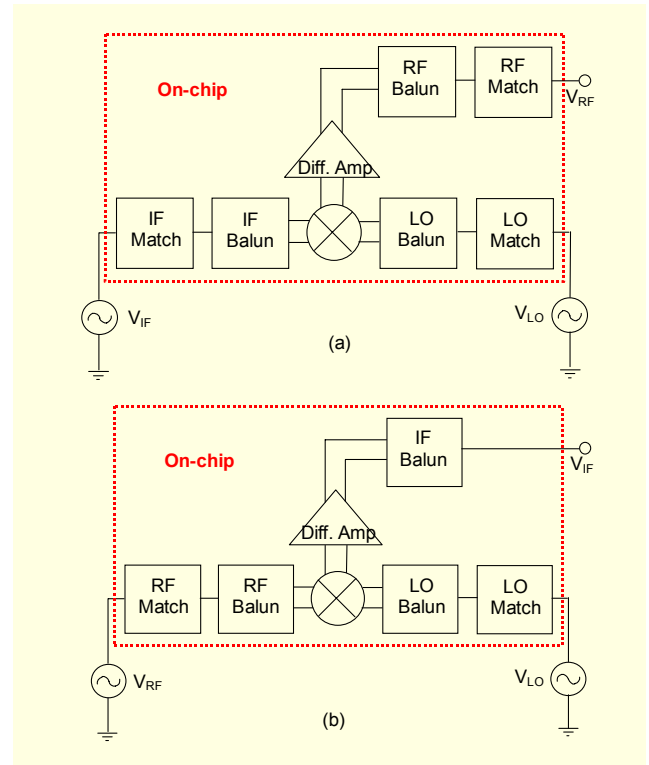


Fig. 3. Architectures of (a) 1 to 6 GHz up-conversion mixer and (b) 1 to 8 GHz down-conversion mixer.

input and output matching circuits, baluns, and a Gilbert cell mixer [8]. A single-ended IF (RF for down-conversion mixer) and LO input signals enter into the mixer, and a single-ended output signal RF (IF for down-conversion mixer) goes out of the mixer. The single-ended IF input (RF input for down-conversion mixer) and single-ended LO input are converted differentially in order to feed into the double balanced mixer by use of on-chip active baluns. At the front of the LO input balun of Fig. 3(a) and the RF and LO input baluns of Fig. 3(b), a wideband matching circuit for  $50 \Omega$  is inserted in order to operate in favor of a wide frequency, which consists of on-chip passive elements.

Figure 4 shows a single-input, balanced-output differential balun, which is used as IF and LO input baluns for the up-conversion mixer (RF and LO input baluns for down-conversion mixer). In particular, this active differential balun offers a high rejection of supply noise and high output swing. In Fig. 4, the single input is applied to the base of transistor Q1, and the output is measured between the two collectors, which are at the same DC potential. The AC signal gain of the balun is determined by transconductances of Q1, Q2, the degeneration inductors L1, L2, and the output resistors R1, R2. The emitter inductive degeneration (L1, L2) reduces the AC signal gain of the input balun, but is used to improve linearity. The capacitor C1 separates DC bias from the ground. Figure 5

shows a push-pull balun composed of both a common-emitter with degeneration and a common-collector, which is used as the RF output balun for the up-conversion mixer (IF output balun for down-conversion mixer). The degeneration resistor R3 controls the gain of the common emitter path for the same amount of gain for both inverting and non-inverting signals, resulting in maximum cancellation of LO leakage at the output of the balun. Resistor R4 is included for 50  $\Omega$  RF output impedance matching (IF output impedance matching for down-conversion mixer). The signal gain of a balun is the sum of the two signal path gains [12]. These on-chip active baluns were designed and integrated together with this mixer core circuit and provide good isolation.

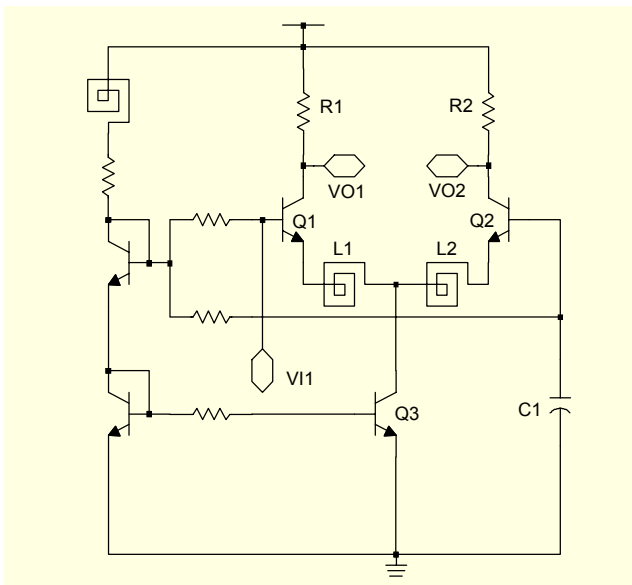


Fig. 4. Input balun with bias circuit.

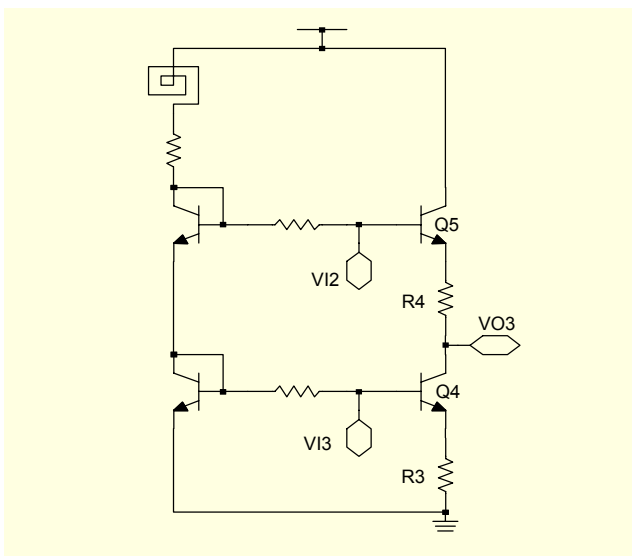


Fig. 5. Output balun with bias circuit.

The frequency conversion function necessary in virtually all receivers and transmitters is commonly implemented by a double-balanced mixer. A double-balanced bipolar mixer in the form of a Gilbert cell used in the mixer design, as shown in Fig. 6, which is a differential structure to avoid the common-mode noise, provides sufficient suppression. The mixers of Figs. 6(a) and 6(b) are for up-conversion and down-conversion, respectively. The higher the output impedance of the current source shown in Fig. 6 is, the better the LO suppression. When the switching transistors of the Gilbert cell mixer are driven fully differentially from each of the LO and IF input baluns (LO and RF input baluns for down-conversion mixer), theoretically there is no LO leakage at the output. Emitter inductive degeneration (L3, L4 with 1 nH) is also added to improve linearity, though these inductors degrade AC signal gain. By means of the emitter inductor (L3, L4), a reduction in transconductance would lower the mixer's conversion gain, but raise the third-order intercept level due to the lower distortion and increased signal capacity. Inductors L5 and L6 for the up-

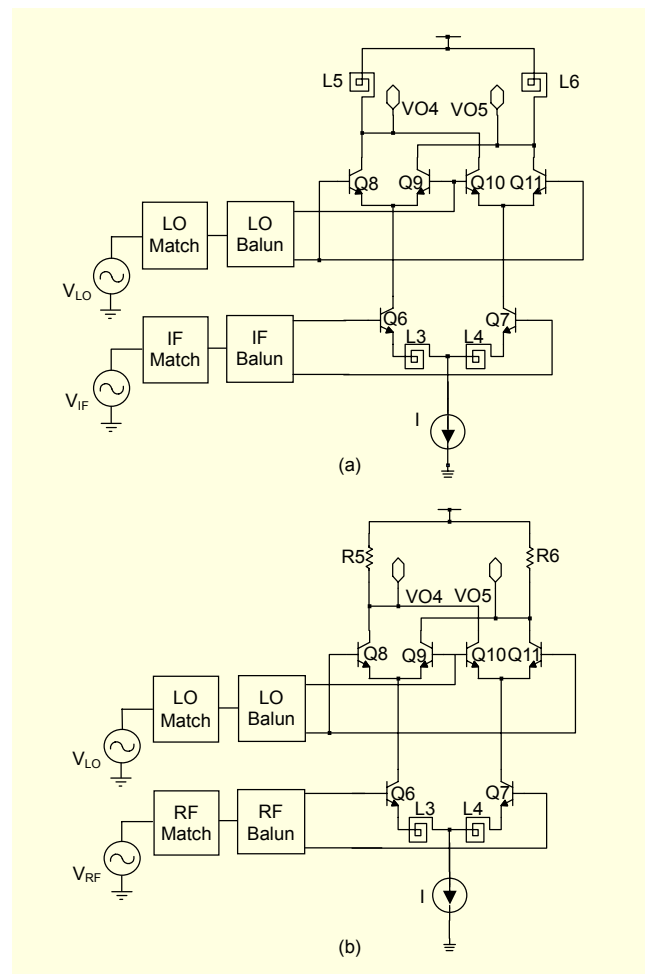


Fig. 6. Circuits of (a) up-conversion mixer and (b) down-conversion mixer.

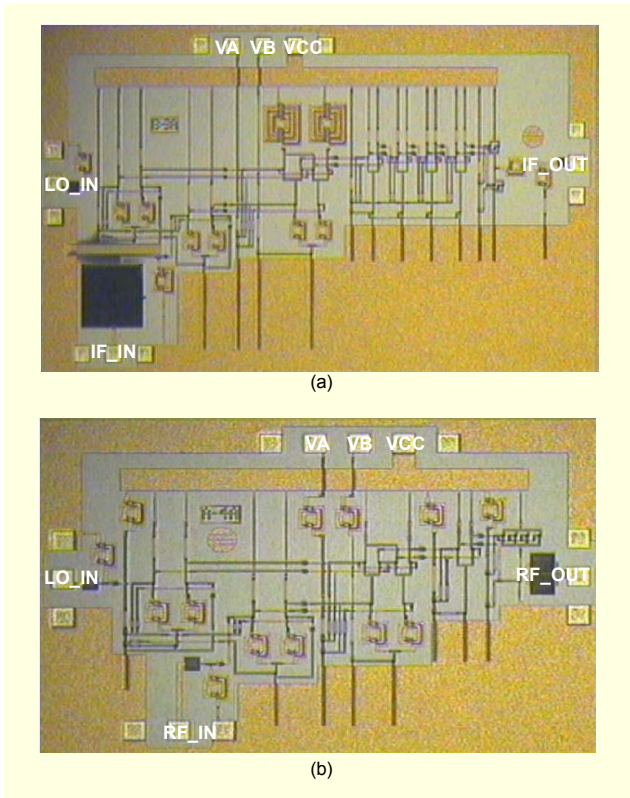


Fig. 7. Microphotographs of the fabricated mixer: (a) up-conversion mixer and (b) down-conversion mixer.

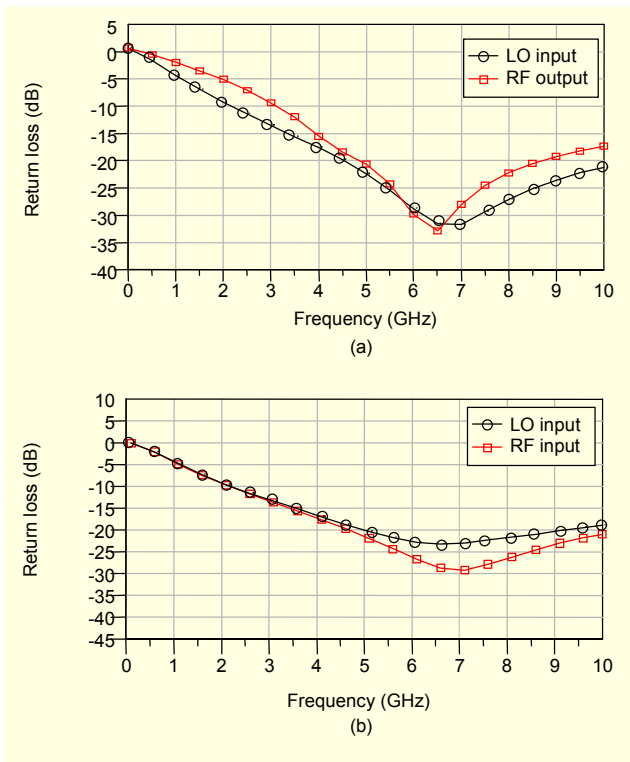


Fig. 8. Matching characteristics of the fabricated mixer: (a) up-conversion mixer and (b) down-conversion mixer.

conversion mixer shown in Fig. 6(a) are used for the collector loads in order to get enough voltage headroom for high linearity.

#### IV. Fabrication and Measurements

We designed and fabricated a 1 to 6 GHz MMIC up-conversion mixer and 1 to 8 GHz MMIC down-conversion mixer using a 0.8  $\mu\text{m}$  SiGe HBT process. Photographs of the manufactured mixers are shown in Fig. 7. The chip sizes of the up-conversion mixer and down-conversion mixer are 2.7 mm  $\times$  1.6 mm, shown in Fig. 7(a), and 1.9 mm  $\times$  1.3 mm,

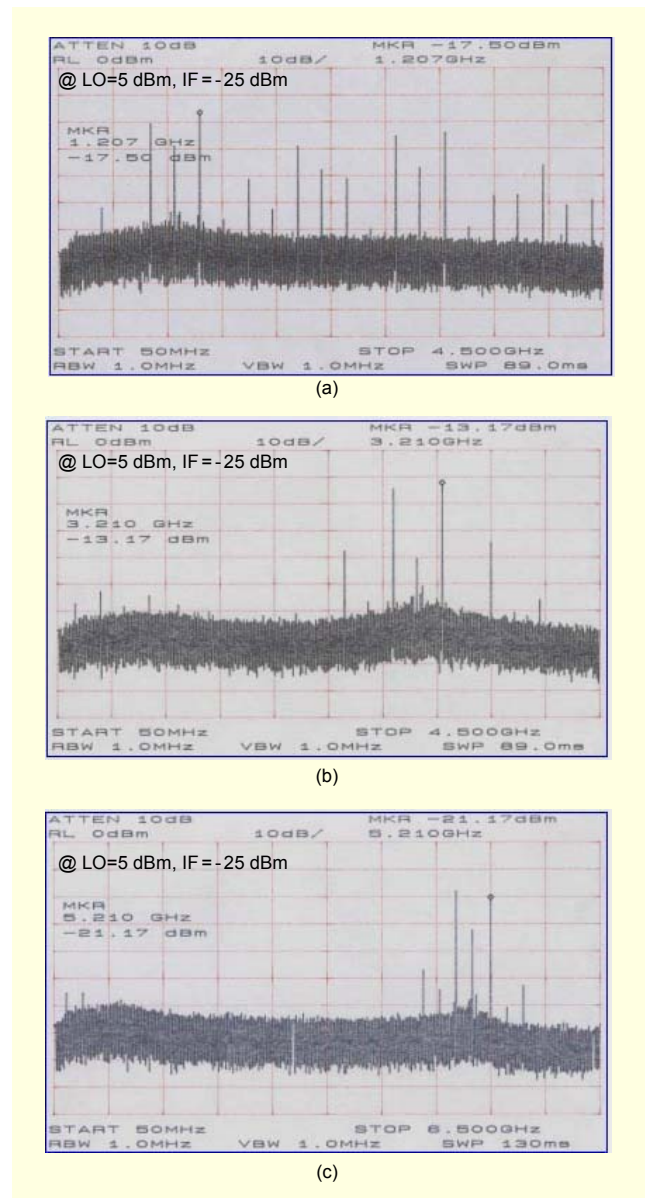


Fig. 9. Frequency spectrum measured at the RF output port of the fabricated mixer when LO input frequencies were (a) 1.0 GHz, (b) 3.0 GHz, and (c) 5.0 GHz for up-conversion mixer.

shown in Fig. 7(b), respectively. In Figs. 7(a) and 7(b), the upper pads are for the supply voltage. In Fig. 7(a), the left, lower, and right center pads are LO input, IF input, and RF output pads, respectively, and in Fig. 7(b), the left, lower, and right center pads are LO input, RF input, and IF output pads, respectively.

For this measurement, two RF power sources HP83650B, HP83752B, and a spectrum analyzer HP8563E were used. Figures 8(a) and 8(b) show return losses measured at the LO input and RF output ports for the up-conversion mixer, and at the

LO input and RF input ports for the down-conversion mixer, respectively.

Figure 9 shows a frequency spectrum measured at the RF output port for a fixed 200 MHz IF input frequency and LO input frequencies of 1.0, 3.0, and 5.0 GHz, when the measured conditions of the fabricated up-conversion mixer were IF=-25 dBm, LO=5.0 dBm, and VCC=3.0 V. Figure 10 shows the measured 3rd-order intercept point characteristics swept according to IF input power from -25 to 0 dBm when the fixed

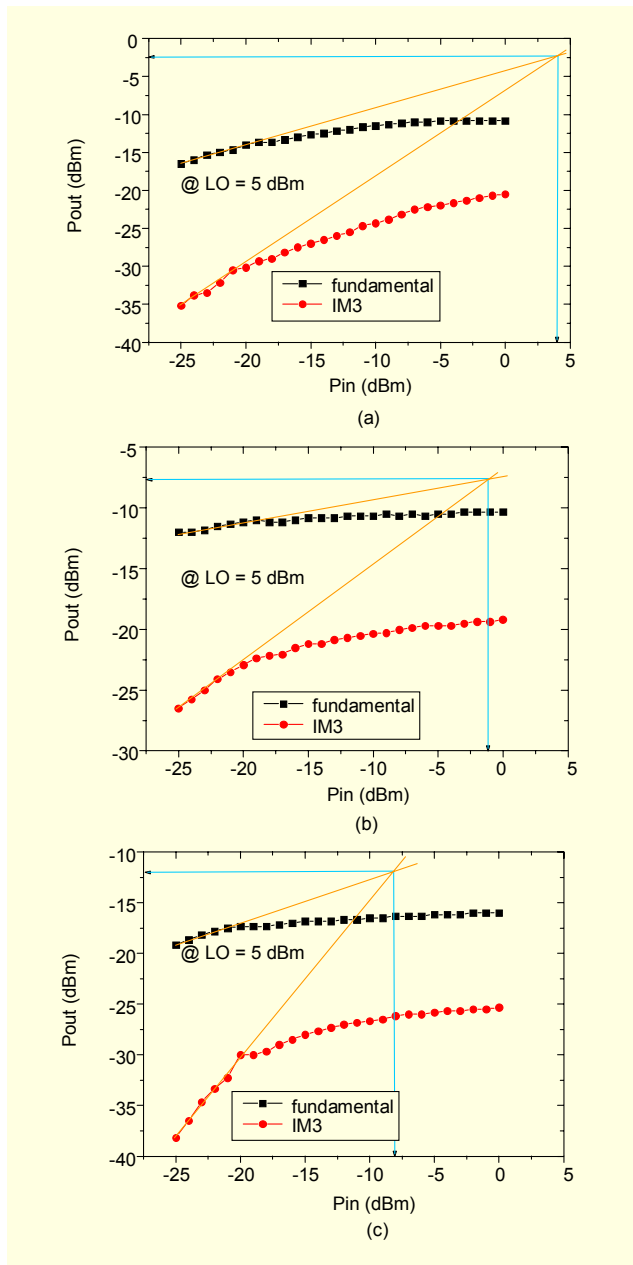


Fig. 10. Measured 3rd order intercept point characteristics when IF input frequency was 200 MHz and LO input frequencies were (a) 1.0 GHz, (b) 3.0 GHz, and (c) 5.0 GHz for the up-conversion mixer.

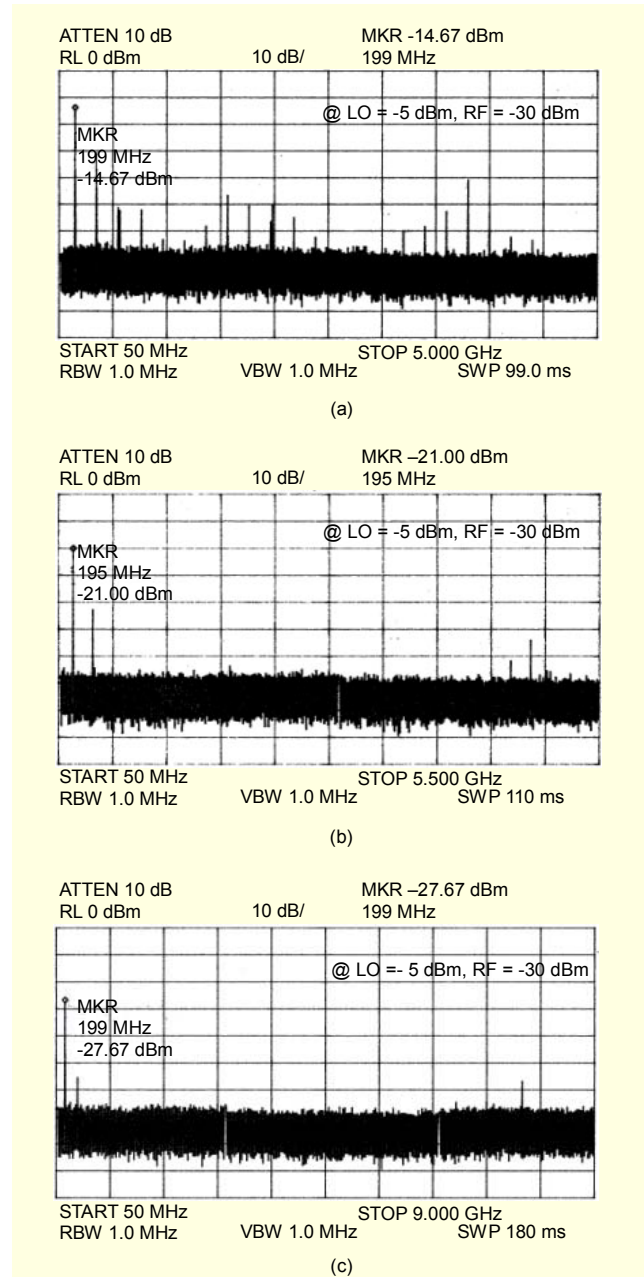


Fig. 11. Frequency spectrum measured at the IF output port of the fabricated mixer when RF input frequencies were (a) 2.0, (b) 5.0, and (c) 8.0 GHz for the down-conversion mixer.

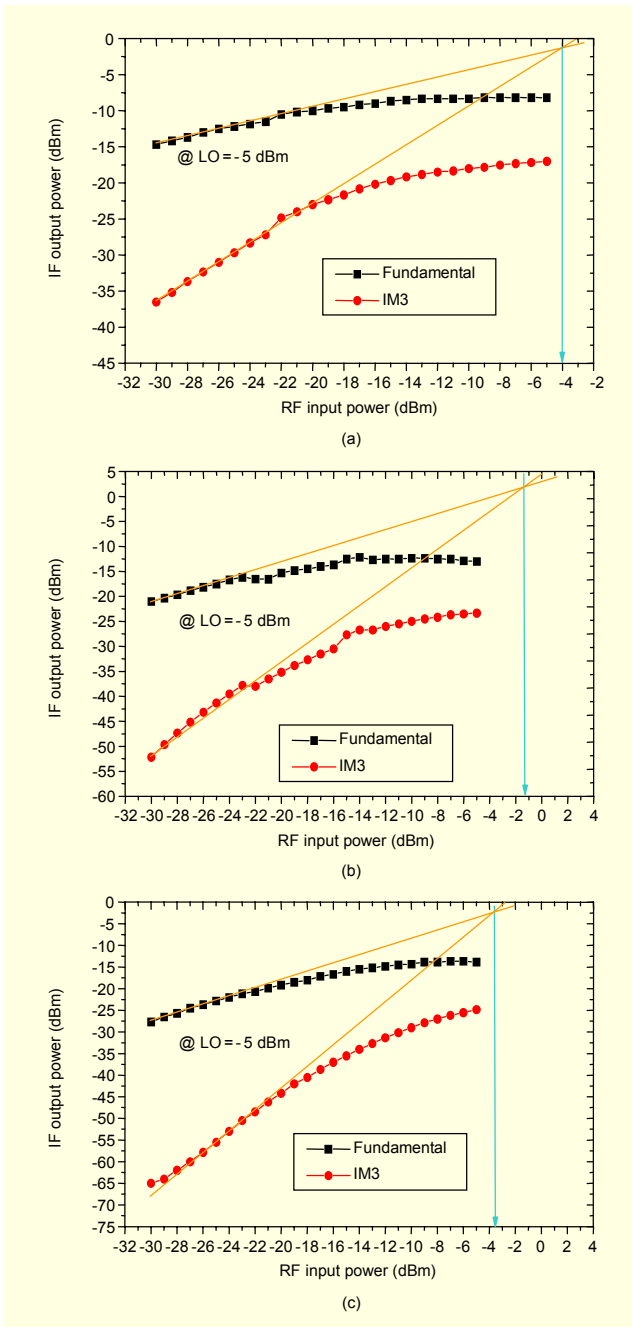


Fig. 12. Measured 3rd-order intercept point characteristics when RF input frequencies were (a) 2.0, (b) 5.0, and (c) 8.0 GHz for the down-conversion mixer.

IF input frequency was 200 MHz and LO input frequencies were 1.0, 3.0, and 5.0 GHz.

Figure 11 shows a frequency spectrum measured at the IF output port with a fixed 200 MHz, as an example, for RF input frequencies of 2.0, 5.0, and 8.0 GHz, when the measured conditions of the fabricated down-conversion mixer were RF=-30 dBm, LO=-5.0 dBm, and VCC=3.0 V (with local biases of  $V_A = 3.0$  and  $V_B = 2.5$ ). Figure 12 shows the

measured 3rd-order intercept point characteristics swept according to RF input power from -30 to -5 dBm, when the RF input frequencies were 2.0, 5.0, and 8.0 GHz.

Figure 13 shows the measured power conversion gain and output 3rd-order intercept point (OIP3), when LO input power was 5 dBm, IF frequency was fixed at 200 MHz, and LO input frequencies were swept in the range of 1 to 6 GHz for the up-conversion mixer. Figure 14 shows the LO to IF isolation and LO to RF isolation according to LO input frequencies when LO input power was 5 dBm, IF input power was -25 dBm, and IF frequency was fixed at 200 MHz for the up-conversion mixer. From Figs. 13 and 14, the measured results showed a positive power conversion gain from 1 to 6 GHz, a bandwidth of about 4.5 GHz, LO isolation (LO to RF isolation and LO to IF isolation) between 27 and 45 dB, and OIP3 between -2 and -12 dBm. The measured up-conversion mixer consumed a current of 29 mA for a 3 V supply voltage.

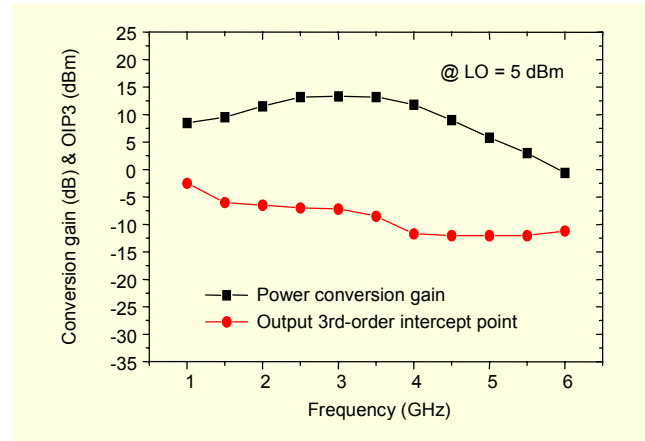


Fig. 13. Measured power conversion gain and output 3rd order intercept point when LO input frequencies were swept in the range of 1 to 6 GHz for the up-conversion mixer.

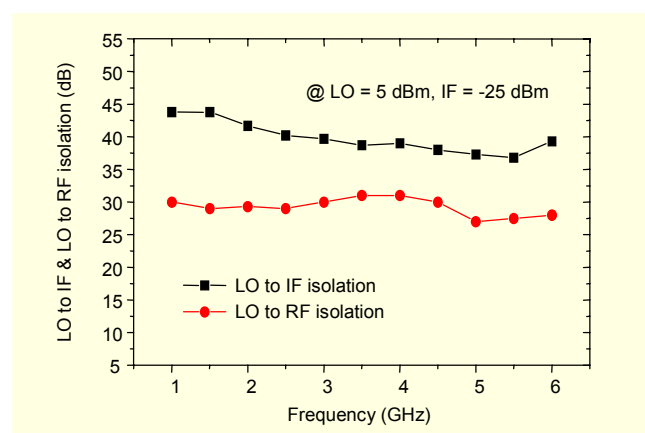


Fig. 14. Measured LO to IF isolation and LO to RF isolation characteristics when LO input frequencies were swept in the range of 1 to 6 GHz for the up-conversion mixer.

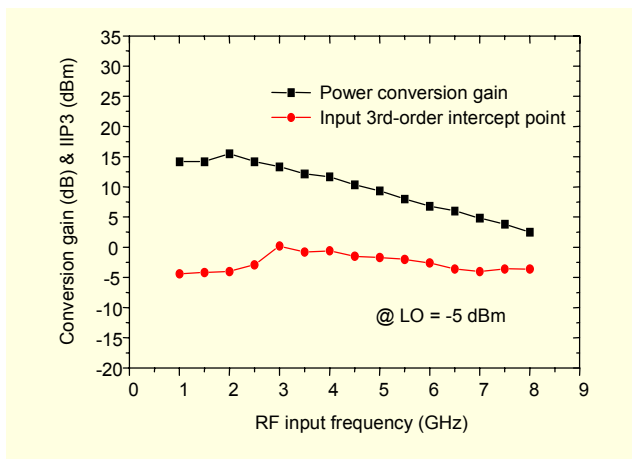


Fig. 15. Measured power conversion gain and input 3rd order intercept point when RF input frequencies were swept in the range of 1 to 8 GHz for the down-conversion mixer.

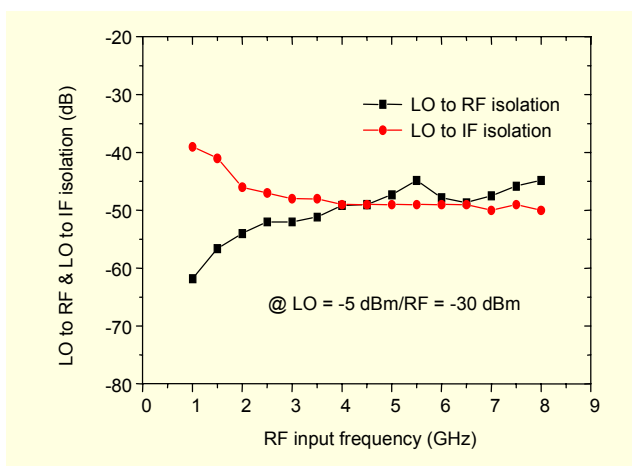


Fig. 16. Measured LO to RF isolation and LO to IF isolation characteristics, when RF input frequencies were swept in the range of 1 to 8 GHz for the down-conversion mixer.

Figure 15 shows the measured power conversion gain and input 3rd-order intercept point (IIP3) when LO input power was -5 dBm, IF frequency was fixed at 200 MHz, and RF input frequencies were swept in the range of 1 to 8 GHz for the down-conversion mixer. Figure 16 shows the LO to RF isolation and LO to IF isolation according to the RF input frequencies when the LO input power was -5 dBm, RF input power was -30 dBm, and IF frequency was fixed at 200 MHz for the down-conversion mixer. From Figs. 15 and 16, the measured results showed a positive power conversion gain from 1 to 8 GHz, a bandwidth of about 4.5 GHz, LO isolation (LO to RF isolation and LO to IF isolation) between 40 and 60 dB, and IIP3 between 0 and -4 dBm. The measured down-conversion mixer consumed a current of 21 mA for a 3.0 V supply voltage.

## V. Conclusions

The purpose of this paper was to monolithically implement matching circuits, interface circuits, and RF core circuits to the same substrate. Thus, in this paper a 1 to 6 GHz MMIC up-conversion mixer for an RF transmitter was designed and fabricated using a 0.8  $\mu\text{m}$  SiGe HBT process technology; and an IF matching circuit, LO/RF wideband matching circuits, IF/LO input balun circuits, and an RF output balun circuit were all integrated on-chip. The measured results obtained from the fabricated up-conversion mixer showed a positive power conversion gain from 1 to 6 GHz, a bandwidth of about 4.5 GHz, LO isolation (LO to IF isolation and LO to RF isolation) between 27 and 45 dB, and OIP3 between -2 and -12 dBm. The measured up-conversion mixer consumed a current of 29 mA for a 3.0 V supply voltage. Also, a 1 to 8 GHz MMIC down-conversion mixer for an RF receiver was designed and fabricated using the same process technology; and LO/RF wideband matching circuits, LO/RF input balun circuits, and an IF output balun circuit were all integrated on-chip. The measured results obtained from the fabricated down-conversion mixer showed a positive power conversion gain from 1 to 8 GHz, a bandwidth of about 4.5 GHz, LO isolation (LO to RF isolation and LO to IF isolation) between 40 and 60 dB, and IIP3 between 0 and -4 dBm. The measured down-conversion mixer consumed a current of 21 mA for a 3.0 V supply voltage.

These results are believed to be the first single chip mixer MMIC with the input and output matching circuits and active baluns covering a 1 to 8 GHz band for the receiver and a 1 to 6 GHz band for the transmitter. We believe this paper is useful for researchers working in RF circuit design.

## References

- [1] Seung-Yun Lee, Hong-Seung Kim, Sang-Heung Lee, Kyu-Hwan Shim, Jin-Yeong Kang, and Min-Kyu Song, "The Behavior of Ti Silicidation on Si/SiGe/Si Base and Its Effect on Base Resistance and  $f_{\text{max}}$  in SiGe Hetero-Junction Bipolar Transistors," *J. of Materials Science: Materials in Electronics*, vol. 12, no. 8, Aug. 2001, pp. 467-472.
- [2] John D. Cressler, "SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 46, no. 5, May 1998, pp. 572-589.
- [3] Chang-Woo Kim and Young-Gi Kim, "A 2.7-V SiGe HBT Variable Gain Amplifier for CDMA Application," *IEEE Microwave and Wireless Components Lett.*, vol. 13, no. 12, Dec. 2003, pp. 502-504.
- [4] Young-Gi Kim, Shin-Young Yoon, Hyuk Kim, Seung-Hee Yoo, Young-Gul Kim, Kyung-Sik Baek, Chang-Woo Kim, Deok-Ho



Cho, Tae-Hyeon Han, and Byoung-Ryul Ryum, "A Dual Band SiGe MMIC LNA and Mixer with Ground Shield for WCDMA and CDMA Applications," *IEEE Radio and Wireless Conf.*, Aug. 2001, pp. 19-22.

- [5] Jonathan P. Comeau, John D. Cressler, Jongsoo Lee, and Alvin J. Joseph, "An 8.4-12.0 GHz Down-Conversion Mixer Implemented in SiGe HBT Technology," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Sept. 2004, pp. 13-16.
- [6] Young-Joo Song, Kyu-Hwan Shim, Jin-Young Kang, and Kyoung-Ik Cho, "DC and RF Characteristics of Si<sub>0.8</sub>Ge<sub>0.2</sub> pMOSFETs: Enhanced Operation Speed and Low 1/f Noise," *ETRI J.*, vol. 25, no. 3, June 2003, pp. 203-209.
- [7] Seok-Bong Hyun, Geum-Young Tak, Sun-Hee Kim, Byung-Jo Kim, Jinho Ko, and Seong-Su Park, "A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems," *ETRI J.*, vol. 26, no. 3, June 2004, pp. 229-240.
- [8] Sang-Heung Lee, Hyun-Chul Bae, Seung-Yun Lee, Jongdae Kim, Bo Woo Kim, and Jin-Yeong Kang, "A 1-6 GHz Monolithic Up-Conversion Mixer with Input/Output Active Baluns Using SiGe HBT Process," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Sept. 2004, pp. 17-20.
- [9] Guofu Niu, Shiming Zhang, John D. Cressler, Alvin J. Joseph, John S. Fairbanks, Lawrence E. Larson, Charles S. Webster, William E. Ansley, and David L. Harnage, "Noise Modeling and SiGe Profile Design Tradeoffs for RF Applications," *IEEE Trans. on Electron Devices*, vol. 47, no. 11, Nov. 2000, pp. 2037-2044.
- [10] William E. Ansley, John D. Cressler, and David M. Richey, "Base-Profile Optimization for Minimum Noise Figure in Advanced UHV/CVD SiGe HBT's," *IEEE Trans. on Microwave Theory and Techniques*, vol. 46, no. 5, May 1998, pp. 653-660.
- [11] Ja-Yol Lee, Dongwoo Suh, Sang-Heung Lee, Seung-Yun Lee, Chan-Woo Park, Sang-Hoon Kim, Kyu-Hwan Shim, Jin-Yeong Kang, Kyung-Ik Cho, and Seung-Hyeob Oh, "A Packaged 2.3 GHz SiGe VCO with Parallel-Branch Inductors," *IEEE MTT-S Int'l Microwave Symp. Digest*, vol. I, Philadelphia, Pennsylvania, June 2003, pp. 141-144.
- [12] Dae-Yeon Kim, Sang-Gug Lee, and Jin-Hyo Lee, "Up-Conversion Mixer for PCS Application Using Si BJT," *IEEE 2nd Int'l Conf. on Microwave and Millimeter Wave Technology Proc.*, 2000, pp. 424-427.



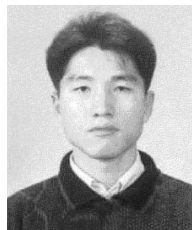
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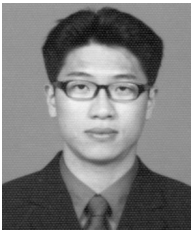
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