A New Strained-Si Channel Power MOSFET for High Performance Applications

Young-Kyun Cho, Tae Moon Roh, and Jongdae Kim

ABSTRACT—We propose a novel power metal oxide semiconductor field effect transistor (MOSFET) employing a strained-Si channel structure to improve the current drivability and on-resistance characteristic of the high-voltage MOSFET. A 20 nm thick strained-Si low field channel NMOSFET with a 0.75 μm thick $Si_{0.8}Ge_{0.2}$ buffer layer improved the drive current by 20% with a 25% reduction in on-resistance compared with a conventional Si channel high-voltage NMOSFET, while suppressing the breakdown voltage and subthreshold slope characteristic degradation by 6% and 8%, respectively. Also, the strained-Si high-voltage NMOSFET improved the transconductance by 28% and 52% at the linear and saturation regimes.

Keywords—High voltage, power device, strained-Si, hot electron, breakdown voltage.

I. Introduction

High-voltage metal oxide semiconductor field effect transistors (MOSFETs), which have a high switching speed and low on-resistance characteristic compared to other power devices [1]-[3], are recognized to be the most promising power devices. However, these devices have a low transconductance (G_m), small signal output resistance, and small threshold voltage, which are caused by a hot electron effect due to the large lateral electric field.

To cope with these problems, a lower doping concentrated extension region is formed [4]. The high-voltage capability was achieved through the use of an n-type diffused region outside the gate to sustain most of the drain voltage. The presence of the extension region substantially enhances the breakdown voltage, but cannot control the low on-resistance precisely and achieve large current drivability. Typically, a 10 to 20% current and transconductance loss is present in extended drain power devices compared with conventional ones.

In this letter, we propose a novel power MOSFET employing a low electric field strained-Si channel structure in order to overcome the disadvantages of the conventional Si channel high-voltage MOSFET, such as a large electric field, high on-resistance, low G_m, and low current drivability.

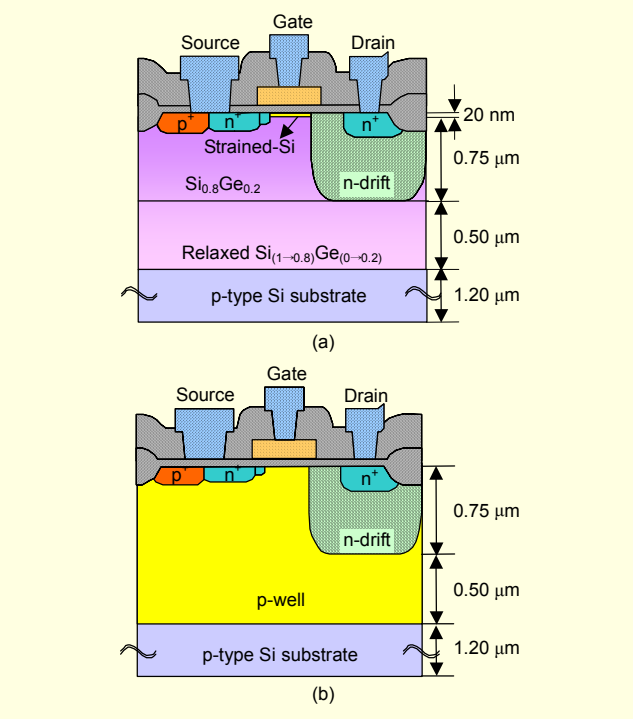

Fig. 1. Schematic figure of (a) the strained-Si channel high-voltage NMOSFET and (b) a conventional Si channel high-voltage NMOSFET.

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II. Device Structure and Simulation

The proposed new high-voltage device and conventional high-voltage device structures are shown in Figs. 1(a) and 1(b), respectively. These devices have the same physical dimension and doping profile. The key structure steps of the proposed device are the following: a) relaxed $Si_{(1\rightarrow0.8)}Ge_{(0\rightarrow0.2)}$ layer formation on the Si substrate, b) buffer $Si_{0.8}Ge_{0.2}$ layer formation with uniform doping concentration on the relaxed layer, c) strained-Si layer formation for the Si channel, d) n-drift region formation for higher breakdown voltage, e) threshold adjustment implantation, f) gate oxide formation, LDD formation, side-wall formation, source/drain implantation, and g) final contact and metal. A summary of the fabrication process is represented in Fig. 2. The final Si layer thickness for the strained-Si channel is 20 nm, which can decrease the breakdown voltage but increase current drive capability of the high-voltage NMOSFET (HVNMOS). The uniform $Si_{0.8}Ge_{0.2}$ layer and the relaxed $Si_{0.8}Ge_{0.2}$ layer thicknesses are 0.75 and 0.5 μm, respectively, in order to form a surface strained-Si channel layer.

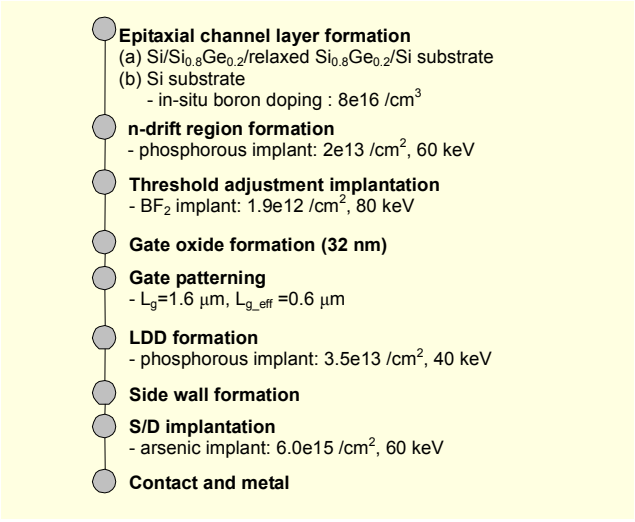

Fig. 2. Summary of the process sequence.

Table 1. Material properties for device simulation.

	Strained-Si	$Si_{0.8}Ge_{0.2}$
Electron affinity	4.304 eV	4.17 eV
Band gap energy	1.0 eV	0.94 eV
Dielectric constant	11.8	12.64
Electron effective mass	0.19 m_0	

III. Results and Discussion

In the development of the HVNMOS structure, two dimensional device simulations [5] were performed for the structures of Figs. 1(a) and 1(b) with the strained-Si channel and conventional Si channel to obtain the optimized electrical characteristics and study high-voltage devices. The unstrained energy band model was chosen for SiGe, and the energy band for the strained-Si was generated based on [6] through [9]. The material properties for device simulation are summarized in Table 1.

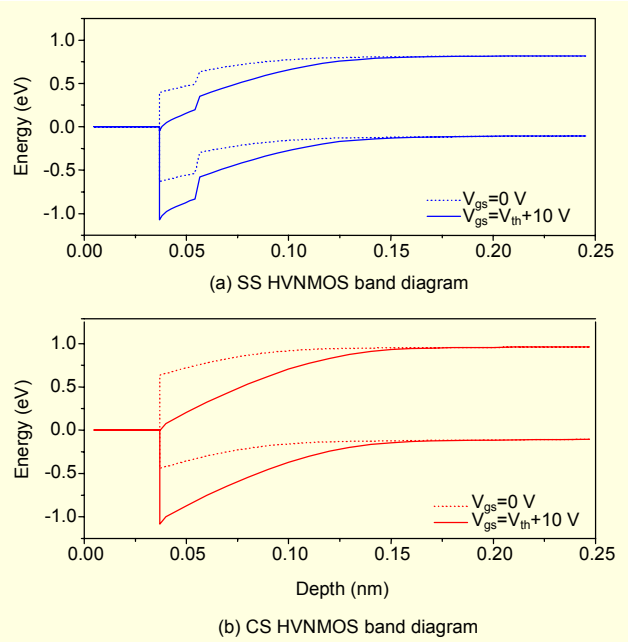

Fig. 3. Calculated energy band diagrams for (a) SS HVNMOS and (b) CS HVNMOS. The solid and dotted lines represent $V_{gs}=V_{th}+10$ V and $V_{gs}=0$ V, respectively.

Figure 3 shows the calculated electronic energy band diagrams for the strained-Si channel high-voltage NMOSFET (SS HVNMOS) and conventional Si channel high-voltage NMOSFET (CS HVNMOS) at $V_{gs} = V_{th} + 10$ V and $V_{gs} = 0$ V, respectively. As illustrated in Fig. 3(a), the conduction band bending due to the heterostructure is helpful to carrier confinement, and the valence band offset fully contributes to the threshold voltage shift. In other words, the negative valence band offset makes the Fermi level closer to the conduction band, and in turn, accumulates more electrons in the inversion layer for the same gate bias. Thus, the band offset lowers the threshold voltage. The simulated threshold voltages of SS HVNMOS and CS HVNMOS are 0.51 V and 0.94 V, respectively.

The modulated band profile in the strained-Si/SiGe layer

reduces the electronic energy band bending, and thus the electric field in the SS HVNMOS alleviates slightly compared with the CS HVNMOS. The simulated field distribution at the same gate overdrive condition for the devices of Figs. 1(a) and 1(b) are illustrated in Figs. 4(a) and 4(b), respectively. It can clearly be seen that the peak electrical field (2.4×10^5 V/cm) at near the drain region of the SS HVNMOS is lower than that (2.6×10^5 V/cm) of the CS HVNMOS. These results lead to the higher electron mobility and lower series resistance.

In spite of the smaller electric field, strained-Si devices have higher impact ionization rates compared to bulk-Si devices due to the smaller energy bandgap and longer mean-free-path. This implies that the mean-free-path in strained-Si for high current operation should be reduced from that used in the lower electric field regime. So, the breakdown voltage (V_{BR}) of the SS HVNMOS is slightly lowered. The breakdown voltages of the SS HVMOS and CS HVMOS are 22.7 V and 24.0 V at the critical electric field, as shown in Fig. 5. The inset of Fig. 5 shows the drain current - drain voltage characteristics of high-voltage NMOSFETs with the strained-Si channel and the conventional Si channel. It reveals a significant current gain for the SS HVNMOS. The result could be explained as the re-population of the energy bands produces an enhancement of the effective electron mobility, and the material properties of SiGe produce a reduction of the channel electric field. Then, the SS HVNMOS exhibited a 20% increase in drive current compared with the CS HVNMOS. The simulated on-resistances (R_{ds}) of the SS HVNMOS was 0.24 Ω·m, which is about 25% lower compared with the value of 0.30 Ω·m obtained from the CS HVNMOS.

The linear and saturation transconductance characteristics of

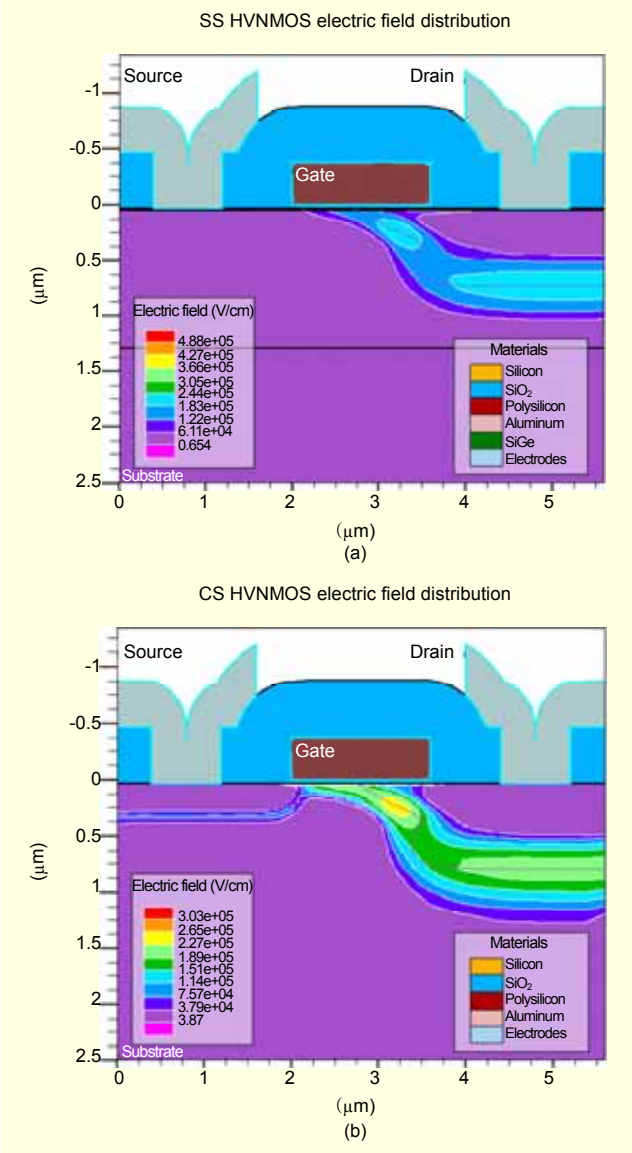

Fig. 4. Simulated electric field distributions for (a) SS HVNMOS and (b) CS HVNMOS.

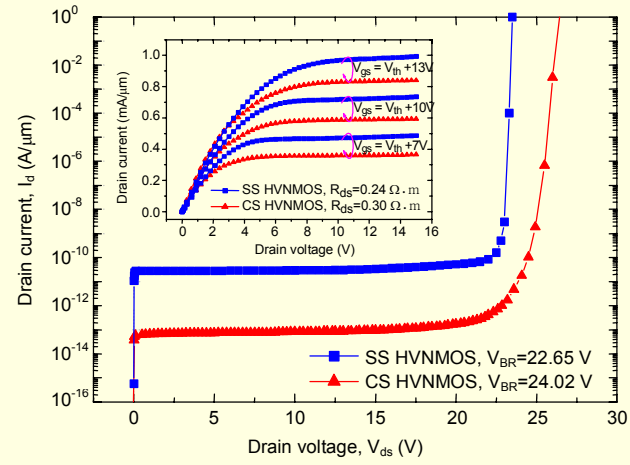

Fig. 5. Breakdown voltage characteristics of the SS HVNMOS compared with the CS HVNMOS. The inset shows the drain current - drain voltage characteristics.

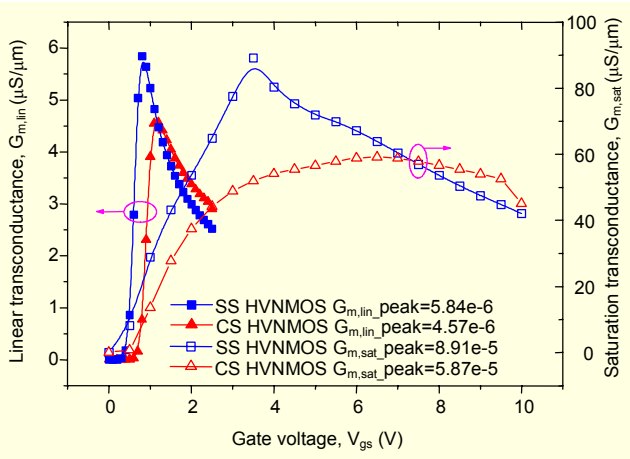

Fig. 6. Linear and saturation G_m characteristics of the SS HVNMOS and CS HVNMOS.

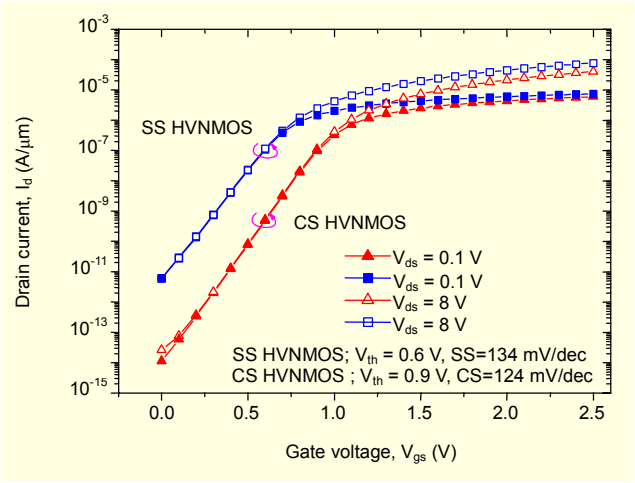

Fig. 7. Simulated subthreshold transfer characteristics of the SS HVNMOS and CS HVNMOS.

the SS HVNMOS and CS HVNMOS are shown in Fig. 6. The gate voltage at which peak transconductance occurs depends on the value of V_{ds} and the device type, that is, strained-Si or control Si. The transconductance of the SS HVNMOS improved by 28% and 52% at the linear and saturation regimes, respectively, compared to the CS HVNMOS. This is due to the mobility enhancement effect of the SS HVNMOS. The subthreshold slope of the SS HVNMOS is 134 mV/dec, which is higher compared with the 124 mV/dec obtained from the CS HVNMOS as shown in Fig. 7. The thickness of the strained-Si layer is smaller than the depletion depth at zero gate bias, as illustrated in Fig. 3; the subthreshold slope degrades due to the higher depletion capacitance, as a consequence of the higher dielectric constant of SiGe and shallower channel depletion depth.

IV. Conclusion

In summary, we propose a novel high-voltage NMOSFET structure employing a strained-Si channel structure to improve the current drive capability and on-resistance characteristic. With the slightly lowered breakdown voltage, the current drive capability and on-resistance are improved by 20% and 25%, respectively. These results indicate that the HVNMOS with a strained-Si channel is a promising candidate for a display driver integrated circuit because this device can decrease the chip size by a high current drivability.

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