Low-Power Direct Conversion Transceiver for 915 MHz Band IEEE 802.15.4b Standard Based on 0.18 μm CMOS Technology

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This paper presents the experimental results of a low-power low-cost RF transceiver for the 915 MHz band IEEE 802.15.4b standard. Low power and low cost are achieved by optimizing the transceiver architecture and circuit design techniques. The proposed transceiver shares the analog baseband section for both receive and transmit modes to reduce the silicon area. The RF transceiver consumes 11.2 mA in receive mode and 22.5 mA in transmit mode under a supply voltage of 1.8 V, in which 5 mA of quadrature voltage controlled oscillator is included. The proposed transceiver is implemented in a 0.18 μm CMOS process and occupies 10 mm^2 of silicon area.

Keywords: 1/f noise, CMOS, DC offset, direct conversion, IEEE 802.15.4b, low cost, low power, radio transceiver, RF integrated circuits, sensor network, WPAN.

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I. Introduction

Wireless LAN has grown rapidly in recent years. Efforts to increase data rates have led to the development of the IEEE 802.11 standard, from an initial 1 to 2 Mbps in 802.11 [1] to as high as 54 Mbps in 802.11a and 802.11g [2], [3]. Most wireless LAN standards do not meet low-cost design objectives due to their high complexity, and high throughput requirements. Bluetooth (IEEE 802.15.1) [4] is the first well-known standard to face low data rate applications. However, Bluetooth is still struggling for success in the market due to its high complexity. Consequently, it is expensive and inappropriate for some simple applications requiring low cost and low power dissipation. An IEEE 802.15.4b task group has been established to develop a standard for low data rate wireless personal area networks (LR-WPANs) [5]. The target markets of this standard are home automation, PC peripherals, consumer electronics, industrial and commercial fields, personal healthcare, as well as toys and games.

This paper focuses on the implementation of a low-power low-cost transceiver by the selection of a suitable architecture and adoption of circuit design optimization techniques. Preliminary experimental results of implementing the RF receiver and RF transmitter front-end in separate chips have been presented in [6] and [7]. However, in this paper, we will discuss system planning in more detail, and provide more experimental results for the whole receiver and transmitter chains, including an analog baseband section and an on-chip quadrature voltage-controlled oscillator.

Table 1. Data rate and sensitivity of IEEE 802.15.4b standard.

PHY (MHz)	Frequency band (MHz)	Spreading parameters		Data parameters		Sensitivity (dBm)
		Chip rate (kchip/s)	Modulation	Bit rate (kbps)	Symbol rate (ksymbol/s)	
868/915	868 - 868.6	300	BPSK	20	20	-92
	902 - 928	600	BPSK	40	40	-92
868/915 optional	868 - 868.6	440	PSSS	250	12.5	-85
	902 - 928	1600	PSSS	250	50	-85
868/915 optional	868 - 868.6	400	O-QPSK	100	25	-85
	902 - 928	1000	O-QPSK	250	62.5	-85
2450	2400 - 2483.5	2000	O-QPSK	250	62.5	-85

This paper is organized as follows. Section II gives an overview of the IEEE 802.15.4b standard, system planning, and the proposed transceiver architecture and solutions for direct conversion implementation. Section III describes the detailed circuit designs, section IV describes the measured results of the implemented chip, and section V concludes this work.

II. System Planning, Transceiver Architecture, and Design Considerations

1. IEEE 802.15.4b Overview

The IEEE 802.15.4b standard can operate in three frequency bands: 868 MHz in Europe, 915 MHz in the US, and 2.4 GHz globally. In the 868 MHz and 915 MHz bands, there are three optional modulation schemes: binary phase shift keying (BPSK), offset quadrature phase shift keying (O-QPSK), and parallel sequence spread spectrum (PSSS) as shown in Table 1. In terms of data rate, 250 kbps at 2.4 GHz, from 20 kbps to 250 kbps at 868 MHz, and from 40 kbps to 250 kbps at 915 MHz can be supported, depending on the modulation scheme. Figure 1 shows the channel assignment of the IEEE 802.15.4b standard, in which only one channel is assigned for the 868 MHz band, 10 channels for the 915 MHz band, and 16 channels for the 2.4 GHz band, respectively. The center frequencies of these channels are defined as follows:

$$fc = 868.3\ [\text{MHz}] \quad \text{for } k = 0,$$
$$fc = 906 + 2(k-1)\ [\text{MHz}] \quad \text{for } k = 1, 2, \cdots, 10,$$
$$fc = 2405 + 5(k-11)\ [\text{MHz}] \quad \text{for } k = 11, 12, \cdots, 26,$$

where k is the channel number.

In the receiver, the required sensitivity is defined as a threshold input signal power that yields a packet error rate (PER) of less than 1%. The minimum sensitivity is -92 dBm for 868/915 MHz bands employing BPSK, and -85 dBm for O-QPSK and PSSS modulation schemes. In the 2.4 GHz band, the sensitivity is -85 dBm. The receiver should be able to receive an input signal at -20 dBm for all cases. In the transmitter, as specified in IEEE 802.15.4b, at least -3 dBm should be transmitted with an error vector magnitude (EVM) of less than 35 % for 1,000 chips. However, 0 dBm output transmit power is preferred.

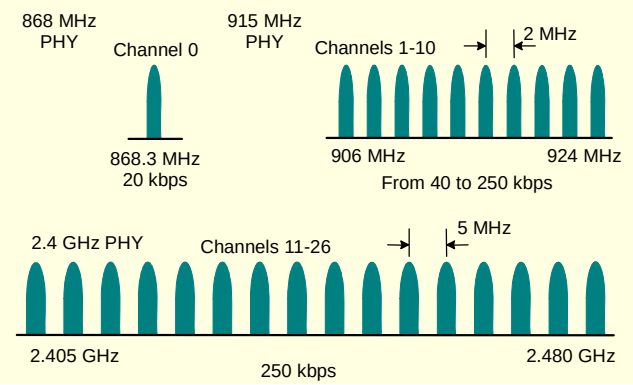

Fig. 1. Channel allocation in IEEE 802.15.4b standard.

This work focuses on the development of an RF transceiver for the 915 MHz band only; therefore, only the radio specifications for the 915 MHz band will be derived as in the following subsection.

2. System Planning for 915 MHz Band

System specifications for the draft version of IEEE 802.15.4b [5] were derived in detail in [8]. However, this work attempts to re-derive the system specifications for the final version of the IEEE 802.15.4b standard [9] reflecting the modifications in the final version.

The relevant required specifications for the design of radio receivers are noise figure (NF), nonlinearity, and the filter characteristic, which is related to the selectivity of the receiver.

The NF of a receiver system in decibels can be derived as given in [10] from the following expression:

$$NF = 174 - P_{in,min} - 10\log BW - SNR_{min}, \quad (1)$$

where BW, $P_{in,min}$, and SNR_{min} are the channel bandwidth, the sensitivity, and the minimum required signal-to-noise ratio of a receiver system, respectively. As defined in IEEE 802.15.4b PHY, the required PER must be less than 1% and the packet average length is 22 bytes. This leads to a BER under 5.7×10^{-5}.

With the BPSK modulation scheme, to obtain a BER of 5.7×10^{-5}, the required SNR_{min} is approximately 8.8 dB. However, the IEEE 802.15.4b standard employs a direct sequence spread spectrum (DSSS) technique with a chip-to-bit ratio of 600 kchip/s to 40 kbps, resulting in processing gain of 12 dB. Therefore, the required SNR_{min} is approximately -3.2 dB. From (1), the required NF of the receiver system is about 19.5 dB, considering the minimum sensitivity of -92 dBm, the BW of 1.2 MHz in the 915 MHz band, and the 5 dB implementation margin.

Similarly, for the O-QPSK modulation scheme, the required SNR_{min} is 2.5 dB considering a 6 dB processing gain (1,000 kchip/s to 250 kbps). With the minimum sensitivity of -85 dBm specified in the standard, the required NF of the receiver is about 20.5 dB assuming a 5 dB implementation margin.

With PSSS modulation, the required SNR for 1% PER is about 4.8 dB [11]. Therefore, the required NF of the receiver is about 24.5 dB considering an 8 dB processing gain, -85 dBm sensitivity, and a 5 dB implementation margin.

The nonlinearity of the receiver system is typically represented by an input third-order intercept point, IIP_3, and an input second-order intercept point IIP_2.

The IIP_3 is derived from the two-tone test. Similar to the effect of noise, the third-order intermodulation product (IM3) must be less than the desired signal by the value of the required SNR_{min}. Therefore, the IIP_3 of the receiver can be calculated as given in [8] and [12] by

$$IIP_3 = \frac{1}{2}\left(3P_{int} - P_{sig} + SNR_{min} + \text{Margins}\right), \quad (2)$$

where P_{int} and P_{sig} are the interferer and signal levels when the IM test is conducted. As specified in the IEEE 802.15.4b PHY, the intermodulation test is performed when the signal power and the interfering power levels are -89 dBm and -59 dBm for BPSK and -82 dBm and -52 dBm for O-QPSK, and PSSS modulation schemes, respectively. From (2), considering the 10 dB implementation margin, the required IIP_3 for BPSK, O-QPSK, and PSSS modulation schemes are -40.5 dBm, -35 dBm, and -39 dBm, respectively. As mentioned in the IEEE 802.15.4b PHY, the maximum input power level is -20 dBm; therefore, the input 1 dB compression point should be higher than -20 dBm. Consequently, the required IIP_3 is -10 dBm, in the low gain mode, assuming the 1 dB compression point is 10 dB lower than the IIP_3.

Like the IIP_3, the IIP_2 test is performed when two nearby interferers at f_1 and f_2 equal f_1-Δf. Because the receiver produces a second-order distortion, a low frequency beat at Δf appears at the output of the receiver [12]. So that the receiver can detect the desired signal, this low-frequency beat must be less than the desired signal by the SNR_{min} value. Therefore, the minimum required IIP_2 of the receiver is given as in [12] by

$$IIP_2 = 2P_{int} - P_{sig} + SNR_{min} + \text{Margins}. \quad (3)$$

With an interfering power at the blocker level of -30 dBm, and SNR_{min} of -3.2, 2.5, and -2.2 dB for BPSK, O-QPSK, and PSSS modulation schemes, respectively, the desired signal must be at least -60 dBm to satisfy the jamming resistance requirements. From (3), assuming a 10 dB implementation margin, the required IIP_2 is 6.8, 12.5, and 7.3 dBm for BPSK, O-QPSK, and PSSS modulation schemes, respectively.

The characteristic of the channel selection filter can be derived from the requirement of the jamming resistance. As mentioned in the IEEE 802.15.4b PHY, 0 dB rejection at adjacent channels and 30 dB rejection at the alternate channels are required. Assuming a 10 dB implementation margin, 10 dB and 40 dB rejections at adjacent and alternate channels are sufficient. To satisfy this requirement, a third-order Butterworth filter with a cut-off frequency of 650 kHz and 46 dB rejection at 4 MHz [8] is chosen.

The required phase noise (PN) is given as in [13] by

$$PN\left(\text{dBc/Hz}\right) = P_{sig} - P_{int} - SNR_{min} - 10\log BW - \text{Margin}. \quad (4)$$

With a minimum sensitivity signal power of -92 dBm for BPSK modulation, -85 dBm for O-QPSK and PSSS modulations; an SNR_{min} of -3.2 dB for BPSK, +2.5 dB for O-QPSK, and -2.2 dB for PSSS modulations; a BW of 1.2 MHz; and about 10 dB implementation margin; the calculated PN requirements are -68 dBc/Hz, -73 dBc/Hz, and -68.5 dBc/Hz at the adjacent channels for BPSK, O-QPSK, and PSSS modulation schemes, respectively. This PN requirement is easily achieved in a conventional CMOS LC VCO.

In the transmitter chain, there is no difference between the draft and final versions of IEEE 802.15.4b standard; therefore, the transmitter specifications are taken from [8]. The radio specifications for the 915 MHz band IEEE 802.15.4b standard are summarized in Table 2. As shown in Table 2, the receiver specifications are slightly different for each modulation scheme. Therefore, for one transceiver to be able to operate under three modulation schemes, the radio specifications should be revised as proposed in Table 3.

The next step is to allocate the module's specifications in the

Table 2. Radio specifications with three different modulation schemes for 915 MHz band IEEE 802.15.4b standard.

Modules	Parameters		BPSK	O-QPSK	PSSS
Receiver	Sensitivity (dBm)		-92	-85	-85
	NF (dB)		19.5	20.5	24.5
	IIP3 (dBm)	@ high gain mode	-40.5	-35	-39
		@ low gain mode	-10	-10	-10
	IIP2 (dBm)		6.8	12.5	7.3
	SFDR (dB)		39	36	34
	Gain control range (dB)		72	65	65
	Low-pass filter		3rd order, fc= 650 kHz		
Transmitter	Output power (dBm)		0	0	0
	OP 1dB (dBm)		2	2	2
	OIP3 (dBm)		12	12	12
	Low-pass filter		2nd order, fc=650 kHz		
	Gin control range (dB)		20		
Frequency synthesizer	PN (dBc/Hz) @ 2 MHz offset		-68	-73	-68.5
	Settling time (μs)		40		
	Power (dBm)		0		

Table 3. Target radio specifications for 915 MHz band IEEE 802.15.4b standard.

Modules	Parameters		Specifications
Receiver	NF (dB)		19.5
	IIP3 (dBm)	@ high gain mode	-35
		@ low gain mode	-10
	IIP2 (dBm)		12.5
	SFDR (dB)		39
	Low-pass filter		3rd order, fc=650 kHz
	Gain control range (dB)		72
Transmitter	Output power (dBm)		0
	OP 1dB (dBm)		2
	OIP3 (dBm)		12
	Low-pass filter		2nd order, fc=650 kHz
	Gin control range (dB)		20
Frequency synthesizer	PN (dBc/Hz) @ 2 MHz		-73
	Settling time (μs)		40
	Power (dBm)		0

transceiver architecture. Here, the transceiver is divided into four individual modules as shown in Fig. 2 (The abbreviations used in Fig. 2 are used in the text for convenience). The Rx-RF module includes a low-noise amplifier (LNA) and a down-conversion mixer; the Tx-RF module consists of an up-conversion mixer and driver amplifier (DA); and the Rx-BB module (analog baseband section in the receiver chain) includes a low-pass filter $(LPF)_{1\text{-}2}$ and variable gain amplifier $(VGA)_{1\text{-}2}$. The Tx-BB module (analog baseband section in the transmitter chain) includes LPF_2 and VGA_2.

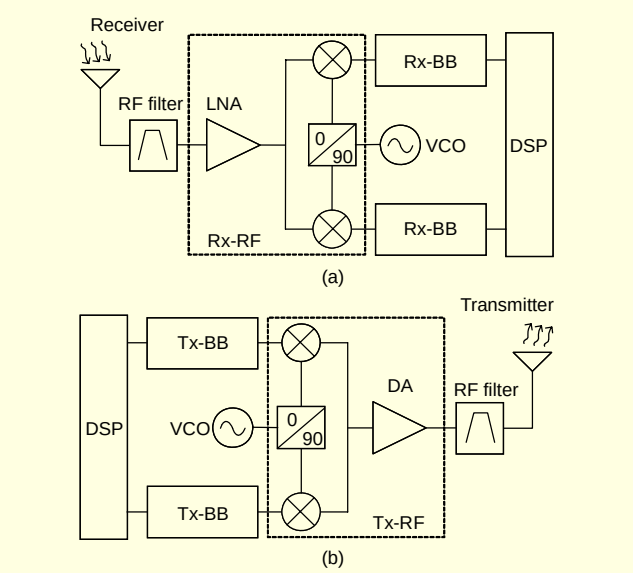

Fig. 2. Block diagram of (a) receiver and (b) transmitter.

Normally, to determine the NF specifications of an individual block in the cascade system, Friis's equation [14] is used. Using the abbreviations in Fig. 2, as given in [10], we have

$$NF_{total} = NF_{Rx-RF,R_S} + \frac{NF_{Rx-BB,R_{out,Rx-RF}} - 1}{A_{P,Rx-RF}}, \quad (5)$$

where $NF_{Rx\text{-}RF}$ and $A_{P,Rx\text{-}RF}$ are the NF and the available power gain of the Rx-RF block, respectively. The available power gain of the Rx-RF block is given by

$$A_{P,Rx-RF} = \left(\frac{R_{in,Rx-RF}}{R_S + R_{in,Rx-RF}}\right)^2 A_{v,Rx-RF}^2 \frac{R_S}{R_{out,Rx-RF}}, \quad (6)$$

where R_s is the source impedance, R_{in}, R_{out}, and A_v are the input impedance, output impedance, and voltage gain of the Rx-RF module, respectively.

To calculate IIP_3, the following expression given in [10] is used:

$$\frac{1}{A_{IIP_3,total}^2} \approx \frac{1}{A_{IIP_3,Rx-RF}^2} + \frac{A_{v,Rx-RF}^2}{A_{IIP_3,Rx-BB}^2}. \quad (7)$$

As can be seen from (5)-(7), there are many possible combinations of block specification that meet the requirements. Specifications were based on our experience and the experimental results of the previous designs. During the design

Table 4. Target specifications of the proposed transceiver.

	Parameters		RF	Baseband
Rx	Voltage gain (dB)		20	-20 to 65
	NF (dB)		4	26
	IIP3 (dBm)	@ high gain mode	-12	-30
		@ low gain mode	-8	10
	IIP2 (dBm)		> 20	> 20
	I/Q mismatch	Gain (dB)	< 2	< 2
		Phase (deg.)	< 2	< 2
Tx	Gain (dB)		10	-10 to 20
	OP 1dB (dBm)		2	-5
	OIP3 (dBm)		12	5
	OIP2 (dBm)		> 30	> 30
	I/Q mismatch	Gain (dB)	< 2	< 2
		Phase (deg.)	< 2	< 2

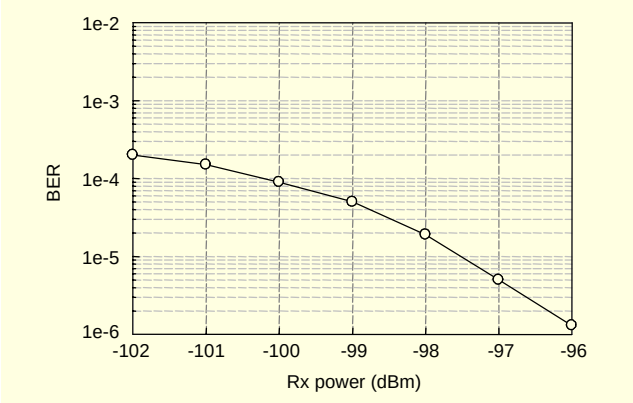

Fig. 3. Simulated BER performance of receiver.

process, some of the values were revised based on the design experimental results. Therefore, we believe that the given specifications are optimal for a transceiver design with low power consumption. The final specifications of the individual modules are listed in Table 4.

After assigning the specifications for individual modules, the system simulations were performed to verify the target specifications given in Table 4. These simulations were based on a commercial simulation tool ADS. For simplicity, the signal was assumed to propagate through an additive white Gaussian noise (AWGN) channel with no fading. Figure 3 shows the simulated BER performance of the 915 MHz band receiver. It achieved -94 dBm sensitivity with 5 dB implementation margins. Figure 4 shows the simulated output spectrum of the 915 MHz band transmitter along with a spectrum mask. As shown in Figs. 3 and 4, the target

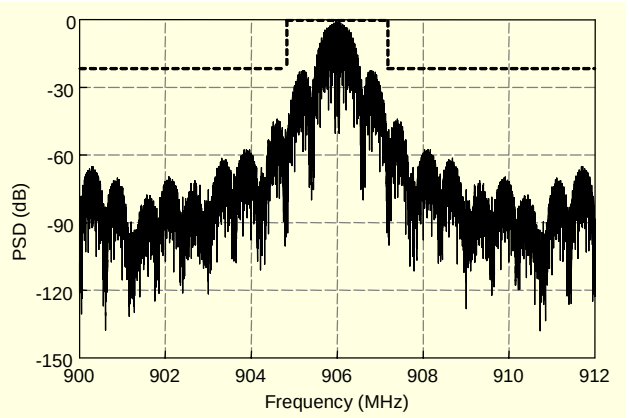

Fig. 4. Simulated output power spectrum density of transmitter.

specifications given in Table 4 satisfy the requirement of IEEE 802.15.4b PHY.

3. Transceiver Architecture

Recently, direct conversion transceiver architecture has been adopted for many wireless transceiver implementations due to its high level of integration and low power consumption. In the direct conversion architecture, no image rejection filter is needed, and the IF band-pass filter is replaced by the low-pass filter. However, this architecture has some disadvantages, such as DC-offset, even-order distortion, flicker noise, I/Q mismatch, LO pulling/pushing, and so on [15], [16]. In this work, considering the need for low cost and low power consumption, a direct conversion architecture was chosen. The proposed transceiver architecture is shown in Fig. 5. Integrated on a single chip, the transceiver contains a direct conversion receiver, where the received radio frequency signal is amplified by an LNA and directly down-converted to a baseband signal by a down-conversion mixer. The analog baseband section consists of an alternating combination of LPFs and VGAs. The transceiver further contains a direct conversion transmitter, where the baseband signal is low-pass filtered by LPF_2 and amplified by VGA_2. Then, this signal is up-converted to RF through the balance mixer. The RF signal is amplified by the on-chip DA. As can be seen in Fig. 5, the LPF_2 and VGA_2 in the base-band section are reused for both the receiver and transmitter considering the time division duplex (TDD) operation of the IEEE 802.15.4b standard. As an economical result, the chip size is reduced. One disadvantage of this configuration is that the VGA_2 and LPF_2 must be designed to satisfy the requirements for both the receiver and transmitter. However, this is not difficult to achieve.

As previously mentioned, direct conversion suffers from DC offset, 1/f noise, even-order distortion, I/Q mismatch, and LO

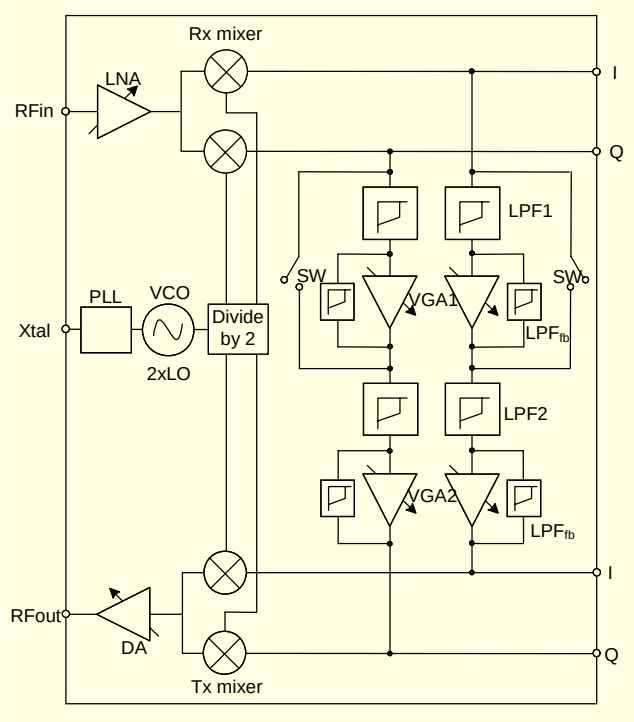

Fig. 5. Proposed transceiver architecture.

pulling/pushing issues. Therefore, for a direct conversion transceiver, the following design considerations are taken into account.

- The DC offset issue is eliminated by using a feedback low-pass filter, LPF_{fb}, acting as a feedback-loop in the VGA stage (see Fig. 5). As mentioned in [8], the cut-off frequency of LPF_{fb} can be chosen within 5% of the channel bandwidth. Therefore, the cut-off frequency of LPF_{fb} is about 30 kHz considering the 650 kHz cut-off frequency of the channel selection filter.
- The 1/f noise problem can be minimized by using a passive downconversion mixer and the DC feedback loop to cancel the DC offset issue.
- Even-order distortion, mainly dominated by second-order distortion, is eliminated by using the double-balance downmixer, careful layout, and symmetric tracing of the RF and LO paths. This issue is not very serious since the required IIP_2 is relaxed.
- The I/Q mismatch problem can be solved by symmetric layout. The required EVM of the IEEE 802.15.4b standard is not very high (35%); therefore, I/Q mismatch is not a critical issue.
- The LO pulling/pushing issue can be eliminated by operating a VCO at double the frequency of the desired signal and then dividing the frequency. The LO leakage due to the device mismatch can be suppressed by using a DC feedback correction circuit in the upconversion mixer [7].
- Regarding the transmitter, thanks to the relatively high input signals level, the problem of DC-offset becomes less critical. Still, the DC-offset needs to be minimized because it gives rise to LO feedthrough which overlaps with the modulated carrier. In this architecture, the DC-offset is implemented inside the VGA along with the receiver chain.

III. Circuit Implementation

1. RF Receiver

As previously mentioned, 1/f noise performance is one of the main critical issues in the direct conversion receiver. To overcome this problem, the front end of the RF receiver shown in Fig. 6 consists of a single-ended LNA and a balance passive mixer [6].

The single-ended LNA is used to reduce the power consumption as compared to a differential one. As Fig. 6 demonstrates, the LNA differs from the conventional inductive degeneration cascode LNA topology by one additional capacitor, C_{ex}. This LNA topology was used to obtain an NF equal to NF_{min} of the given LNA topology under very low power consumption [17]. In Fig. 6, the DC bias and device size of an input transistor M_1, and the value of C_{ex} and L_s are chosen following the design principle of a power-constrained simultaneous noise and input matching technique introduced in [17]. In addition, an off-chip inductor L_g is inserted to match the input impedance of the proposed RF receiver front end with the 50 Ω input impedance of the signal source. Here, the LNA and mixer are ac coupled by capacitor C_d to eliminate second-order intermodulation products generated by the LNA and to filter out DC offset. The loading inductor, L_d, is chosen by considering the trade-off between noise and gain of the mixer.

It can be said that the passive mixer dissipates no DC current and gives high linearity. The absence of DC current through the switches also makes it possible to eliminate the 1/f noise,

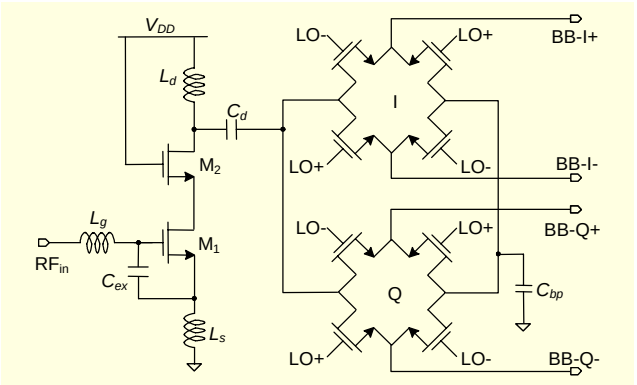

Fig. 6. Simplified schematic of RF receiver front end.

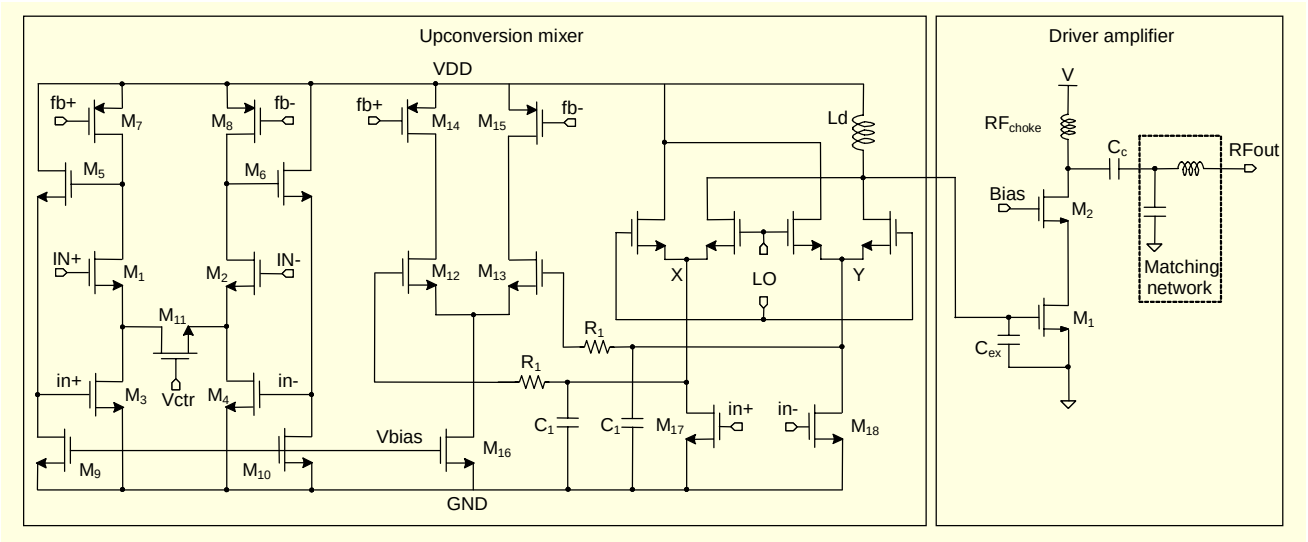

Fig. 7. Simplified schematic of RF transmitter front end.

which is a problem for direct conversion receivers. The detailed design optimization and performance trade-off of this passive mixer are described in [6].

The RF receiver front end is designed to provide a 20 dB voltage conversion gain and to dissipate 1 mA under a supply voltage of 1.8 V.

2. RF Transmitter

In the direct conversion transmitter chain, an LO leakage to the RF out port is one of the main drawbacks. In the upconversion mixer, the LO leakage is caused by either the mismatches in input signal or the mismatches in the DC current between two differential branches in the switching pair. To solve this problem, the upconversion mixer topology shown in Fig. 7 is adopted [7]. The DC feedback loop created by M_{12}-M_{16} is low-pass filtered and fed back to nodes X and Y in the switching pair to correct the mismatches in the DC current at those nodes. As shown in Fig. 7, an output RF signal of the upconversion mixer is then amplified by a conventional cascode driver amplifier topology with an additional capacitor, C_{ex}. This capacitor is added to the gate-source terminal of an input transistor M_1 to keep the input signal linear since the intrinsic gate-source capacitance, C_{gs}, which is essentially a bias dependent varactor, may lead to significant distortion at high input power levels [18]. The input transistor is biased at a high gate-source voltage to operate in class-A mode. The loading of the driver amplifier is chosen by considering the voltage and current swing at this node [19]. The total current consumption of the RF transmitter is 17.5 mA under a supply voltage of 1.8 V. The RF transmitter is expected to transmit an output power of 0 dBm.

3. Quadrature Voltage Controlled Oscillator

In the direct conversion architecture, quadrature signals must be incorporated. There are several techniques which can be used to generate quadrature signals, such as polyphase filtering, coupling two oscillators, and incorporating the differential VCO with a divide-by-2 circuit [20]. The latter approach has the advantages of being wideband and very compact. Moreover, it avoids any pushing/pulling effect on the VCO due to a strong signal from power amplifier (PA) in the direct conversion transmitter architecture. Also, since the oscillator operates at a higher frequency, it enables the use of smaller on-chip inductors, leading to the reduction of the silicon area. As a drawback, this approach consumes more power to run the frequency divider circuit and buffer; however, considering the buffers required by other solutions, the power consumption penalty is not very severe. Due to its many advantages, the latter approach is chosen in the proposed design.

Figure 8 shows a schematic diagram of a differential LC VCO which is implemented by using a stacked complementary differential configuration. The oscillation amplitude of this structure is approximately two times larger than that of the NMOS-only structure due to the conductance provided by the PMOS pair [21]. This property helps to reduce the VCO power dissipation while maintaining a necessary output swing because the passive mixer adopted requires a high LO amplitude. Rise and fall time symmetry is also incorporated in the VCO design to further reduce the 1/f noise up conversion [21]. These properties result in a better phase noise performance for a given tail current.

The frequency tuning characteristic is implemented by using a 2-bit switched capacitor array incorporated into a pn-junction

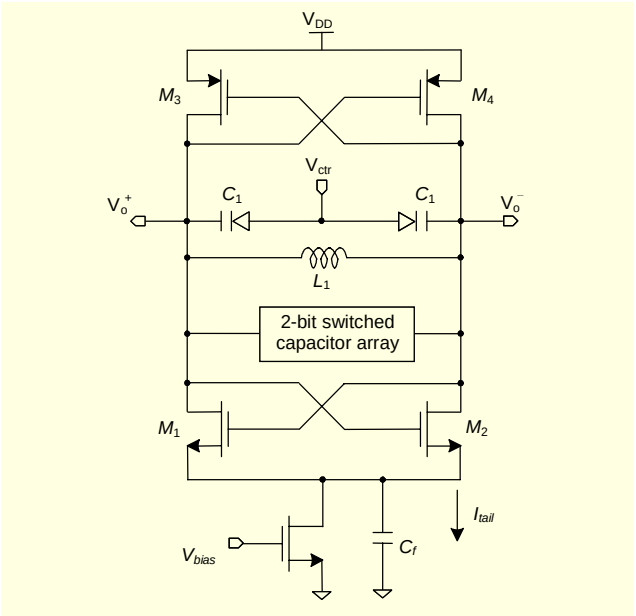

Fig. 8. Simplified schematic of differential LC VCO.

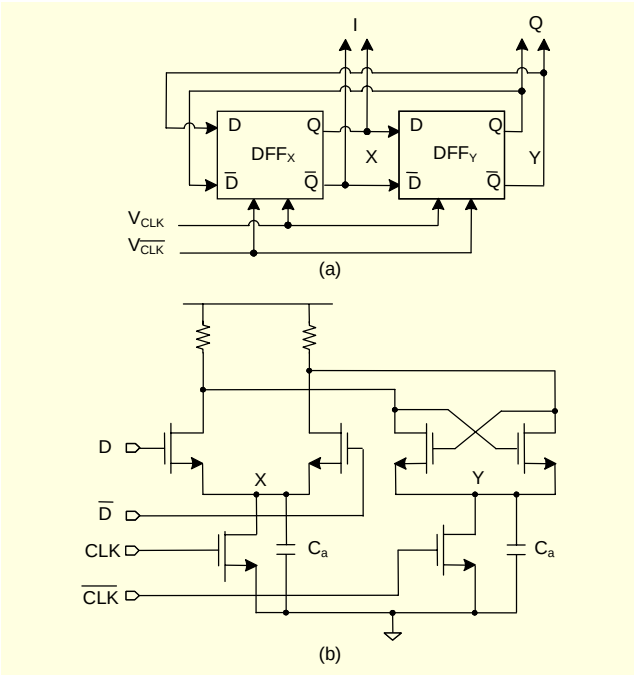

Fig. 9. (a) Block diagram and (b) schematic of divide-by-2 circuit.

varactor. In Fig. 8, an on-chip bypass capacitor C_f is added to introduce a low impedance path to ground for noise around $2\omega_o$ [22]. In the proposed design, the more accurate model of the on-chip spiral inductor described in [23] is adopted in the VCO simulation.

Figure 9 shows a block diagram and schematic drawing of the divide-by-2 circuit consisting of two latches in a negative feedback loop. Each latch is implemented by using a simple source-coupled-logic without a tail current. As shown in Fig. 9, an additional capacitor C_a is added at nodes X and Y to reduce the input signal magnitude and to filter the harmonics because large harmonics in this division will lead to undesired operation [22].

The QVCO is designed with a total current consumption of 5 mA, of which 0.6 mA, 1.2 mA, and 3.2 mA were assigned for the differential LC VCO, divide-by-2, and LO buffer, respectively.

4. Analog Baseband Section

A. Low-Pass Filter

There are three main type of implementation of active LPF [24]: MOSFET-C filters, G_m-C filters, and RC filters. The RC active filter, consisting of Opamps, resistors, and capacitors, is the most widely adopted. The advantages of the active RC filtering technique are insensitivity to parasitics, suitability for low supply voltages, good linearity, and a large dynamic range. The speed of this type of LPF is sufficient for modern wideband communication systems, like WCDMA, WLAN, and IEEE 802.15.4b. Due to its many advantages, the active RC-filter is chosen in this work. A simplified schematic of the implemented active RC LPF is shown in Fig. 10. Composed of one Opamp and an RC network, this circuit provides a second-order characteristic. To adjust the cut-off frequency on the basis of the process and temperature variations, capacitor C_2 is implemented as a binary weighted capacitor array [25], as shown in the righthand side of Fig. 10.

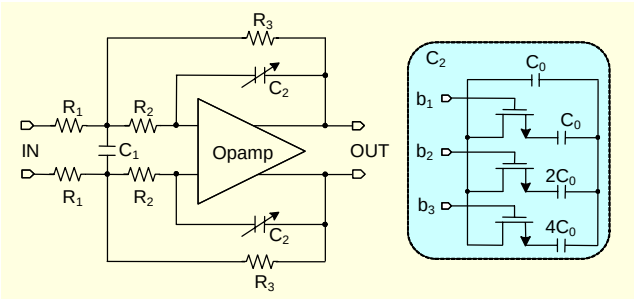

Fig. 10. Simplified schematic of LPF.

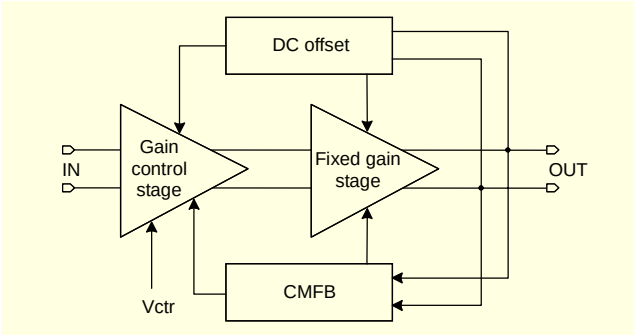

Fig. 11. Block diagram of the VGA.

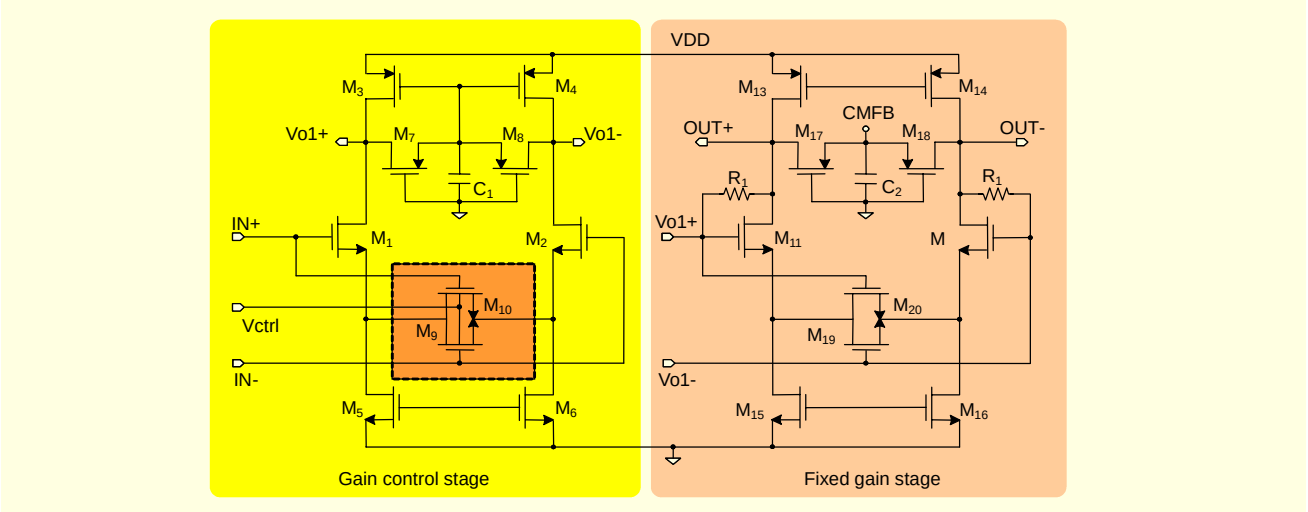

Fig. 12. Simplified schematic of variable gain amplifier.

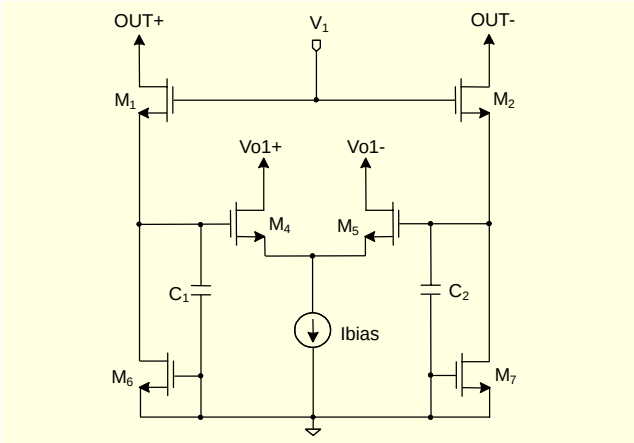

Fig. 13. Schematic of DC offset circuitry.

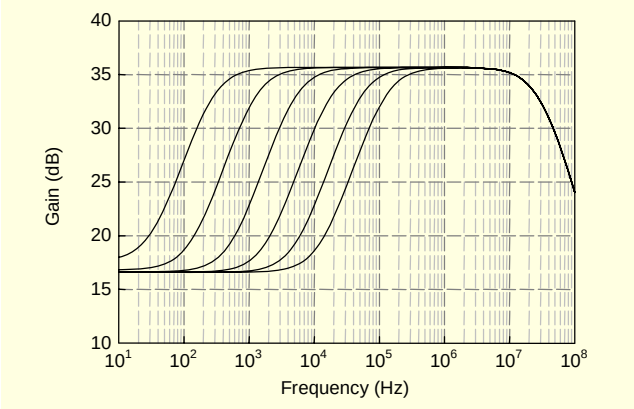

Fig. 14. Simulated VGA incorporated with DC offset circuit.

B. Variable Gain Amplifier

A block diagram of the implemented VGA is shown in Fig. 11. It consists of two amplifier stages. The first stage has a gain control function and the second stage is a fixed gain amplifier to provide a sufficient gain. A detailed schematic of the VGA is shown in Fig. 12. The first and second stages consist of an identical standard differential pair. In the first stage (gain control stage), two degeneration MOS transistors M_9 and M_{10} are used as a gain control function; in the second stage (fixed gain stage), they are used as a linearization technique. By controlling the body voltage of M_9 and M_{10}, a very wide range dB-linear gain variation can be obtained.

Typically, a VGA provides very high gain such that a small amount of DC mismatch will cause a serious problem in the following stages. With the direct conversion receiver, DC offset is the most critical issue. Therefore, a DC offset circuit is absolutely needed. The DC offset cancellation circuit is shown in Fig. 13, in which transistors M_1 and M_2 function as high value resistors. These resistors, together with the capacitors C_1 and C_2, create a low-pass filter characteristic. A low-frequency signal is filtered and applied to the gates of a differential pair, formed by M_3 and M_4. They are amplified and fed back to the output of the first stage to cancel the DC offset signal. As mentioned in [8], the BER performance of the receiver will be affected by the cut-off frequency of the DC offset feedback loop. Therefore, the controllable cut-off frequency function in the DC offset circuit should be provided to avoid process variations. In Fig. 13, the cut-off frequency is controlled by changing the gate-source voltage of M_1 and M_2. Figure 14 shows the simulated results of the VGA circuit incorporated with the DC offset circuit under various cut-off frequency levels. In this work, the cut-off frequency in the DC offset feedback loop is set to be lower than 30 kHz.

IV. Experimental Results and Discussion

The proposed transceiver was fabricated using 0.18 μm

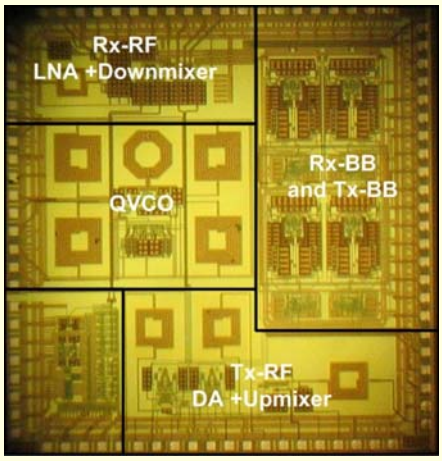

Fig. 15. Microphotograph of the implemented transceiver.

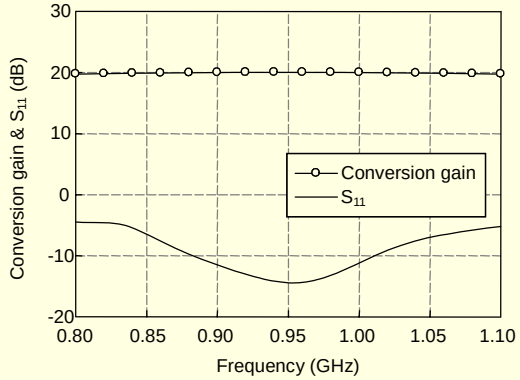

Fig. 16. Measured input return loss and conversion gain of RF receiver front end.

CMOS technology with on-chip ESD protection. A microphotograph of the proposed transceiver, which has an area of 10 mm^2, is shown in Fig. 15.

The measurements were taken as chip-on board (COB). The testing board was built by directly bonding the die onto a two-layer FR4 substrate. Figure 16 shows the measured voltage conversion gain and input return loss, S_{11}, of the RF receiver front end (Rx-RF) sweeping the local oscillator frequency across the entire target band (902 MHz to 928 MHz). Figure 15 shows that the input return loss of Rx-RF is lower than -14 dB, and the voltage conversion gain is about 20 dB and almost flat in whole operating frequency band.

The minimum frequency of the NF meter is 10 MHz. Therefore, in order to measure the noise of the Rx-RF at a low frequency, a spectrum analyzer must be used. The Rx-RF NF was measured with the aid of a spectrum analyzer. A detailed description of this technique is given in [26]. The measured NF result is shown in Fig. 17. It is about 2.5 dB at the center of the band and 3.5 at 10 kHz. Considering the 30 kHz cut-off

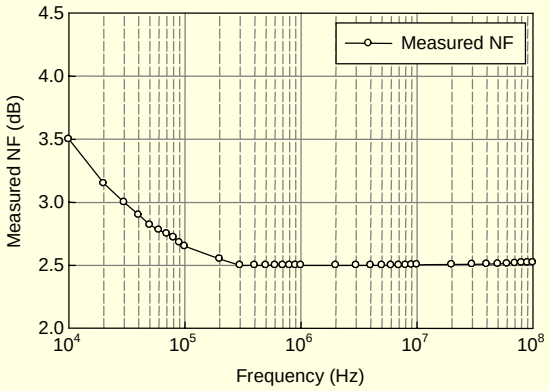

Fig. 17. Measured NF of RF receiver front end.

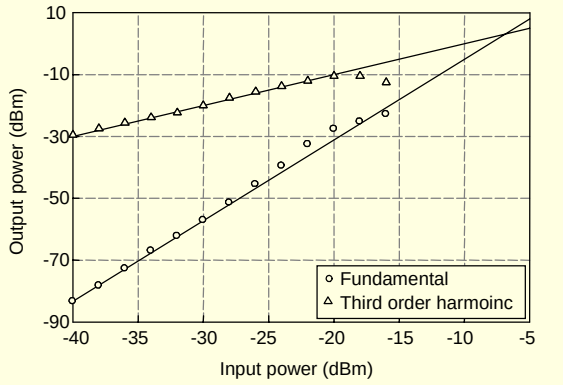

Fig. 18. Measured IIP3 of RF receiver front end.

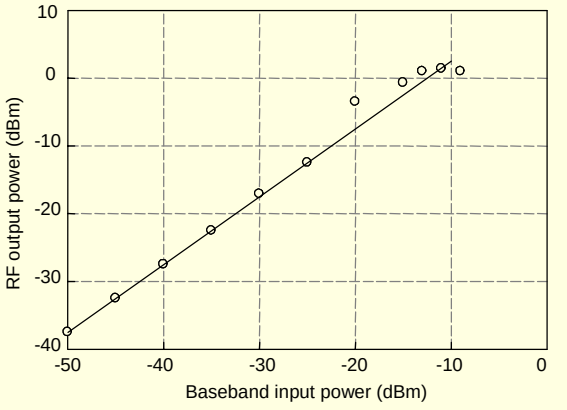

Fig. 19. Measured output 1 dB compression point of RF transmitter front end.

frequency of the DC-offset loop, we can conclude that the implemented Rx-RF front end achieves excellent noise performance.

Figure 18 shows the measured IIP_3 result of the Rx-RF which is about -8 dBm when two-tone signals spaced by 500 kHz were applied.

The Tx-RF front end measurements were performed by

applying 915 MHz LO frequency and 600 kHz baseband input signal. At the input of Tx-RF, a hand-made transformer should be used to convert a single-ended signal generated by the signal generator to a differential one since the minimum frequency of a commercial transformer is about 1.5 MHz. Figures 19 and 20 show the measured output 1 dB compression point (OP 1dB) and output third-order intermodulation (OIP3) of the Tx-RF front end. The obtained results were 2 dBm for OP 1dB and 8 dBm for OIP3.

Figure 21 shows the measured PN and spectrum of the implemented VCO. The measured PN of the implemented QVCO is -118 dBc/Hz at 1 MHz offset. This result is more than enough for the IEEE 802.15.4b standard. The measured tuning characteristic of the QVCO is shown in Fig. 22. With two-bit word control and the control voltage of the varactor, the implemented QVCO achieves a frequency tuning range from 760 MHz to 1,000 MHz. The measured tuning range is about 50 MHz lower than that of the simulation. However, this obtained tuning range is still sufficient over the operation frequency of the IEEE 802.15.4b standard.

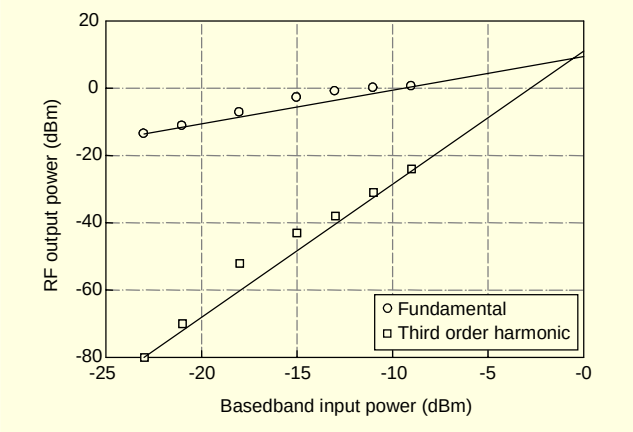

Fig. 20. Measured OIP3 of RF transmitter front end.

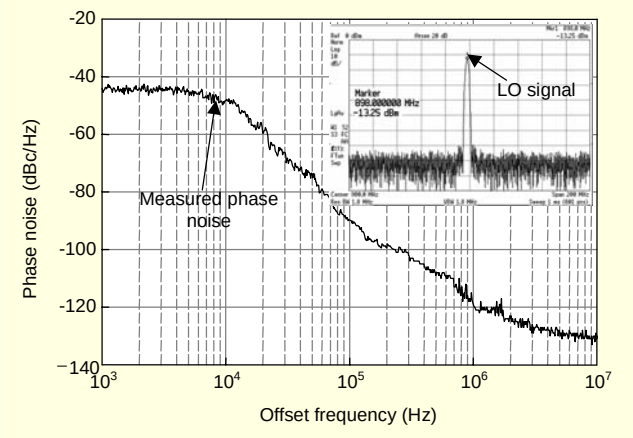

Fig. 21. Measured phase noise of QVCO.

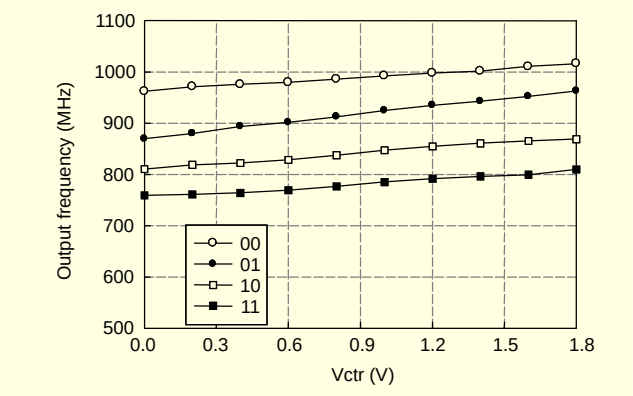

Fig. 22. Measured tuning range of QVCO.

Fig. 23. Measured gain control characteristic of analog baseband section in (a) receive mode and (b) transmit mode.

Figure 23 shows the measured gain variation characteristic of the analog baseband section operating in receive (a) and transmit (b) mode. As shown in Fig. 23, the analog baseband section can provide up to 120 dB and 60 dB dynamic control range for the receiver and transmitter, respectively.

The measured results of the whole receiver and the transmitter chain were also performed. In the receiver chain measurement, the input RF frequency was fixed at 915 MHz while the LO frequency was swept such that the output

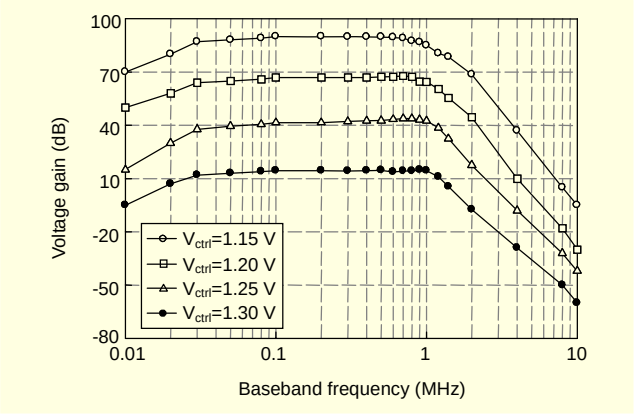

Fig. 24. Measured frequency response of receiver chain with various gain control levels.

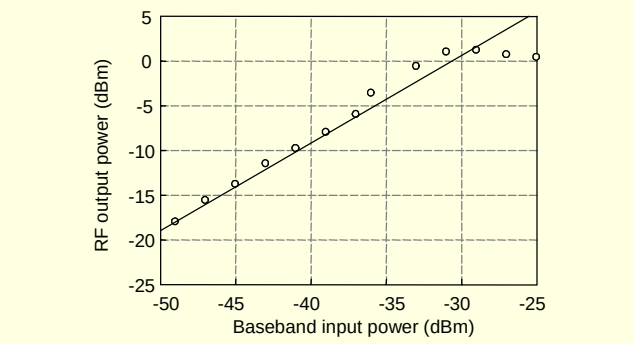

Fig. 25. Measured output 1 dB compression point of transmitter chain.

baseband frequency was in the range of 10 kHz to 10 MHz.

For this measurement, the hand-made transformer was wired with the ratio of 3.5:1 since our receiver would be expected to operate with 5 kΩ loading. The loss of this transformer, which was obtained from its measurement, has been compensated in the receiver chain measurement. The receiver can provide more than 85 dB voltage conversion as shown in Fig. 24. In the transmitter chain measurement, again, the handmade transformer is used at the input of the transmitter. The measured OP 1dB is shown in Fig. 24. The maximum transmit output power of 0 dBm can be achieved. The overall measured performance of the modules and transceiver is summarized in Table 5. The overall NF of the receiver is about 19 dB. In the simulation, the very low-frequency noise (below 1/f noise corner frequency) and the overall NF of the receiver are significantly degraded by the Rx-BB because the passive mixer shows conversion loss. However, this NF value is in agreement with the target specifications.

V. Conclusion

In this paper, a low-power low-cost direct conversion transceiver for the 915 MHz band IEEE 802.15.4b standard was presented, and the system specifications for the 915 MHz band IEEE 802.15.14b standard were derived. Then, the specifications for each individual module in the transceiver were assigned. The proposed transceiver uses a direct conversion scheme with a shared analog baseband section for both the receiver and transmitter. In the receiver chain, with the main goal of low-power and low 1/f noise, a single-ended LNA followed by a balance passive mixer was applied. In the transmitter chain, power consumption was kept as low as possible by using a single-ended driver amplifier. The upconversion mixer was designed using the on-chip LO leakage cancellation technique. Quadrature LO signals were generated by using a differential LC VCO operating at double the frequency of the desired signal and a digital divide-by-2 circuit. The RF receiver front end achieved very good noise performance. The proposed transceiver was fabricated using 0.18 μm CMOS technology with a supply voltage of 1.8 V. The whole receiver chain showed more than 85 dB conversion gain with a dynamic range of 120 dB and dissipated 6.2 mA. In the transmitter chain, 0 dBm transmit power and 8 dBm OIP3 were obtained. The transmitter dissipated 17.5 mA. The QVCO showed a phase noise of -118 dBc/Hz at 1 MHz offset with a frequency tuning range from 760 MHz to 1,000 MHz. The transceiver occupies 10 mm^2 of silicon area.

Table 5. Summary of transceiver performances.

Items	Parameter		Target specifications	This work
Receiver	NF (dB)		19.5	19
	Voltage gain (dB)		85	> 85
	IIP3 (dBm)	@ high gain	-35	-33
		@ low gain	-10	-6
	IIP2 (dBm)		12.5	> 30
	Input P-1dB (dBm)		-20	-15
	Gain control range (dB)		72	100
	Current consumption (mA)		< 10	6.2
Transmitter	Output power (dBm)		0	0
	Power gain		20	32
	OP 1dB (dBm)		2	2
	LO leakage (dB)		NA	29
	Current dissipation (mA)		< 20	17.5
QVCO	PN (dBc/Hz) @ 2MHz		-78	< -120
	Tuning range (MHz)		920 - 928	760 - 1000
	Current dissipation (mA)		< 10	5

All the target specifications include 5 dB implementation margins.

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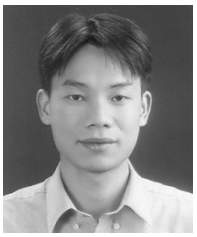

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