Light Effects on the Bias Stability of Transparent ZnO Thin Film Transistors

Jae-Heon Shin, Ji-Su Lee, Chi-Sun Hwang, Sang-Hee Ko Park, Woo-Seok Cheong, Minki Ryu, Chun-Won Byun, Jeong-Ik Lee, and Hye Yong Chu

ABSTRACT—We report on the bias stability characteristics of transparent ZnO thin film transistors (TFTs) under visible light illumination. The transfer curve shows virtually no change under positive gate bias stress with light illumination, while it shows dramatic negative shifts under negative gate bias stress. The major mechanism of the bias stability under visible illumination of our ZnO TFTs is thought to be the charge trapping of photo-generated holes at the gate insulator and/or insulator/channel interface.

Keywords—ZnO, transparent oxide semiconductor, thin film transistor (TFT), bias stability, light effect.

I. Introduction

Oxide-based thin film transistors (TFTs) such as ZnO and InGaZnO (IGZO) have attracted much attention for their possible applications to flat, flexible, and transparent display devices [1]-[4]. Having good stability and large-area uniformity, oxide TFTs are more suitable for application to active matrix organic light emitting display (AM-OLED) panels than a-Si:H and poly-Si counterparts [4]. In general, the stability of TFTs under gate bias stress is of crucial importance for their application. Oxide TFTs have an additional issue of light stability because of their unique transparent circuit application. A few studies on the bias stability of oxide TFTs have been reported very recently [5], [6]. Fewer studies on the influence of visible light on oxide TFTs without any electrical biases have also been reported [7]. However, the stability of oxide TFTs under simultaneous application of light and bias has not been reported yet. Since switching and driving TFTs in transparent AM-OLED panels always operate under the illumination of OLED and environmental lights, systematic studies on the effects of light on the bias stability of transparent oxide TFTs under real operating conditions are very important for actual transparent panel applications. In this work, we report on the gate bias stability characteristics of transparent ZnO TFTs under visible light illumination. The possible mechanisms of light induced bias instability in our ZnO TFTs are also discussed.

II. Experiments

A top gate staggered structure and an ITO/glass substrate were employed in the fabrication of a ZnO TFT. A 130 nm thick ITO layer was patterned for source and drain electrodes. A 20 nm thick ZnO layer and a 9 nm thick first gate insulator, alumina, were deposited continuously at 200°C by plasma enhanced atomic layer deposition (PEALD) using diethylzinc and ALD using trimethylaluminum (TMA), respectively. After wet etching the first gate insulator and the ZnO layer, a 160 nm thick second gate insulator, alumina, was deposited by ALD using TMA as the source gas. Finally, a 100 nm thick ITO layer was deposited by sputtering and patterned for the gate electrode.

A bias stress test and I_D-V_G measurement were done using an Agilent B1500A parameter analyzer with a dark probe box system. Samples were located inside the dark box blocking external light. The noise current level of the instrument ranges from 0.1 pA to 1 pA. The gate bias stress test was done in three different modes: on state (V_{G_ST} = 10 V), weak off state

Manuscript received Aug. 28, 2008; revised Nov. 17, 2008; accepted Dec. 11, 2008.

This work was supported by IT R&D Program of MKE (2006-S079-02, Smart Window with Transparent Electronic Devices), Rep. of Korea.

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(V_{G_ST}=-3 V), and strong off state (V_{G_ST}=-10 V). The strong off state of V_{G_ST}=-10 V was chosen for practically simulating the switching transistors (sw-TRs) in the AM-OLED panel pixels. This is because all the sw-TRs are always in a negative gate bias state between short positive gate-line pulses. Each gate bias stress was carried out up to 46,000 s (about 12 h). A green light source (λ_{peak}, about 540 nm) of a tungsten-halogen lamp and a band-pass filter (515 to 555 nm) was chosen for the visible light source and located in the dark box for illumination.

III. Results

Figures 1(a) and (b) show the changes of the transfer characteristics of ZnO TFTs under a 10 V gate bias stress condition with illumination power density (P_{ill}) of 0 and 1 mW/cm^2, respectively. The sub-threshold slope is about 0.5 V/dec, and the mobility at V_G=20 V is about 5 cm^2/Vs. Without light, as seen in Fig. 1(a), the I_D-V_G transfer curve shows a parallel shift in a positive direction while keeping its shape. It is well known that the transfer curve of a-Si:H TFTs shifts in a positive direction under positive gate bias stress because of defect state generation or electron trapping near the gate insulator interface [8]. In general, the state creation is accompanied by change in the sub-threshold slope and mobility while the charge trapping is not [5]. Therefore, the instability of our ZnO TFTs under positive gate bias stress can be explained by the mechanism of electron trapping at the gate insulator and/or interface. With light illumination, the transfer curve can be expected to move more rapidly in a positive direction because of the accelerated charge trapping by photo-generated carriers as observed in organic TFTs [9]. However, the transfer curve under light illumination (Fig. 1(b)) shows less movement than that without light (Fig. 1(a)). To find the reason for this somewhat strange behavior, we measured the transfer curves under -10 V gate bias stress with and without light illumination as shown in Figs. 1(c) and (d). The transfer curve without light (Fig. 1(c)) shows virtually no change (very little shift in a negative direction) while the transfer curve with light shows a dramatic parallel shift in a negative direction (Fig. 1(d)). We think that the main mechanism of this dramatic behavior could be related to the charge trapping of photo-generated holes at the gate insulator and/or interface. Since n-type oxide semiconductors have negligible holes in their valence bands, hole trapping at the gate insulator or interface would be negligible even under negative gate field stress. However, abundant holes can be generated in valence bands by light illumination because of electron transitions via mid-gap states. Therefore, many generated free holes drift toward the gate insulator and are trapped under negative gate bias yielding a dramatic negative shift of the transfer curve as seen in Fig. 1(d).

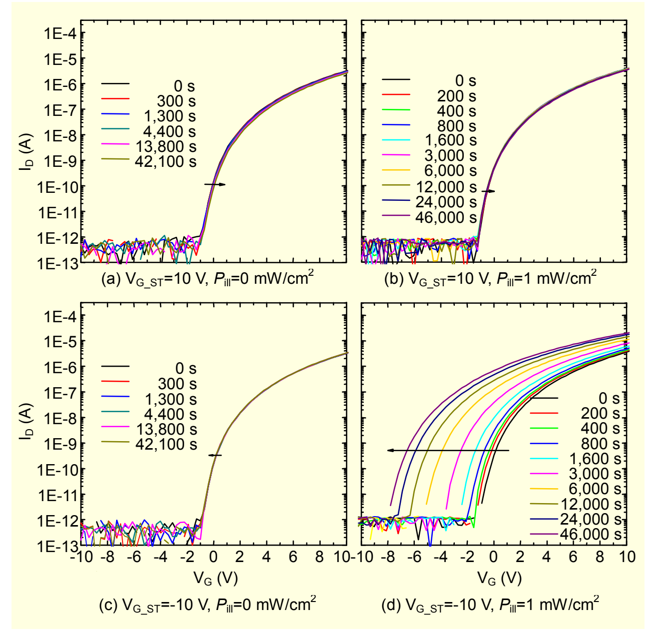

Fig. 1. Changes in the I_D-V_G characteristics of ZnO TFTs (W/L = 40 μm/20 μm) under 10 V gate bias stress with (a) P_{ill} of 0 mW/cm^2 and (b) 1.0 mW/cm^2 and under -10 V gate bias stress with (c) P_{ill} of 0 mW/cm^2 and (d) 1.0 mW/cm^2. V_D is 15 V during the V_G sweep.

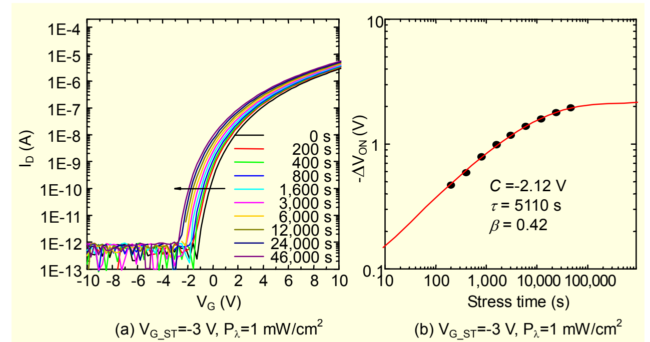

Fig. 2. (a) Changes in the I_D-V_G characteristics of ZnO TFTs (W/L = 40 μm/20 μm) under –3 V gate bias stress with light intensity of 1 mW/cm^2 and (b) ΔV_{on} vs. stress time in log scale (circles: experiments, line: theoretical calculation).

On the contrary, under positive gate bias, the positive gate field repels most of the photo-generated holes away from the gate insulator resulting in negligible hole trapping (Fig. 1 (b)).

Figure 2(a) shows the changes in the transfer characteristics of ZnO TFTs under -3 V gate bias stress condition with light (1 mW/cm^2). A less dramatic negative shift of the transfer curve is seen as well as the saturation behavior of turn-on voltage (V_{on}) around -3 V. Figure 2(b) shows the changes in V_{on} (ΔV_{on}) versus stress time in log scale. The solid line represents the theoretical calculations based on the well-accepted stretched exponential model for the charge trapping

kinetics in a-Si:H TFTs [9],

$$\Delta V_{\text{on}} = C[1 - \exp\{-(\frac{t}{\tau})^{\beta}\}], \quad (1)$$

where C, τ, and β are the fitting parameters. The obtained C, τ, and β values are -2.12 V, 5110 s, and 0.42, respectively. As seen in Fig. 2(b), the stretched-exponential function based on the charge trapping model excellently fits the data, which also supports the hole-trapping mechanism suggested in this work. The predicted saturation value of V_{on} from Figs. 2(a) and (b) is about -3.12 V, which is nearly equal to the applied gate bias stress voltage of -3 V. In general, the V_{on} voltage is very close to the flat band voltage (V_{FB}) [10]. Therefore, if V_{on} (i.e., V_{FB}) is negative compared to the gate bias voltage, the gate bias would start to act as a positive field prohibiting hole trapping at the gate insulator, which would result in the saturation of V_{on} as seen in Fig. 2(b).

Figure 3(a) shows ΔV_{on} versus stress time t when the TFTs are biased in the strong off state (V_{G_ST} = -10 V) during illumination with P_{ill} between 0 mW/cm^2 and 2.6 mW/cm^2. All the data are well fitted by a unified stretched exponential function based on the light-induced charge trapping model [9],

$$\Delta V_{\text{on}} = C[1 - \exp\{-(\frac{t(1+\eta P_{\text{ill}})}{\tau})^{\beta}\}], \quad (2)$$

where η is an efficiency factor determining the acceleration of ΔV_{on} by means of illumination and is chosen to achieve an optimal overlap in a ΔV_{on} versus $t(1+\eta P_{ill})$ plot as shown in Fig. 3(b). The obtained η, C, τ, and β parameters are 800 cm^2/mW, -7.2 V, 5.3×10^6 s, and 0.83, respectively. The excellent fit between experiment and theory based on the charge trapping model also supports the mechanism of photo-generated hole trapping suggested in this work. The predicted saturation value of V_{on} from Fig. 3 is about -8.2 V, which is still positive compared to the gate bias voltage (-10 V). Therefore, in this case, the V_{on} is not saturated due to the change of the gate field polarity. Rather, it could be saturated due to the complete depletion of hole-trap centers in the gate insulator and interface. We think that the ALD-grown alumina gate insulator may have hole-trap centers much more than electron-trap centers. For more evidence, however, light and bias stress experiments will be conducted in future work for various oxide-based TFTs having gate insulator of various materials and structures.

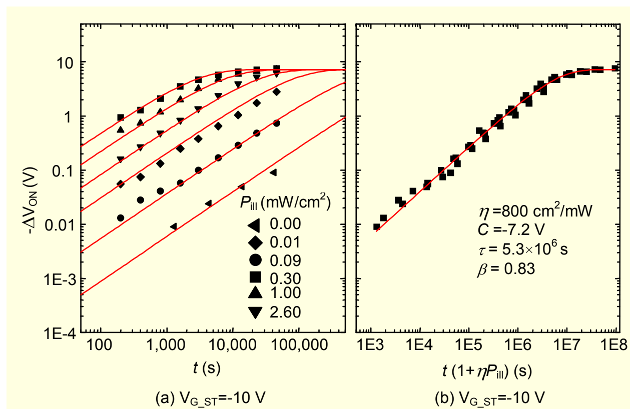

Fig. 3. ΔV_{on} vs. stress time (a) and unified stress time $t(1+\eta P_{ill})$ (b), when the ZnO TFTs (W/L=40 μm/20 μm) are biased in the strong off state (V_{G_ST}=-10 V) during illumination with P_{ill} of 0 to 2.6 mW/cm^2 (Lines are theoretical calculations).

IV. Conclusion

The bias stability characteristics of transparent ZnO TFTs under visible light illumination were studied for the first time in this work. The transfer curve shows virtually no change under positive V_G stress with light illumination of 1 mW/cm^2, while it shows dramatic negative shifts under negative V_G stress. The major mechanism of bias instability under visible illumination of our ZnO TFTs is thought to be the charge trapping of photo-generated holes rather than defect state creation.

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