

Low Voltage CMOS LC VCO with Switched Self-Biasing

Byung-Hun Min, Seok-Bong Hyun, and Hyun-Kyu Yu

This paper presents a switched self-biasing and a tail current-shaping technique to suppress the $1/f$ noise from a tail current source in differential cross-coupled inductance-capacitance (LC) voltage-controlled oscillators (VCOs). The proposed LC VCO has an amplitude control characteristic due to the creation of negative feedback for the oscillation waveform amplitude. It is fabricated using a $0.13\ \mu\text{m}$ CMOS process. The measured phase noise is $-117\ \text{dBc/Hz}$ at a 1 MHz offset from a 4.85 GHz carrier frequency, while it draws 6.5 mA from a 0.6 V supply voltage. For frequency tuning, process variation, and temperature change, the amplitude change rate of the oscillation waveform in the proposed VCO is 2.1 to 3.2 times smaller than that of an existing VCO with a fixed bias. The measured amplitude change rate of the oscillation waveform for frequency tuning from 4.55 GHz to 5.04 GHz is $131\ \text{pV/Hz}$.

Keywords: Switched biasing, $1/f$ noise, amplitude control, tail current-shaping, VCO, CMOS.

I. Introduction

Regarding the improvement of phase noise characteristics in conventional inductance-capacitance (LC) voltage-controlled oscillators (VCOs) with a differential cross-coupled pair, many studies have been advanced. Among these studies, methodologies for suppressing the flicker noise from a tail current source have been reported [1]-[5]. Hajimiri first explained $1/f$ noise upconversion effects in an oscillator and revealed that the symmetry in the oscillator waveform can help to minimize the upconversion [1]. Next, Hegazi and others proposed a filtering technique that suppresses the upconversion of flicker noise by inserting a passive LC filter to resonate at twice the oscillation frequency between the tail current and the LC tank [2]. Their measurement results also showed that the phase noise of the proposed VCO with filter was about 7 dB better than that of a VCO with no filter. In addition, various methods, such as a bias current shaping technique, flicker noise upconversion minimization technique, and exploitation of the vertical-NPN transistor as a tail current source in the CMOS process have been reported [3]-[5].

It was also revealed that the switching of the tail current source by applying a sine or square wave can reduce $1/f$ noise itself; that is, cycling a MOS transistor between strong inversion and accumulation has a reduction effect on $1/f$ noise [6]-[10]. Oscillator circuits are suitable for applying a switched biasing technique in that they can use an oscillation waveform for the switching of the tail current source.

This paper presents a new bias scheme based on switched biasing and a current shaping technique in order to suppress the $1/f$ noise of the tail current source in a cross-coupled differential LC VCO circuit. It also has the amplitude control characteristics of an oscillation waveform through self-biasing.

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This helps create a stable oscillation condition for process variation, temperature change, and frequency tuning.

This paper is organized as follows. Section II describes the proposed LC VCO topology based on switched self-biasing, and section III explains the advantages of this structure, such as a flicker noise reduction effect and amplitude control characteristics. Section IV shows the experimental results, and conclusions are given in section V.

II. LC VCO Structure with Switched Self-Biasing

The switched biasing technique has been studied as a method to reduce flicker noise [6]-[10]. Figure 1(a) shows a fixed bias with a constant voltage of V_B , and Fig. 1(b) demonstrates a switched biasing structure applying a sine waveform. It is assumed that the common mode voltage of this waveform is the threshold voltage (V_{th}) of an NMOS transistor for an on-off operation of duty 50%. During the half period when the switching waveform is higher than the threshold voltage, the NMOS transistor enters into the saturation or linear region. However, at the opposite half period of the former, it is in the cut-off region. A MOS transistor cycles from cut-off region to linear region in one period.

Generally, it has been known that flicker noise is generated by the carrier trapping in localized oxide states [10]. Switching a MOS transistor will force the release of captured electrons or holes from a trap. The higher the frequency of a switching waveform is, the smaller the flicker noise will be. Up to now, the switched biasing technique has been applied to oscillator circuits including sawtooth oscillators, ring oscillators, and LC oscillators [10]-[12]. According to [10] and [11], the phase noise characteristic of an oscillator with switched biasing has been reported to be reduced by 8 dB compared with a fixed bias.

However, the switched biasing of Fig. 1(b) is difficult to

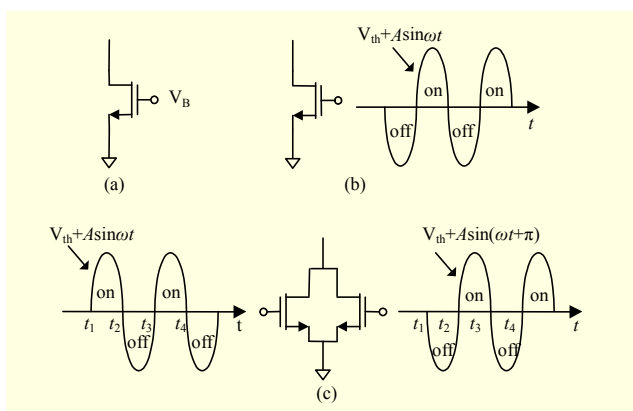


Fig. 1. Bias methods: (a) a fixed bias, (b) switched biasing, and (c) complementary switched biasing.

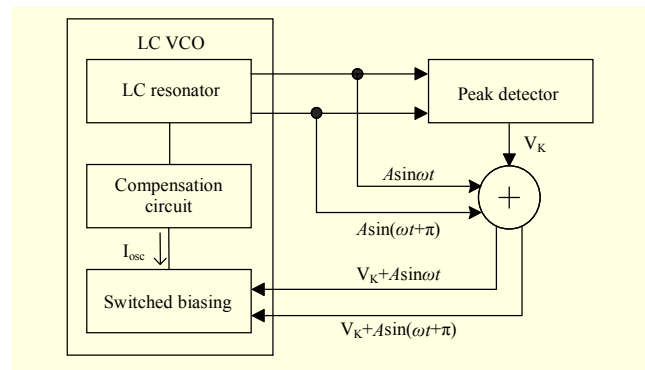


Fig. 2. LC VCO topology with switched self-biasing.

apply to a differential cross-coupled LC VCO structure because the bias current does not draw during the half period of the switching time. Figure 1(c) shows the complementary switched biasing to draw the current continuously. Complementary ON-OFF operations between two transistors are possible by applying differential signals such as $V_{th} + A \sin(\omega t)$ and $V_{th} + A \sin(\omega t + \pi)$.

Using the bias scheme of Fig. 1(c), the proposed LC VCO topology is shown in Fig. 2, where two differential outputs of the LC VCO are denoted by $A \sin(\omega t)$ and $A \sin(\omega t + \pi)$, and the detected values of the peak detector and bias current of the LC VCO are denoted by V_K and I_{osc} , respectively.

The proposed LC VCO structure with switched biasing is composed of two parts: an LC VCO consisting of an LC resonator, compensation circuit, and switched bias circuit as well as a peak detector. The peak detector detects the peak value from the differential outputs of the LC VCO, and the detected voltage (V_K) is used as the common mode voltage of switching waveforms for switching the bias circuit of the LC VCO. The switching waveforms are obtained from two oscillating waveforms of the LC VCO. In this structure, the amplitude control loop of the oscillation waveform is formed by the circuit blocks of the LC VCO and the peak detector. The detailed operation principles are explained using an example of a practical circuit in the next section.

III. Advantages of the LC VCO with Switched Self-Biasing

Figure 3 shows an example of a practical circuit of the proposed VCO structure. It has two characteristics, namely, switched biasing to suppress the flicker noise from the tail current source, and self-control of the amplitude of the oscillation waveform.

The operation steps of switched biasing proceed as follows. Two differential output nodes (Q_1 and Q_2) of the LC VCO with n -core and n -tail are connected to a peak detector that is

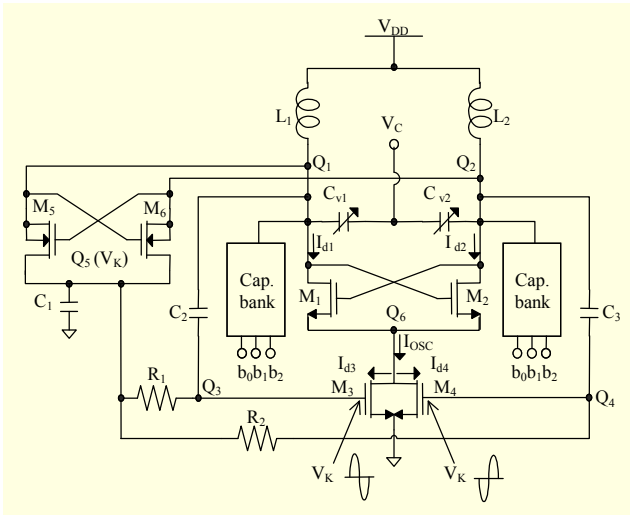


Fig. 3. LC VCO circuit with switched self-biasing.

composed of M_5 , M_6 , and C_1 . The peak detector detects the negative peak of the oscillation waveform, and its output voltage (V_K) is applied in a bias circuit that consists of M_3 and M_4 . M_3 and M_4 have a switched biasing operation carried out by receiving differential oscillation signals through the AC coupling capacitors C_2 and C_3 on the common mode voltage of V_K , where the operation principle of the peak detector is carried out as follows [13]. When Q_1 in the differential oscillation nodes is high and Q_2 is low, M_5 is off, and M_6 is on. Also, M_6 charges C_1 to the negative peak value of the oscillation waveform. In the opposite situation, M_5 is on, M_6 is off, and M_5 charges C_1 to a negative peak value. Through the periodic ON-OFF operation of M_5 and M_6 , the negative peak value of the oscillation waveform is detected. This has an advantage in that the peak detector of this type does not dissipate the DC current.

The operation principle for self-biasing is based on negative feedback. If the amplitude of an oscillating waveform is increased by an external condition such as frequency tuning or PVT variation, the DC output value (V_K) of the peak detector that detects a negative peak will descend toward the ground voltage. It will also decrease the bias current (I_{osc}) due to the reduction of the common mode voltage of the switched biasing. Therefore, the amplitude of the oscillation waveform returns again. This feedback loop for an oscillating waveform helps to stabilize the amplitude characteristics of the LC VCO.

1. $1/f$ Noise Suppressing Effect

The flicker noise from a tail current source is an important issue that is associated with the close-in phase noise in an LC VCO design. The proposed LC VCO is conducive to the application of the current shaping technique for suppressing flicker noise. The tail current shaping technique was proposed

by Soltanian and Kinget, and is based on Hajimiri's theory [1], [3]. According to this theory, the sensitivity of the output phase noise to an injected noise is largest at the zero-crossings of two differential oscillating outputs, and it is smallest when the oscillating outputs reach their maximum or minimum values.

Therefore, a tail current circuit is designed such that its current has its smallest value at zero-crossings and its largest value at the maximum or minimum peak of oscillating output. This tail current shaping technique was implemented by attaching a capacitor in parallel with the tail transistor [3]. However, the capacitance must be optimized to align the phase between the tail current and oscillation waveforms, and the process variation of this capacitor must also be considered. The proposed LC VCO structure is conducive to aligning the phase between the tail current and oscillating waveforms. This is obtained by a design in which the common-mode voltage (V_K) at nodes Q_3 and Q_4 is lower than the threshold voltage of the tail transistors (M_3 or M_4).

Two oscillating waveforms can be expressed as $V_{DD} + A \sin(\omega_0 t)$ and $V_{DD} + A \sin(\omega_0 t + \pi)$. From these, the negative detected value (V_K) of the peak detector is obtained:

$$V_K = V_{DD} - A. \quad (1)$$

The two switching waveforms that drive the tail transistors at nodes Q_3 and Q_4 can be expressed as

$$\begin{aligned} V_{Q3} &= V_K + A \sin(\omega_0 t), \\ V_{Q4} &= V_K + A \sin(\omega_0 t + \pi), \end{aligned} \quad (2)$$

where ω_0 and π indicate the oscillating angle frequency and phase in radian, respectively.

Assume that the common mode voltage (V_K) of the switching waveform is lower than the threshold voltage of the tail transistors (M_3 or M_4). When Q_1 is high and Q_2 is low, M_2 and M_3 are on, and M_1 and M_4 are off. In the opposite situation, M_2 and M_3 are off, and M_1 and M_4 are on. Due to the same switching operation, the current flowing into M_1 during the first half period of the oscillating waveform flows out of M_4 , and the current flowing into M_2 in the second half period flows out of M_3 . Therefore, we obtain

$$I_{d1} \approx I_{d4} \quad \text{and} \quad I_{d2} \approx I_{d3} \quad \text{if} \quad V_K \leq V_{thb}, \quad (3)$$

where I_{d1} , I_{d2} , I_{d3} , and I_{d4} are the current flowing into the drains of M_1 , M_2 , M_3 , and M_4 , and V_{thb} is the threshold voltage of M_3 or M_4 .

Figure 4 shows the voltage and current waveforms for variations of V_K . Assume that M_1 , M_2 , M_3 , and M_4 are ideal switches; then, a square-wave current is generated by the ideal switching operation.

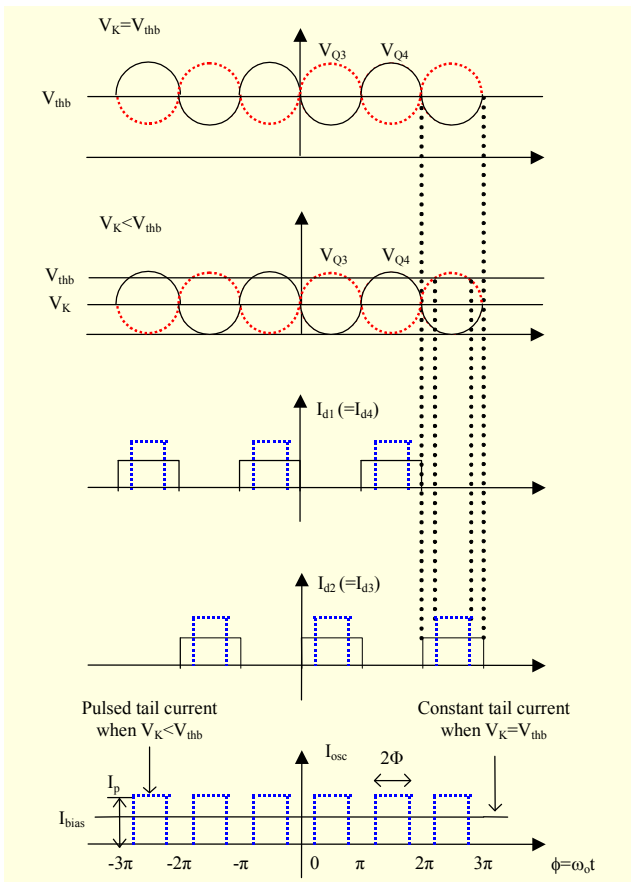


Fig. 4. Voltage and current waveforms for the variation of V_K .

In the case of $V_K > V_{thb}$, the approximations in (3) do not hold because tail transistors M_3 and M_4 have a switching operation time of more than half the period of the oscillating waveform.

In the case of $V_K < V_{thb}$, and the tail current (I_{osc}) values at the zero-crossings of two oscillating waveforms are zero while those at maximum or minimum have the maximum value. We can know that tail-current shaping is performed by the switched biasing of the tail transistors.

In addition, the current bias of the pulsed form is obtained. When V_K is equal to V_{thb} , M_1 and M_2 (or M_3 and M_4) have a switching operation per half period of the oscillating frequency with 50% duty. In this case, the tail current source is the same as a constant tail current and is defined as I_{bias} in (4), whereas when V_K is lower than V_{thb} , the tail current source has a pulsed form as shown in Fig. 4. We can define a pulsed tail current that has a conduction angle and amplitude of 2Φ and I_p , respectively. From this, the tail current for the switched biasing is expressed as

$$I_{osc} = \begin{cases} I_{bias}, & V_K = V_{thb}, \\ I_p \sum_{n=-\infty}^{\infty} \prod \left(\frac{\phi - n\pi}{2\Phi} \right), & V_K < V_{thb}. \end{cases} \quad (4)$$

Through a Fourier expansion in the pulsed tail current of (4), the amplitude of the oscillating waveform is obtained, as given in [3], by

$$A = \frac{1}{\Phi} I_{bias} R_t \sin(\Phi), \quad 0 < \Phi \leq \frac{\pi}{2}, \quad (5)$$

where R_t is the impedance of an LC tank, and I_{bias} is equal to $I_p(2\Phi/\pi)$ and is the common mode level of the pulsed tail current [3].

The conduction angle at a constant tail current is $\pi/2$, and its amplitude is equal to $(2/\pi)I_{bias}R_t$ from (5), whereas when the half of one period at the pulsed bias current is switched, the conduction angle is $\pi/4$, and its amplitude from (5) is increased by more than 1.4 times (40%) compared to that at a constant tail current. A pulsed tail current has an advantage over a constant bias in that the amplitude of the oscillation waveform is increased under the same power dissipation.

It is important to set V_K lower than V_{thb} in order to obtain the pulsed tail current effect and the current-shaping characteristics. The common mode level (I_{bias}) of the pulsed tail current is obtained by the product of the common-mode voltage (V_K) of the switched waveforms and the transconductance (g_{mb}) of the tail transistor (M_3 or M_4):

$$I_{bias} = V_K g_{mb}. \quad (6)$$

When arranging for the amplitude of the oscillating waveform in (1), (5), and (6), we can obtain (7), where A_{fb} means the amplitude of the oscillating waveform through the feedback loop of the proposed LC VCO. Also, (8) and (9) are obtained by arranging for V_K and I_{bias} using the same method, respectively.

$$A_{fb} = \frac{g_{mb} R_t V_{DD} \sin(\Phi)}{\Phi + g_{mb} R_t \sin(\Phi)}, \quad (7)$$

$$V_K = \frac{V_{DD}}{1 + \frac{1}{\Phi} g_{mb} R_t \sin(\Phi)}, \quad (8)$$

$$I_{bias} = \frac{V_{DD}}{\frac{1}{g_{mb}} + \frac{1}{\Phi} R_t \sin(\Phi)}. \quad (9)$$

We can simulate variations of V_K , I_{bias} , and A_{fb} by changing g_{mb} . The supply voltage of the LC oscillator is fixed at 0.6 V. The simulation results for when g_{mb} is increased from 12 mA/V to 22.6 mA/V by adjusting the size of the tail transistors are shown in Table 1.

We can know that I_{bias} and V_K have an inverse proportionality to each other. Lowering V_K improves the phase noise characteristics due to the pulsed bias and current shaping effects,

Table 1. V_K , I_{avg} , and A_{fb} for g_{mb} at 0.6 V of the supply voltage.

g_{mb} (mA/V)	V_K (mV)	I_{bias} (mA)	A_{fb} (mV)
12.00	430	5.162	175
15.00	390	5.860	218
17.43	365	6.376	245
19.10	349	6.675	265
21.08	329	6.947	280
22.57	318	7.179	291

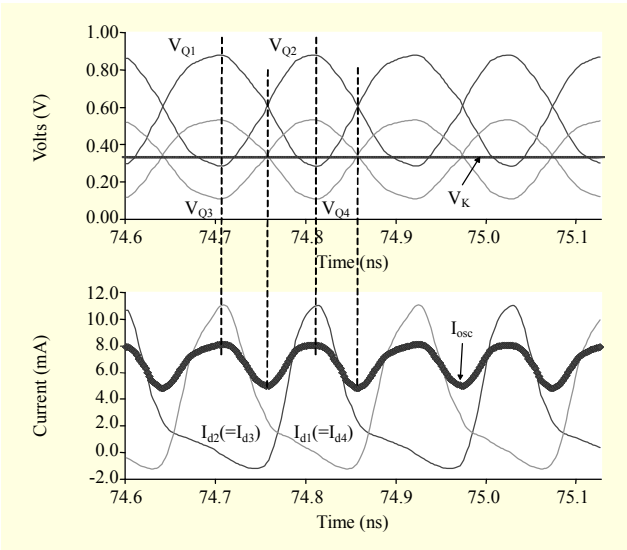


Fig. 5. Simulated voltage and current waveforms with tail current shaping and pulsed tail bias.

but the bias current increases as much as V_K decreases.

Simulated V_K , I_{bias} , and A_{fb} were inserted into (7), (8), and (9) in our design, and the conduction angle was then calculated. We selected the designed values for a conduction angle of almost $\pi/2$.

Figure 5 shows the simulated voltage and current waveforms of the proposed VCO of Table 1 when g_{mb} is 17.43 mA/V. It can be seen that I_{OSC} at the zero-crossings of V_{Q1} and V_{Q2} (or V_{Q3} and V_{Q4}) has the minimum current, and that at the maximum or minimum values of V_{Q1} and V_{Q2} (or V_{Q3} and V_{Q4}) have the maximum current. It can also be seen that the currents of I_{d1} and I_{d2} have a pulsed shape. The phase noise equation in [1] is calculated as

$$L\{\Delta\omega\} = 10 \log_{10} \left(\frac{\Gamma_{rms}^2}{8\pi^2 f_{offset}^2} \frac{\sum \overline{i_n^2} / \Delta f}{q_{max}^2} \right), \quad (10)$$

where q_{max} , Γ_{rms} , $\overline{i_n^2}$, and f_{offset} are the maximum signal charge swing, root mean square value of the impulse sensitivity

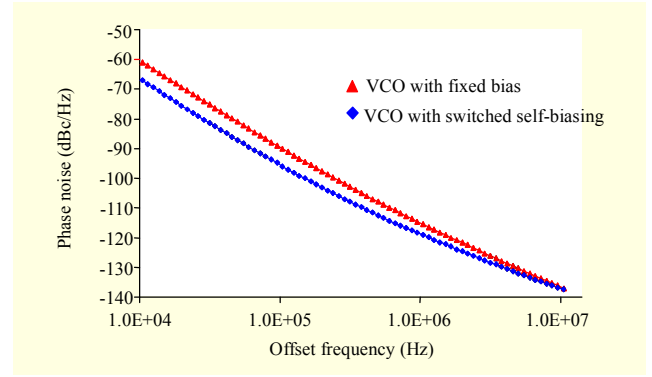


Fig. 6. Simulated phase noise of the VCOs using spectreRF simulation tool.

function, power spectral density of the noise current, and offset frequency from the carrier, respectively.

The phase noise in the proposed LC VCO with switched self-biasing is reduced by three different mechanisms. First, the switched biasing of the tail transistors decreases the intrinsic $1/f$ noise itself of the tail transistors. Second, the tail current-shaping technique using switched self-biasing improves the phase noise by decreasing the flicker noise up-conversion of the tail transistor. Third, the pulsed tail current improves the phase noise by increasing q_{max} in (10).

Figure 6 shows a comparison of the phase noise characteristics between the existing VCO with fixed bias and the proposed VCO with switched self-biasing using a SpectreRF tool under the condition of a same current consumption of 6.37 mA and same carrier frequency of 4.85 GHz. At a low frequency offset lower than 100 kHz, the phase noise characteristics of the proposed VCO is 6 dB lower than that of the existing VCO with a fixed bias.

2. Amplitude Control Effect through Self-Biasing

In the case of an LC VCO design with a wide frequency tuning using a capacitor bank, it is important to verify the oscillation condition for the frequency tuning. In general, the oscillation condition of the LC VCO is defined as

$$g_{mc} > 1/R_t, \quad (11)$$

where g_{mc} indicates the trans-conductance of M_1 (or M_2).

To achieve a stable oscillation operation, we know that the product of g_{mc} and R_t must be larger than unity, and its rate of change for frequency tuning or PVT variation must be smaller. These principles can also be applied to the amplitude of an oscillating waveform that is proportional to the product of I_{bias} and R_t , as g_{mc} is proportional to the square root of I_{bias} .

In the LC VCO design, R_t is the function of frequency, and is generally proportional to ω^2 . Therefore, R_t is set equal to $K\omega^2$,

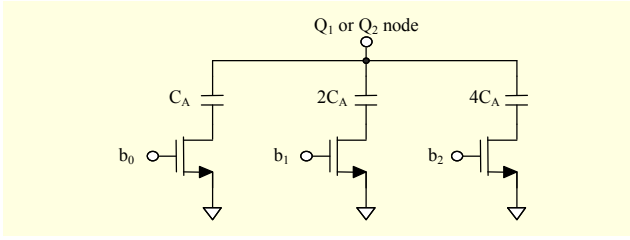


Fig. 7. Capacitor bank for coarse frequency tuning.

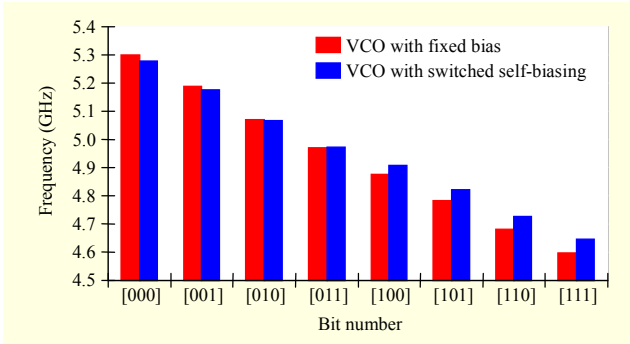


Fig. 8. Simulated coarse frequency tuning characteristics.

where K is a proportional constant. In the case of a fixed bias with tail current shaping, the equation for the amplitude of the oscillation waveform is (5), and its slope for frequency is calculated as

$$\frac{\partial A}{\partial \omega} = \frac{2K\omega I_{\text{bias}} \sin(\Phi)}{\Phi} = \frac{2A}{\omega} \quad (12)$$

On the other hand, the equation for the amplitude of the proposed LC VCO with switched self-biasing is (9), and its slope for frequency is calculated as

$$\begin{aligned} \frac{\partial A_{\text{fb}}}{\partial \omega} &= \frac{\partial A_{\text{fb}}}{\partial R_t} \cdot \frac{\partial R_t}{\partial \omega} = \frac{g_{\text{mb}} V_{\text{DD}} \Phi \sin(\Phi)}{(\Phi + g_{\text{mb}} R_t \sin(\Phi))^2} \cdot \frac{2R_t}{\omega} \\ &= \frac{2A_{\text{fb}}}{\omega} \cdot \frac{\Phi}{\Phi + g_{\text{mb}} R_t \sin(\Phi)}. \end{aligned} \quad (13)$$

Comparing (12) with (13), we can see that the amplitude change rate for frequency tuning in the proposed LC VCO is smaller than that of the LC VCO using a fixed bias. When it is designed so that Φ is equal to $g_{\text{mb}} R_t \sin(\Phi)$, the stability of the amplitude change rate is improved to twice that of the existing VCO.

Figure 7 shows the structure of the capacitor bank for the coarse frequency tuning seen in Fig. 3. The capacitor bank that is connected to the oscillation node can tune the oscillation frequency by adjusting the digital bit number.

Figure 8 shows the simulation results using this capacitor bank for coarse frequency tuning between the existing VCO with a fixed bias and the proposed VCO with switched self-biasing under the condition of the same current consumption of

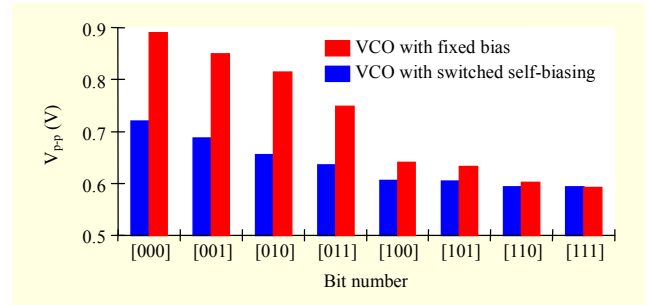


Fig. 9. Simulated amplitude characteristics of oscillating waveform for frequency tuning.

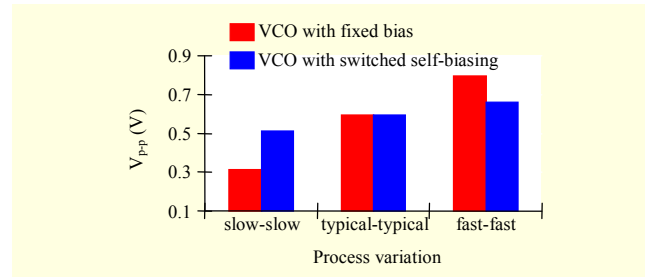


Fig. 10. Simulated amplitude characteristics for process variation.

6.376 mA and the same supply voltage of 0.6 V. The difference for frequency tuning between the existing VCO and the proposed VCO is small. However, the peak-to-peak voltage of the oscillating waveform between the existing and proposed VCOs shows a large difference as seen in Fig. 9.

From the simulated data of Figs. 8 and 9, the change rate ($\partial A / \partial f$) of the amplitude for frequency tuning can be obtained. The existing VCO with fixed bias has a frequency tuning range of 4.597 GHz to 5.301 GHz with a variation of peak-to-peak voltages of 0.593 V to 0.89 V. Its change rate is 211 pV/Hz. On the other hand, the proposed VCO has a tuning range of 4.647 GHz to 5.278 GHz with a variation of peak-to-peak voltages of 0.594 V to 0.72 V. Its change rate is 99.8 pV/Hz. The stability of the amplitude change for frequency tuning of the proposed VCO is improved 2.1 times that of the existing VCO.

Figures 10 and 11 show the simulation results for process variation and temperature change when the binary number of the capacitor bank is 111. In a typical-typical state of process variation, the peak-to-peak voltages between a VCO with fixed bias and VCO with switched self-biasing are nearly the same. However, in the process variation from a slow-slow state to a fast-fast state, the stability of the amplitude change for the process variation of the proposed VCO is 3.2 times better than that of the existing VCO. Also, in terms of temperature change, the stability of the proposed VCO is 2.9 times better than that of the existing VCO. Due to the amplitude control mechanism through the peak detector, the proposed VCO is more stable

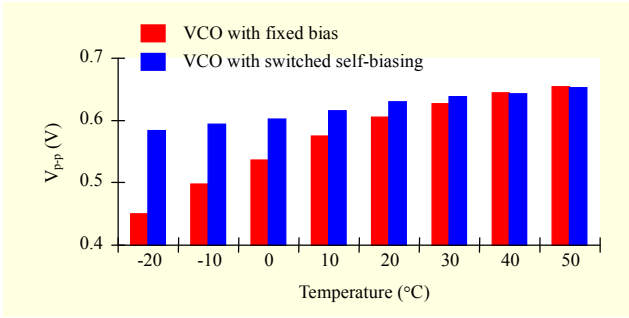


Fig. 11. Simulated amplitude characteristics for temperature change.

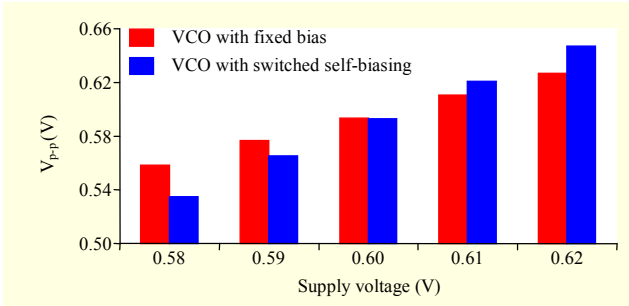


Fig. 12. Simulated amplitude characteristics for the change of supply voltage.

than the existing VCO in terms of frequency tuning, process variation, and temperature change has more stability in the amplitude change of the oscillation waveform.

For the change of supply voltage, the change rate ($\partial A_{fb} / \partial V_{DD}$) of the amplitude in the proposed VCO is calculated as

$$\frac{\partial A_{fb}}{\partial V_{DD}} = \frac{g_{mb} R_t \sin(\Phi)}{\Phi + g_{mb} R_t \sin(\Phi)}. \quad (14)$$

On the other hand, the amplitude slope ($\partial A / \partial V_{DD}$) for the supply voltage of the existing VCO is zero. Therefore, the stability of the amplitude change for the supply voltage of the proposed VCO is worse than that of the existing VCO. Figure 12 shows a comparison.

This problem can be solved by attaching a regulator between the supply voltage and the proposed VCO as shown in Fig. 13. The dotted line in Fig. 13 is the VCO circuit schematic that is included in chip. The regulator block was not implemented in our chip design.

The amplitude change rate of VCO with the amplitude control mechanism is 2.1 to 3.2 times smaller than that of the VCO with fixed bias in terms of frequency tuning, process variation, and temperature change. This helps the stable oscillation operation by satisfying (11). Also, it has a good effect on phase noise performance. Generally, the amplitude modulation of a VCO is converted to a frequency modulation,

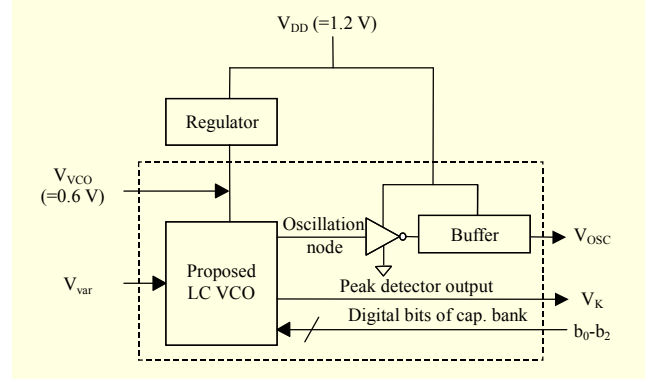


Fig. 13. Implemented VCO circuit schematic.

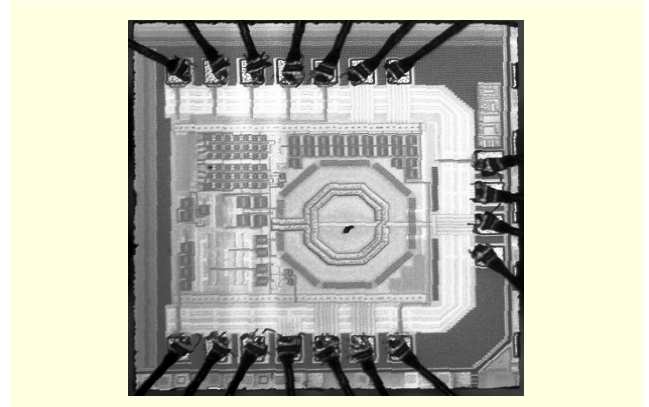


Fig. 14. Photograph of the fabricated wire-bonded VCO chip.

which affects the phase noise performance [15]. The proposed amplitude control mechanism has an advantage for phase noise performance by limiting fluctuations in amplitude.

IV. Measured Results and Discussion

Figure 14 shows a photograph of the VCO chip wire-bonded onto the test PCB board. The chip size is $850 \mu\text{m} \times 850 \mu\text{m}$. The proposed VCO with switched self-biasing was implemented using a $0.13 \mu\text{m}$ CMOS process.

The fabricated VCO can be tuned from 4.5 GHz to 5.1 GHz (a 12.5% tuning range) with 8 coarse tuning steps. The VCO gain for the fixed coarse tuning bit varies from 77.5 MHz/V to 98.3 MHz/V as shown in Fig. 15. The varactor used in the proposed VCO is a typical MOS varactor with the n-region in the gate and source terminal on the n-well using an accumulation mode.

The amplitude characteristics of an oscillation waveform are verified by measuring the peak detector output voltages (V_K) for the coarse frequency tuning, which are shown in Fig. 16. From the peak detector output voltages (V_K), the “obtained V_{pp} from V_K ” value is obtained by $2(V_{DD} - V_K)$. The measured peak-to-peak voltages are slightly smaller than those simulated. We

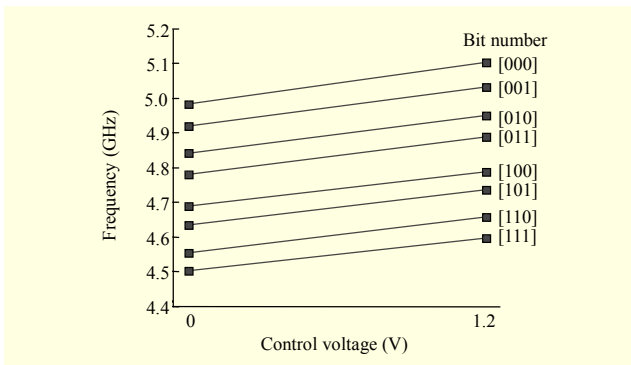


Fig. 15. Measured frequency tuning characteristics.

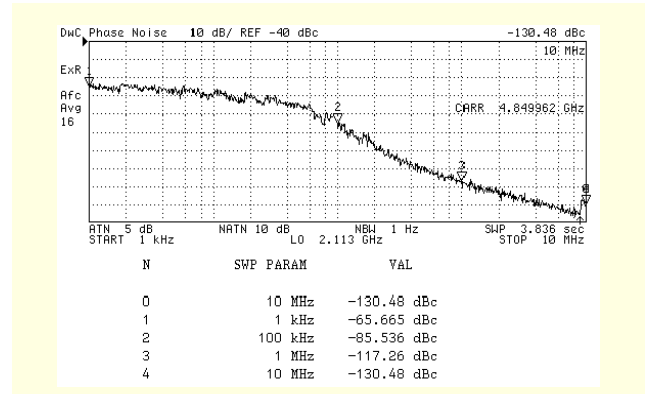


Fig. 18. Measured phase noise at a 4.85 GHz carrier frequency.

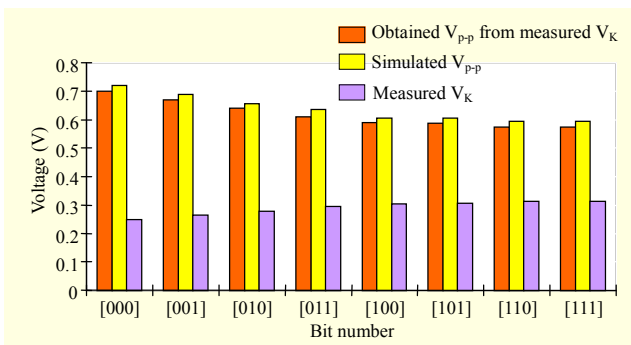


Fig. 16. Measured peak detector output voltages for various digital bit number.

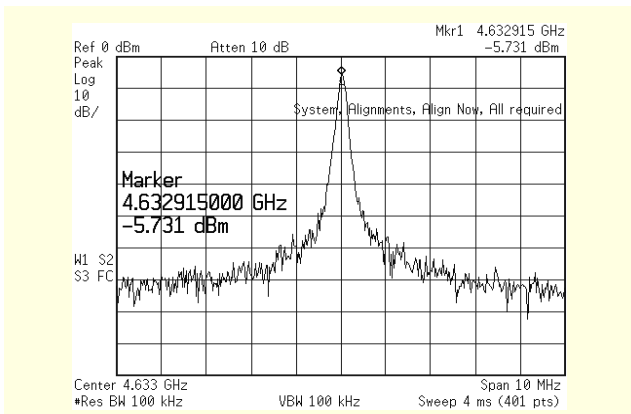


Fig. 17. Measured output spectrum at 4.6329 GHz.

believe this is because the peak detector tracks slightly higher values than the negative peak value of the oscillating waveform. The measured VCO has a tuning range of 4.55 GHz to 5.04 GHz with a variation of peak-to-peak voltages of 0.573 V to 0.701 V. The amplitude change rate for frequency tuning is 131 pV/Hz.

Figure 17 shows the spectrum of the output waveform, and Fig. 18 shows an expanded view of the spectrum near the center frequency obtained by HP4352B (VCO/PLL analyzer) equipment for phase noise measurements. The phase noise

measured at 4.85 GHz shows -85.5 dBc/Hz and -117.3 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. The phase noise curve shows a 32 dB/decade slope between the two offset frequencies.

V. Conclusion

This paper presented an LC VCO with switched self-biasing to improve the phase noise and create an amplitude control effect. By switching the tail transistors in a complementary manner, the flicker noise reduction effect of the tail current source, the current-shaping, and the pulsed bias effect contribute to improving the phase noise characteristics. Table 2 shows the phase noise characteristics that have been published in other works for LC VCOs with flicker noise suppression of the tail current source. A widely used figure-of-merit (FOM) for a VCO is defined, as given in [14], by

$$\text{FOM (dBc)} = L\{\Delta f\} - 20 \log\left(\frac{f_0}{\Delta f}\right) + 10 \log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right), \quad (15)$$

where f_0 , Δf , $L\{\Delta f\}$, and P are the carrier frequency, offset frequency, phase noise specified at the offset frequency, and power consumption, respectively. The calculated FOM is 184.8 dBc with a power dissipation of 3.9 mW at a supply voltage of 0.6 V. The proposed LC VCO with switched self-biasing compares favorably with high performance designs that suppress flicker noise.

Also, the amplitude control loop of the oscillating waveform using a peak detector offers a stable amplitude change rate for frequency tuning, process variation, and temperature change. The measured amplitude change rate ($\partial A / \partial f$) for a frequency tuning of 4.55GHz to 5.04 GHz is 131 pV/Hz. These VCO characteristics can be applied to radio frequency systems such as wireless local area networks that require sufficient tuning range and a good phase noise characteristic.

Table 2. Comparison with prior works on LC VCO.

Reference	Tech. (μm)	f_o (GHz)/ f_{offset} (MHz)	Phase noise (dBc/Hz)	Power (mW)	Supply voltage (V)	FOM (dBc)
[1]	0.25	1.80 / 0.60	-121	6.00	1.50	-182.8
[2]	0.35	2.10 / 15.0	-148	10.8	2.70	-180.6
[3]	0.25	1.75 / 3.00	-134	2.25	1.50	-185.8
[4]	0.65	2.00 / 0.60	-125	34.2	1.80	-180.1
This work	0.13	4.85 / 1.00	-117	3.90	0.60	-184.8

References

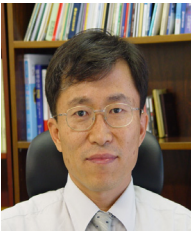
- [1] A. Hajimiri and T.H. Lee, "Design Issues in CMOS Differential LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 34, May 1999, pp. 717-724.
- [2] E. Hegazi, H. Sjöland, and A.A. Abidi, "A Filtering Technique to Lower LC Oscillator Phase Noise," *IEEE J. Solid-State Circuits*, vol. 36, Dec. 2001, pp. 1921-1930.
- [3] B. Soltanian and P. Kinget, "Tail Current-Shaping to Improve Phase Noise in LC Voltage-Controlled Oscillators," *IEEE J. Solid-State Circuits*, vol. 41, Aug. 2006, pp. 1792-1802.
- [4] B.D. Muer et al., "A 2-GHz Low-Phase-Noise Integrated LC VCO Set with Flicker-Noise Up-Conversion Minimization," *IEEE J. Solid-State Circuits*, vol. 35, July 2000, pp. 1034-1038.
- [5] Y. Ku et al., "Close-In Phase-Noise Enhanced Voltage-Controlled Oscillator Employing Parasitic V-NPN Transistor in CMOS Process," *IEEE J. Trans. Microwave Theory and Technique*, vol. 54, Apr. 2006, pp. 1363-1369.
- [6] I. Bloom and Y. Nemirovsky, "1/f Noise Reduction of Metal-Oxide-Semiconductor Transistors by Cycling from Inversion to Accumulation," *Appl. Phys. Lett.*, vol. 58, Apr. 1991, pp. 1664-1666.
- [7] B. Dierickx and E. Simoen, "The Decrease of 'Random Telegraph Signal' Noise in Metal-Oxide-Semiconductor Field-Effect Transistors When Cycled from Inversion to Accumulation," *J. Appl. Phys.*, vol. 71, Feb. 1992, pp. 2028-2029.
- [8] A.P. van der Wel et al., "MOSFET 1/f Noise Measurement under Switched Bias Conditions," *IEEE Electron Device Letters*, vol. 21, Jan. 2000, pp. 43-46.
- [9] Z. Zhang and J. Lau, "Experimental Study on MOSFET's Flicker Noise under Switching Conditions and Modeling in RF Applications," *Proc. IEEE Custom Integrated Circuits Conf.*, 2001, pp. 393-396.
- [10] E.A.M. Klumperink et al., "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing," *IEEE J. Solid-State Circuits*, vol. 35, July 2000, pp. 994-1001.
- [11] S.L.J. Gierkink et al., "Intrinsic 1/f Device Noise Reduction and Its Effect on Phase Noise in CMOS Ring Oscillators," *IEEE J. Solid-State Circuits*, vol. 34, July 1999, pp. 1022-1025.
- [12] C.C. Boon et al., "RF CMOS Low-Phase-Noise LC Oscillator through Memory Reduction Tail Transistor," *IEEE J. Trans. Circuits and Systems-II: Express Briefs*, vol. 51, Feb. 2004, pp. 85-90.
- [13] D. Park and S. Cho, "A Power-Optimized CMOS LC VCO with Wide Tuning Range in 0.5 V Supply," *Proc. ISCAS*, 2006, pp. 3233-3236.
- [14] N. Fong et al., "Design of Wide-Band CMOS VCO for Multiband Wireless LAN Applications," *IEEE J. Solid-State Circuits*, vol. 38, Aug. 2003, pp. 1333-1342.
- [15] Ja-Yol Lee et al., "Fully Differential 5-GHz LC-Tank VCOs with Improved Phase Noise and Wide Tuning Range," *ETRI Journal*, vol. 27, no. 5, 2005, pp. 473-483.



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