Demonstration of burst mode bit discrimination circuit for 1.25 Gb/s and 10.3 Gb/s dual-rate reach extender of WDM-TDM-hybrid-PON systems based on 10G-EPON

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Abstract: We proposed a simple and cost-effective burst mode bit discrimination circuit for dual rate reach extender based on 10 gigabit Ethernet passive optical network. To distinguish the dual rate burst mode packets, periodic idle patterns which have specific frequency components in the frequency domain and radio frequency power detection technique were used. The burst mode dual rate upstream transmission was demonstrated to confirm the feasibility of our suggested method in a coexisted gigabit Ethernet passive optical network and 10 gigabit Ethernet passive optical network. We achieved the dual rate burst mode receiver sensitivity of – 32 dBm for 1.25 Gbit/s signal and –27 dBm for 10.3 Gbit/s signal, respectively.

OCIS codes: (060.4250) Networks; (060.4510) Optical communications.

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1. Introduction

Strong demands for 10 Gbit/s-class PON systems are being increased to meet the rapid growth of required dedicated bandwidth for each customer along with the development of 3DTV and UHDTV technologies [1]. Although these higher bit rate PON systems offer relatively huge bandwidth per subscriber, there have still been some problems for achieving long reach transmission and compensating higher splitting loss. One of the meaningful approaches to solve these obstacles is to place the active reach extender (RE) in the feeder span [2]. So far, a various kinds of methods to implement the RE have been reported [3–5]. Among them, the RE based on OEO regeneration has been preferred to provide the better transmission performances and cost-effectiveness [4]. For realizations of 10 Gbit/s-class RE, the coexistence of legacy 1 Gbit/s-class optical network unit (ONU) and 10 Gbit/s-class ONU should be taken into account [6]. In case of 10 gigabit Ethernet PON (10G-EPON) standard, 1 G & 10 G signals adopted same wavelength band for upstream transmission and they could induce signal overlap in the optical domain. To separate these dual rate signals, the concept of dual rate physical medium dependent (PMD) sub-layers has been introduced [6,7]. Most of dual rate PMD sub-layers have been designed to be operated in optical line terminal (OLT) side which already equipped the media access control (MAC) layer and provided the rate select (RS) signal from MAC layer to distinguish the dual rate burst mode packets [8]. However, in the RE, it is necessary to prepare the additional functional block to discriminate the dual rate upstream packets, because the RS signal cannot be provided by the RE. Hara et al. firstly reported the burst mode bit discrimination circuit (BM-BDC) using delay lines and many digital logic gates [7]. But this scheme was relatively difficult and expensive to implement owing to the tight delay control and complicated configuration.

In this paper, we propose a simple and cost-effective method to provide BM-BDC for dual rate RE based on 10G-EPON and several transmission performances are reported to confirm feasibility of it.

2. Configuration of dual rate reach extender

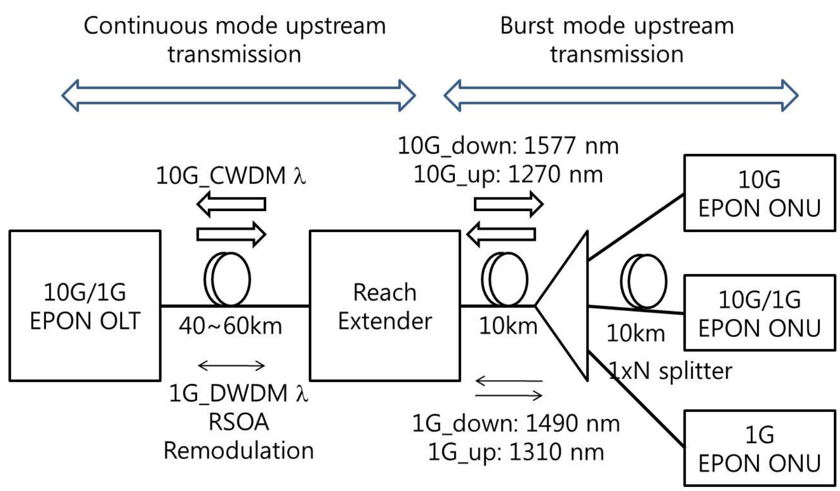

Fig. 1. Our proposed link architecture of 1G/10G coexisted WDM-TDM-Hybrid-PON by using dual rate reach extender.

Figure 1 shows our proposed link architecture of 1G/10G coexisted WDM-TDM-Hybrid-PON by using dual rate reach extender. In the distribution network, we used the wavelength plan for legacy 10G-EPON system. The downstream transmission wavelength is 1490 nm for

1.25 Gb/s signal and 1577 nm for 10.3 Gb/s signal. The upstream wavelengths for 10.3 Gb/s and 1.25 Gb/s are coexisted in the range from the 1260 nm to 1360 nm. While in the feeder section, the 10.3 Gb/s signals are transmitted in the CWDM wavelength ranges and 1.25 Gb/s signals are transmitted in the C-band which centered at the 1550 nm. The coarse wavelength division multiplexing (CWDM) transceivers based on the electro-absorption modulator integrated laser (EML) and dense wavelength division multiplexing (DWDM) transceivers based on RSOA using remodulation techniques can be used for the 10.3 Gb/s and 1.25 Gb/s, respectively [9].

Figure 2 illustrates the detail configuration of dual rate RE. The RE has the abilities to convert the wavelengths between WDM and legacy TDM-PON systems and to achieve the 3R regeneration for enhancing the total link power budget. Especially, the upstream burst mode signals have been converted to continuous mode packets in the RE by means of the field-programmable gate array (FPGA) and externally equipped frame multiplexer and demultiplexer. So, we don't need to employ the burst mode transceiver in the feeder section.

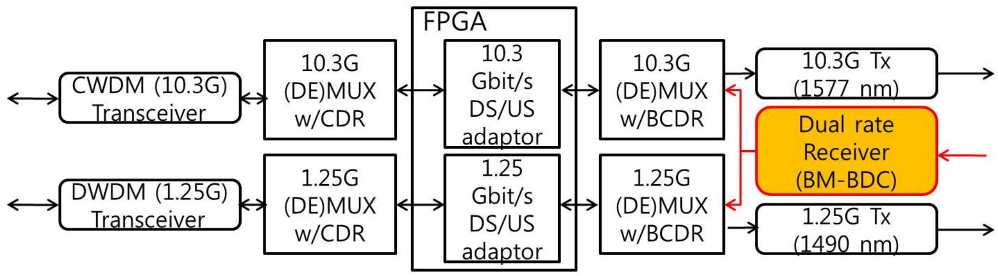

Fig. 2. Detail configuration of dual rate reach extender based on 10G-EPON.

3. Burst mode receiver with dual rate bit discrimination circuit

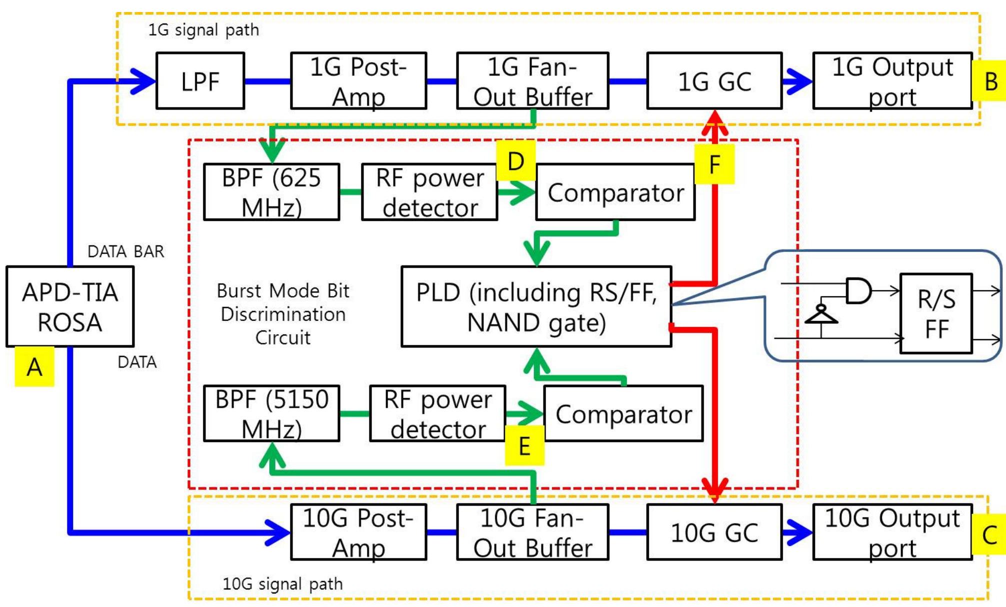

Fig. 3. Functional block diagram of dual rate burst mode receiver including BM-BDC.

Figure 3 shows the functional block diagram of dual rate burst mode receiver including BM-BDC. The dual rate burst mode receiver is comprised of an avalanche photodiode-trans impedance-amplifier (APD-TIA), a 1G post-amplifier, a 10G post-amplifier, a BM-BDC for

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separating the each incoming burst packet depending on the bit rate, and two gating circuits (GCs). The typical trans-impedance gain of our used APD-preamplifier was approximately 900 ohm for single ended operation and the 3dB cut-off frequency was about 8 GHz. The 1G and 10 post amplifiers had 1 GHz and 10 GHz of 3 dB bandwidth, respectively. Our dual rate burst mode receiver could not employ a burst mode preamplifier and post-amplifiers integrated circuits (IC) which were not available in our laboratory. However, we could employ the well-known baseline-wander-common-mode-rejection technique and an inverted distortion technique to build an AC-coupled burst mode receiver by using commercially available continuous mode operated pre- and post-amplifiers [10].

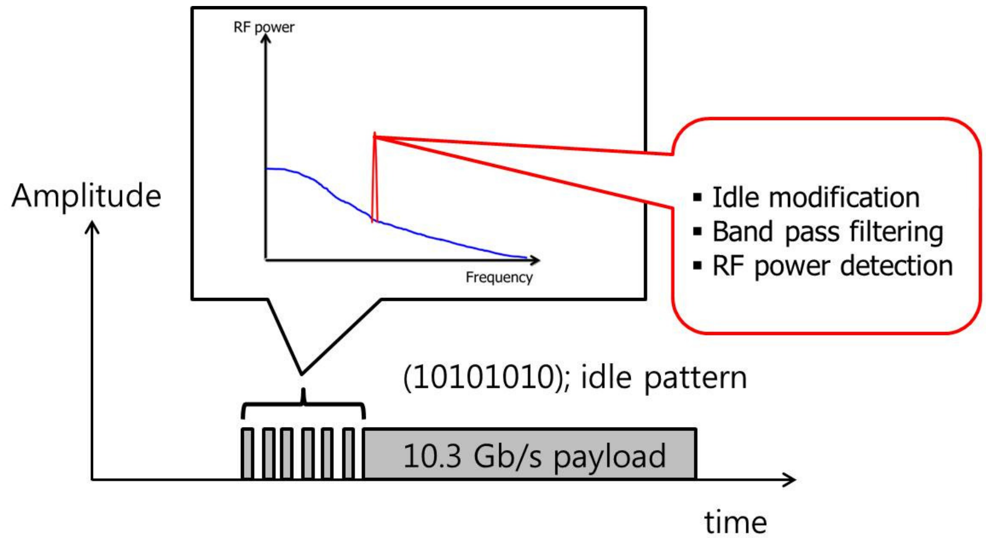

Fig. 4. Basic operating principle of BM-BDC by means of band pass filtering and RF power detection techniques.

In order to implement the BM-BDC easily, we made use of periodicity of some idle patterns that were typically included in the burst mode signal, which is shown in Fig. 4. Conventionally, binary 10 followed by 0x BF 40 18 E5 C5 49 BB 59 (transmission bit sequence 10 1111 1101 0000 0010 0001 1000 1010 0111 1010 0011 1001 0010 1101 1101 1001 1010) pattern is used for a burst mode idle (synchronization) pattern in 10G-EPON systems. Similarly, in the 1G-EPON systems, idle patterns are comprised of (0011111010) and (1001000101). To generate the arbitral peak components in the frequency domain, we proposed to modify the normal idle patterns employed in the 1G-EPON and 10G-EPON to “1010 “alternating bit streams. Theoretically, this cyclic idle pattern has specific peak components in the frequency regime. For example, 1.25 Gbit/s idle patterns such as “1010” provided the peak component at the 625 MHz, and 10.3 Gbit/s idle patterns also produced the spectral distribution peaking at the 5.15 GHz. Due to these different peak elements in the frequency domain, it could be enabled us to automatically discriminate the received dual rate burst packets by means of band pass filter and RF power detector. The pass band of our used band pass filter for the detection of 1G and 10G idle pattern was 3 MHz and 100 MHz, respectively. Temperature Compensated Internal Schottky Diode RF Detectors were used for band pass filtered RF power level detection.

However this modification of idle pattern caused some performances degradations of burst mode receiver. These degradations came from the peak detector in burst mode pre- and post-amplifier and phase error in burst mode clock data recovery IC. As a result, sensitivity deterioration of burst mode receiver and reduction of timing margin for data recovery might be happened if we changed the idle patterns [11]. Nevertheless, we could mitigate the “1010”

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pattern induced performance degradations by means of AC coupling method (average peak detector) to realize the dual rate burst mode receiver [12].

The analog output of RF power detector was employed for an input of the digital comparator. Then, the digital comparator provided the digital logic levels with the limited time duration, which is also an input of programmable logic device (PLD) including reset-set flip flop (R/S FF) and NAND gate [7]. Detail configuration of PLD is depicted in inset of Fig. 3. The PLD generates the gating signals which are dependent on the pulses output from the 1G-path comparator and the 10G-path comparator.

4. Transmission performances

Figure 5 shows an experimental setup to investigate the upstream burst packet transmission performances. Upstream burst signal from ONU transmitters which had bit rates of 10.3- and 1.25 Gbit/s with 2^{31}-1 pseudo-random binary sequences (PRBS) patterns and 2^{7}-1 PRBS patterns, respectively. To generate the dual rate burst mode upstream packets, we employed the Agilent Technologies' PARBERT™ system. We set the extinction ratio of 10 dB for each burst mode transmitter and adjusted the optical power level to our burst mode dual rate receiver including BM-BDC with variable optical amplifier. Both 1G and 10G burst mode upstream signals had an idle pattern length of up to 400 ns, a payload length of 12800 ns, and a guard time of 100 ns. The idle patterns we used were "1010".

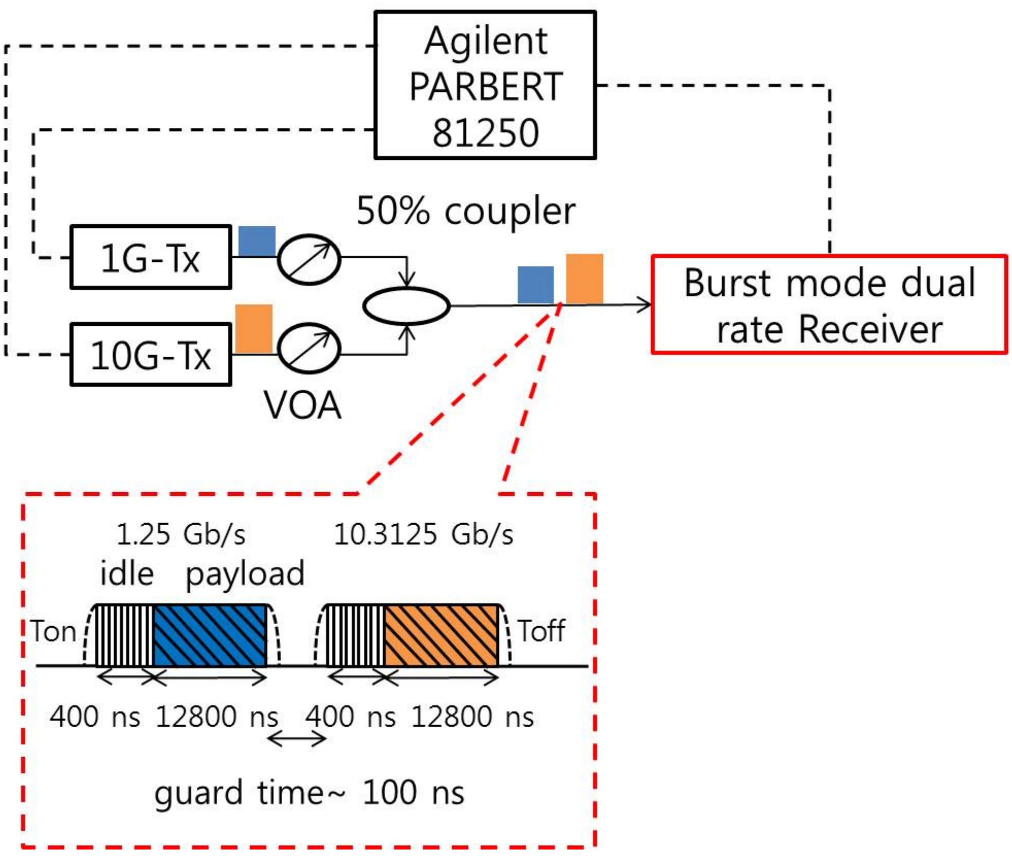

Fig. 5. Experimental setup for burst mode upstream transmission.

Figure 6(A) shows the optical waveform of combined 1.25- and 10.3-Gbit/s signals, which was measured at the optical input port of APD-TIA. Figure 6(B) and Fig. 6(C) shows the measured electrical output waveforms of the 1G-GC and 10 G-GC, respectively. The band pass filtered analog signal outputs from the RF power detector in 1G-path and 10G-path in

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BM-BDC are also shown in Fig. 6(D) and Fig. 6(E), respectively. The starting points of them are all existed within idle time durations. In the Fig. 6(F), the input of 1G-GC is illustrated, which is one of the outputs from the PLD. As expected, the input of 10G-GC is complementary signal of 1G-GC.

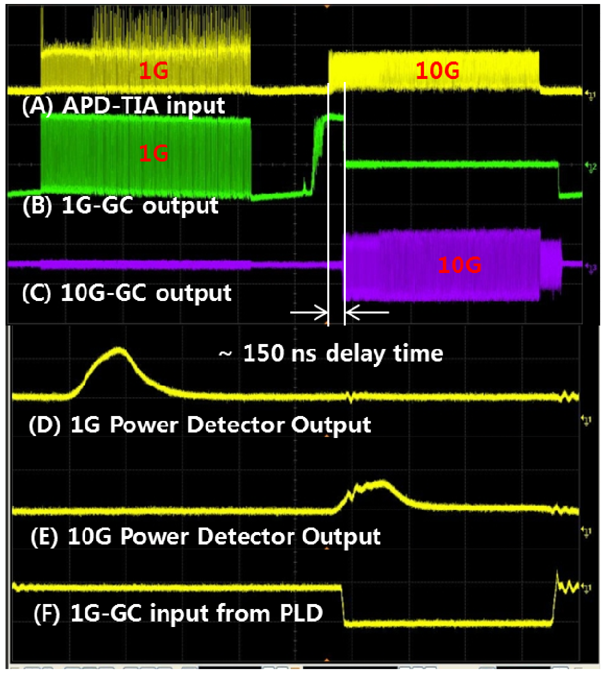

Fig. 6. Measured waveforms at the each reference point which are already depicted in Fig. 3.

Finally, we measured the delay time between the APD-TIA and 10G-GC output, which is shown in Fig. 7. The measured delay time was within idle time of 400 ns. There have been no problems to discriminate the dual rate burst packets in the required idle time, which was proposed in the standardization document [6].

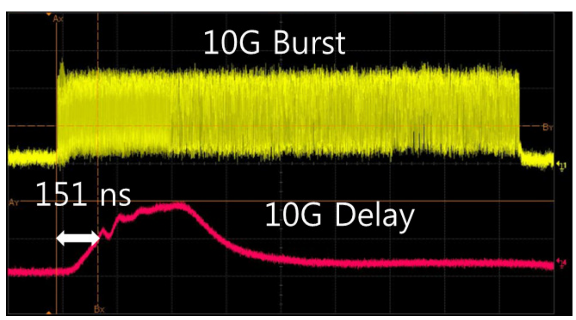

Fig. 7. Measured delay time of 10G burst mode signal.

Figure 8 shows the bit error rate plots for burst-mode operation of 1.25 and 10.3 Gbit/s signals. For the 1.25 Gbit/s signal, we obtained a sensitivity of −32 dBm to achieve the 10^{-12} BER. For the 10.3 Gbit/s signal we realized a sensitivity of −27 dBm to attain 10^{-3} BER, which corresponds to the forward error correction technique [10].

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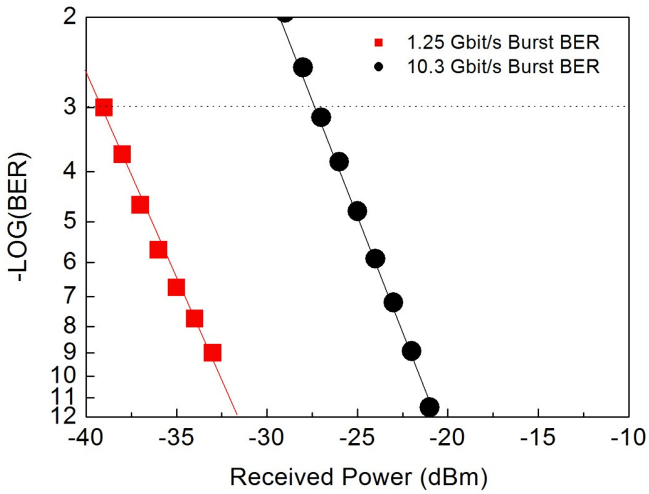

Fig. 8. Measured BER plots for both 1G and 10G burst mode upstream signals.

5. Conclusion

We have proposed simplified BM-BDC for 10G-EPON based dual rate RE and experimentally examined via upstream burst packet transmission. A dual rate burst mode receiver with our proposed BM-BDC needed not any RS signal and also successfully distinguished the dual rate burst mode upstream signals in the required idle time duration. We also achieved the dual rate burst mode receiver sensitivity of – 32 dBm for 1.25 Gbit/s signal and −27 dBm for 10.3 Gbit/s signal, respectively. Our suggested scheme for BM-BDC shows relatively simple configuration and cost-effectiveness by taking advantage of band pass filtering and RF power detection of burst mode idle patterns.

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