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The Characteristics of Seebeck Coefficient in Silicon Nanowires Manufactured by CMOS Compatible Process

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Abstract Silicon nanowires are patterned down to 30 nm using complementary metal-oxide-semiconductor (CMOS) compatible process. The electrical conductivities of n-/p-leg nanowires are extracted with the variation of width. Using this structure, Seebeck coefficients are measured. The obtained maximum Seebeck coefficient values are 122 μV/K for p-leg and −94 μV/K for n-leg. The maximum attainable power factor is 0.74 mW/m K^2 at room temperature.

Keywords Thermoelectric effect · Seebeck coefficient · Silicon · Nanowire

Introduction

Thermoelectric device interconverts thermal gradient and electricity for power generation or cooling [1–3]. Traditionally, Bi_2Te_3 semiconductor has been widely used as thermoelectric material due to its high thermoelectric performance, which has $ZT = \alpha^2\sigma T/\kappa \approx 1$, where α, σ, κ and T represent Seebeck coefficient, electrical conductivity, thermal conductivity and absolute temperature, respectively [4, 5]. However, thermoelectric devices based on Bi_2Te_3 are difficult to miniaturize. In addition, according to the late tendency of development and production of products using Bi_2Te_3 thermoelectric devices, supplies of Bi_2Te_3 are predicted to face shortage soon. On the contrary, silicon is the most abundant semiconductor material with the matured fabrication infrastructure. One drawback in the consideration of silicon as thermoelectric material is the low ZT value (~0.01) due to its high κ value (~150 $Wm^{-1}K^{-1}$) at room temperature [6, 7]. Thus, silicon has been considered as the impropriate material for the thermoelectric applications. However, recent research revealed the possibility of silicon as thermoelectric material by incorporating nanotechnology. One-dimensional (nanostructured) silicon nanowire can dramatically reduce the phonon propagation through the nanowire while maintaining the electron/hole propagation property [8–10].

In this work, complementary metal-oxide-semiconductor (CMOS) compatible process is adopted to implement silicon thermoelectric device. By using conventional CMOS process, we have manufactured n-/p-type silicon nanowires, which correspond to n-/p-legs, respectively. The defined minimum width of silicon nanowire is 30 nm. The electrical conductivities are evaluated for the various nanowire widths. Also, Seebeck coefficient and maximum attainable power factor is evaluated from the manufactured n-/p-legs.

Experimental Details

The <100> *p*-type 8-inch silicon-on-insulator (SOI) wafer is used to fabricate thermoelectric device. SOI wafer is boron doped with a resistivity of 13.5–22.5 Ω cm, and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. The thickness of the SOI and buried oxide (BOX) layer is 100 and 2,000 nm, respectively. SOI layer is thinned down to 40 nm using thermal oxidation method. BF_2 and phosphorus atoms are doped for n-/p-leg formation using ion implantation method. And 160 nm wire

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patterns are defined by using KrF lithography technique. After photo-lithography step, O_2 plasma ashing technique is adopted to reduce the wire width down to 30 nm. After the patterning of silicon nanowires using dry etching technique, 10 nm-thick titanium layer and 100-nm-thick platinum layer are sputtered and patterned using lift-off method. Titanium is used as adhesion layer between silicon and platinum. Platinum layer is used as heating source and temperature sensor.

Results and Discussion

Figure 1 shows the scanning electron microscopy (SEM) images after KrF lithography and O_2 plasma ashing. As explained in the experimental details, 160-nm silicon patterns are defined photo-lithographically defined by using KrF scanner as shown in Fig. 1a. And by using O_2 plasma ashing technique, 160-nm patterns are reduced down to 30 nm as shown Fig. 1b. By using this technique, bunches of silicon nanowires can be patterned on the whole region of 8-inch wafer.

Figure 2 shows the finally formed silicon nanowire pattern after the removal of 2 μm-thick BOX layer using gas phase etching (GPE) using HF vapor gas. As shown in Fig. 2, the 30 nm-wide silicon nanowire is fully suspended.

The variations of electrical conductivities of n-/p-legs as a function of nanowire width are summarized in Fig. 3. The open and closed circles correspond to n-/p-leg, respectively. N-leg is doped using phosphorus with the dose of 5×10^{15} cm^{-2}. The extracted electrical conductivity of 30-nm n-leg (σ_n) is 842 Ω^{-1} cm^{-1}, and the corresponding doping concentration is around 6.0×10^{19} cm^{-3}. P-leg is doped using BF_2 with the dose of 5×10^{15} cm^{-2}. The extracted electrical conductivity of 30 nm p-leg (σ_p) is 396 Ω^{-1} cm^{-1}, and the corresponding doping concentration is around 4.0×10^{19} cm^{-3} [11]. The

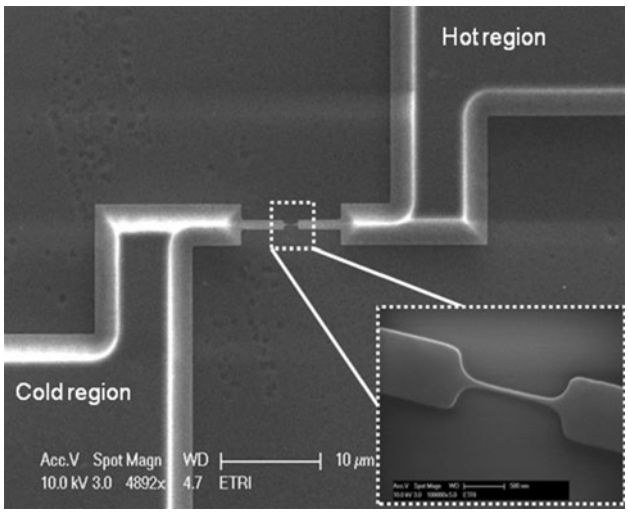

Fig. 2 SEM image of the finally formed silicon nanowire after the removal of 2 μm-thick BOX layer using GPE method

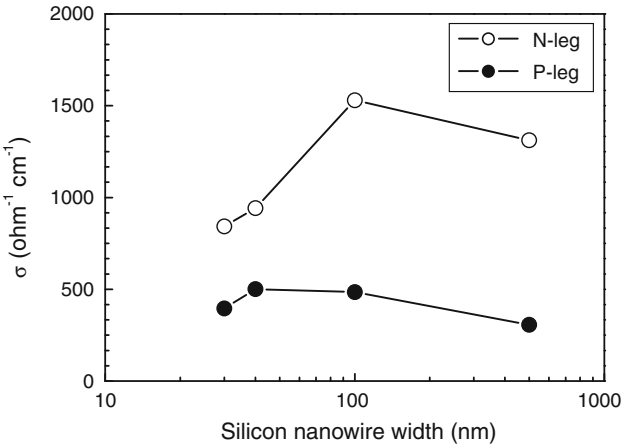

Fig. 3 The variations of electrical conductivities as a function of nanowire width in n-/p-legs. The *open* and *closed circles* correspond to n-leg and p-leg, respectively. N-leg is doped using phosphorus with the dose of 5×10^{15} cm^{-2}. P-leg is doped using BF_2 with the dose of 5×10^{15} cm^{-2}

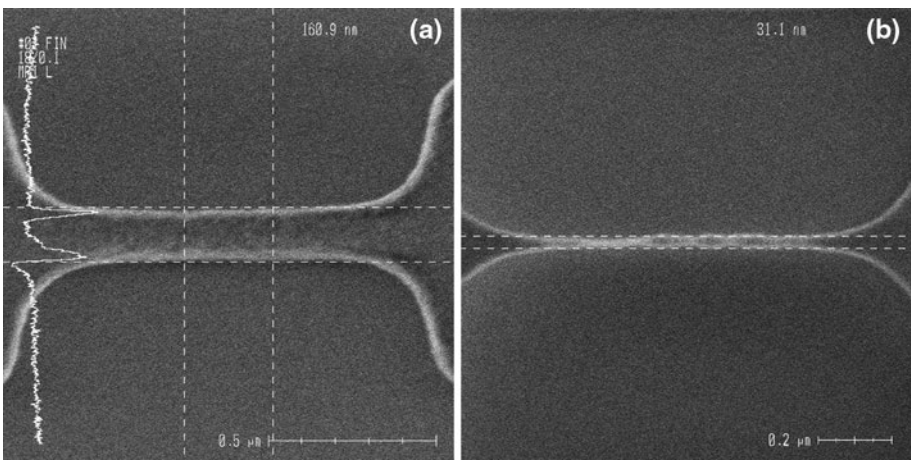

Fig. 1 SEM images after KrF lithography (**a**) and O_2 plasma ashing (**b**)

decrease in electrical conductivities with the decrease in width is due to the finite line width effect.

Figure 4 shows the measured output voltage as a function of temperature difference between cold and hot region. The cold region temperature (T_C) is set as 20°C, and the hot region temperature (T_H) is controlled from 20 to 42°C. The output voltage characteristics are measured in various nanowire widths of 30, 40, 100 and 150 nm. The output voltage linearly increases as the temperature increases in both n-/p-leg. The slope represents Seebeck coefficient. P-leg shows more sensitive response to the temperature than n-leg, which is typical characteristic in thermoelectric material [13].

Figure 5 shows the extracted Seebeck coefficients from Fig. 4. The open and closed circles correspond to n-leg and p-leg, respectively. In n-leg, Seebeck coefficient (α_n) varies from −77 to −94 μV/K depending on the width. In p-leg, Seebeck coefficient (α_p) varies from 108 to 122 μV/K. In the case of serial connection between n-leg and p-leg, the attainable Seebeck coefficient value (α) can be estimated using weighted average relation, i.e., $\alpha = (\alpha_n\sigma_n + \alpha_p\sigma_p)/(\sigma_n + \alpha_p)$ [2]. By applying this relation, the maximum attainable Seebeck coefficient is 105 μV/K in the case of serial connection between 30-nm n-leg and 40-nm p-leg. In this case, the maximum attainable power factor ($\alpha^2 \cdot \sigma$) is 0.74 mW K^{-2} cm^{-1}. By optimizing the doping concentration, nanowire width and process conditions, Seebeck coefficient should be increased up to 200 μV/K for the comparable property with Bi_2Te_3 in power factor.

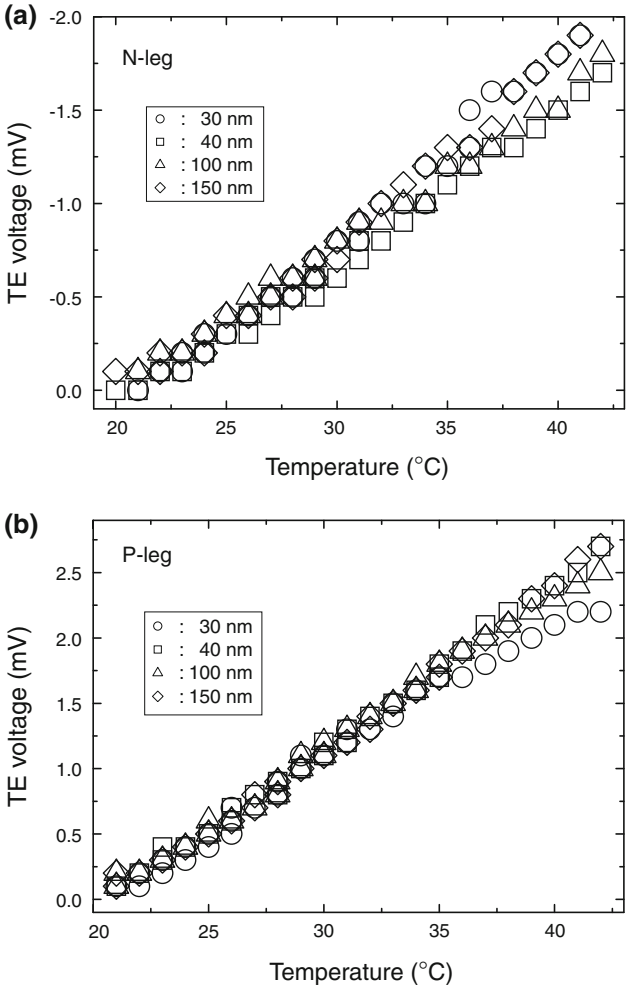

Fig. 4 The measured output voltage as a function of temperature difference between cold and hot region. The cold region temperature (T_C) is set as 20°C, and the hot region temperature (T_H) is controlled from 20 to 42°C. The output voltage characteristics are measured in various nanowire widths of 30, 40, 100 and 150 nm

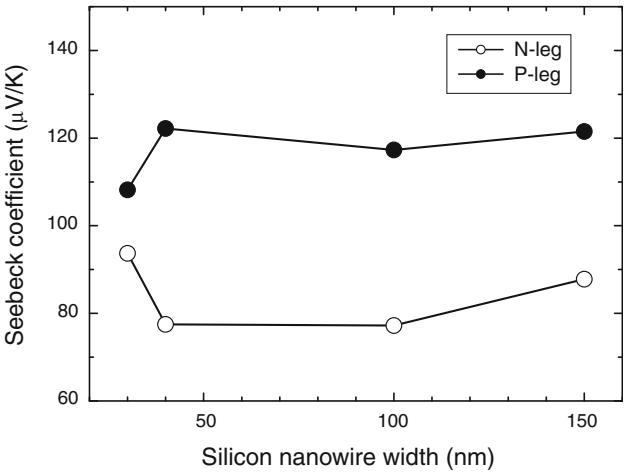

Fig. 5 The extracted Seebeck coefficients with the variation of nanowire width. The *open* and *closed circles* correspond to n-leg and p-leg, respectively

Conclusions

CMOS compatible process is adopted to implement the real silicon thermoelectric device. By using conventional CMOS process, we have manufactured n-/p-type silicon nanowires. The defined minimum width of silicon nanowire is 30 nm. The electrical conductivities of n-/p-leg nanowires are extracted with the variation of width. Using this structure, Seebeck coefficients are measured. The obtained maximum Seebeck coefficient values are 122 μV/K for p-leg and −94 μV/K for n-leg, respectively. The maximum attainable power factor is 0.74 mW/m K^2 at room temperature.

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