Novel Bumping and Underfill Technologies for 3D IC Integration

Ki-Jun Sung, Kwang-Seong Choi, Hyun-Cheol Bae, Yong-Hwan Kwon, and Yong-Sung Eom

In previous work, novel maskless bumping and no-flow underfill technologies for three-dimensional (3D) integrated circuit (IC) integration were developed. The bumping material, solder bump maker (SBM) composed of resin and solder powder, is designed to form low-volume solder bumps on a through silicon via (TSV) chip for the 3D IC integration through the conventional reflow process. To obtain the optimized volume of solder bumps using the SBM, the effect of the volumetric mixing ratio of resin and solder powder is studied in this paper. A no-flow underfill material named "fluxing underfill" is proposed for a simplified stacking process for the 3D IC integration. It can remove the oxide layer on solder bumps like flux and play a role of an underfill after the stacking process. The bumping process and the stacking process using the SBM and the fluxing underfill, respectively, for the TSV chips are carefully designed so that two-tier stacked TSV chips are sucessfully stacked.

Keywords: Maskless bumping, solder bump maker (SBM), fluxing underfill, through silicon via (TSV), stacking process.

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I. Introduction

Three-dimensional (3D) packaging technology with through silicon via (TSV) has been considered as a solution for the market demand for high-density, high-speed, high-performance, and low-cost electronic components [1]-[3]. It can improve the electrical performance by reducing the physical size of the electronic systems and combining different devices into one packaged system. For 3D silicon chips, flip chip technology can be a good solution for the 3D integration through chip-to-chip or chip-to-wafer bonding processes [4]-[8].

However, the conventional flip chip bonding technology does not seem to be applicable to the 3D integration process, because its pitch of the bump array and gap between the chips after stacked are not suitable for that. For example, screen printing and electroplating are typical technologies used for the conventional bumping process. Screen printing has the desirable features of low-cost bumping and easy processing, but it cannot be used in a fine-pitch less than 150 μm, which is quite a big pitch for the 3D integrated circuit (IC) technology [9], [10]. Currently, electroplating is used in bumping processes for the 3D IC, but it is high-cost and has a low-level degree of freedom of material compositions.

To overcome these limitations, solder bump maker (SBM) technology was proposed [11], [12]. Its distinct advantages were low cost, a maskless process, and adaptability of fine-pitch and material compositions such as Sn3.0Ag0.5Cu (SAC305), SnAg, and other lead-free solders. Since its bumping mechanism depends on the diameter distributions of solder powder, the uniformity of the solder bump array formed using SBM needed to be enhanced.

One of the differences between conventional flip chip and stacking processes for 3D IC technology is flux. The flux

cannot be used in 3D IC technology since the residue it leaves after bonding cannot be washed away because of the narrow gap between stacked chips [6]. There are many technical approaches to replace flux. To remove the oxide layer on solder bumps without flux, [13] considered plasma treatment, formic acid, hydrogen radicals, and vacuum ultraviolet. However, these solutions need additional equipment developments for mass production. Other researchers focused on the material developments [14]-[17]. No-flow (pre-applied) underfill, wafer-level underfill, and nonconductive paste (NCP) bonding have the same purpose, which is to combine the functions of flux and underfill into one polymer matrix. With these materials, the process steps to stack the TSV chips can be simplified. However, for these materials to be used as commercial products, improvements must be made, such as creating a void-free underfill and ensuring manufacturability.

In this paper, the bumping process using the SBM is optimized to obtain a uniform solder bump array on a TSV chip. The effect of the volumetric mixing ratio of resin and solder powder in the SBM and the coining process after the bumping process using the SBM are studied. Also, we propose a novel no-flow underfill called "fluxing underfill." The fluxing underfill is distinguished as having a deoxidizing capacity of the oxide layer on the surface of the solder bumps as well as the metal electrodes and no out-gassing related with solvents during the stacking process. The characteristics of the fluxing underfill are analyzed using a differential scanning calorimetry (DSC), a dynamic mechanical analyzer (DMA), and a thermo-gravimetric analyzer (TGA). Finally, a TSV chip is fabricated, and the bumping process using the SBM on a TSV chip and the stacking process using fluxing underfill are successfully performed with the TSV chips.

II. Materials and Experiment

1. Materials

A. SBM

The SBM is composed of resin and solder powder. The resin carries the solder powder during the bumping process. A deoxidizing agent and additives are added into the resin to remove the oxide layer on the solder powder as well as metal electrodes during the bumping process [18]-[20]. The mixing ratio between the deoxidizing agent and solder powder is precisely designed according to the amount of oxide in the solder powder. The solvent is not included in the resin to prevent out-gassing from the resin during the bumping process, which can be one of the sources of the voids in the underfill. The composition of the solder powder is Sn-58Bi.

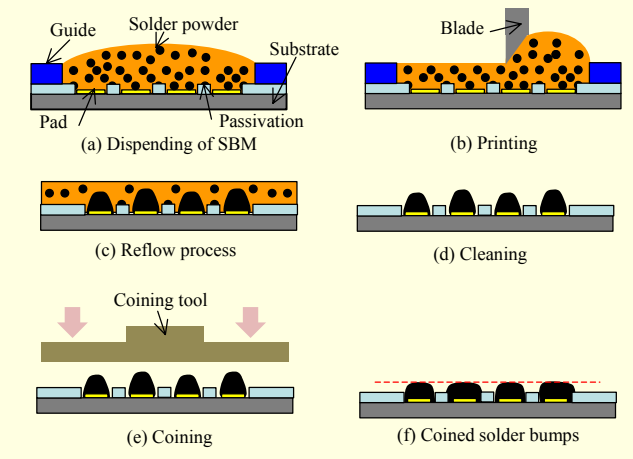

Fig. 1. Schematic diagram of solder bumping process using SBM.

B. Fluxing Underfill

Fluxing underfill is made of an epoxy-based thermoset, a deoxidizing agent, additives, and a hardener. The viscosity change with temperature is controlled by the thermoset so that considering the process condition of the stacking process leads to proper material design. Since the function of the deoxidizing agent and additives is the same as that in the SBM, the same types of the materials are used in the fluxing underfill. To design a proper hardener for the fluxing underfill, the effect of the increase rate of process temperature during the stacking process on the curing temperature of the fluxing underfill is considered so that the curing of the fluxing underfill occurs after the solder bump melts. As in the SBM, no solvents are added in the fluxing underfill because they can cause voids in the underfill after the stacking process.

2. Experimental Procedure

A. Bumping Process Using SBM

Test vehicles are fabricated to evaluate the SBM and fluxing underfill technologies. The diameter and pitch of TSVs in the silicon chip are 45 μm and 150 μm, respectively. The array of the TSV is 32 × 32. The size of the TSV chip is 7 mm × 7 mm, and its thickness is 50 μm. No under-bump metallization (UBM) is deposited on the Cu-filled TSVs in the TSV chips. A silicon substrate with one redistribution layer is fabricated, and its UBM structure is Cu (5 μm)/Ni (2 μm)/Au (0.5μm). The size of the Si substrate is 9.5 mm × 11.5 mm × 0.75 mm.

Figure 1 shows the schematic diagram of the solder bumping process using the SBM. As shown in Fig. 1(a), a guide is placed on a substrate. The substrate can be a TSV chip, Si wafer, or a plastic substrate such as a printed circuit board (PCB). The guide is only a standoff to keep the thickness of the SBM uniform; the guide is not a patterned mask used in the

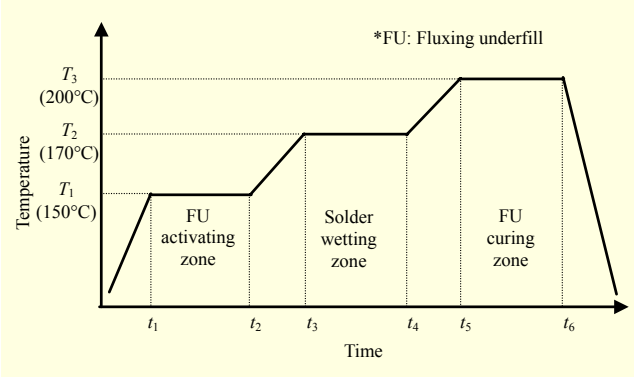

Fig. 2. Reflow profile to stack TSV chips on Si substrate using fluxing underfill.

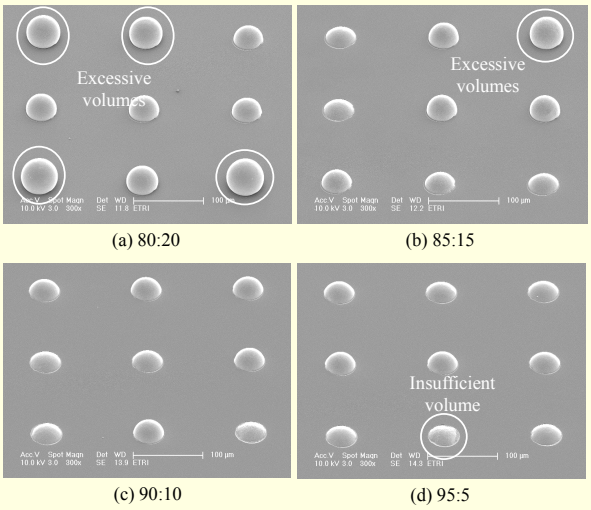

Fig. 3. SEM images of formed solder bump arrays using SBM with variations of volumetric mixing ratios of resin and solder: (a) 80:20, (b) 85:15, (c) 90:10, and (d) 95:5.

stencil printing process to separate each pad. The SBM is scraped by a blade on the guide, as shown in Fig. 1(b). The guide is then removed from the substrate. The substrate with the SBM is reflowed at 200°C for 60 seconds in an IR oven. The remaining resin and solder powder in the resin are washed away by a cleaning process. After that, the solder bumps are coined using a commercial flip-chip bonder. The coining process is performed at 110°C for 60 seconds under the pressure of 0.1 gf/bump to make the heights of the solder bumps uniform. Then, the heights of at least 10 solder bumps at the top, bottom, left, right, and middle areas of the substrate are measured using an alpha-step instrument.

B. Stacking Process Using Fluxing Underfill

The TSV chips are stacked on the Si substrate using the fluxing underfill. Figure 2 shows a reflow profile to stack TSV chips on a Si substrate using fluxing underfill. It consists of five steps. First, fluxing underfill is applied on the substrate, and a TSV chip is picked and placed on a Si substrate. Next, the fluxing underfill is activated and spreads by a capillary force between the TSV chip and the substrate at the temperature T_1. Then, the solder bump array on the TSV chip melts on the UBM on the opposite substrate at the temperature T_2, which is higher than the melting temperature of the solder bump array. After that, the temperature is increased to T_3 for the curing of the fluxing underfill. Finally, the temperature is decreased to room temperature. More than two tiers of stacked TSV chips on the substrate can be stacked by iterating the process explained above. It should be noted that there is not a process of the underfill that includes flux dispensing, cleaning, plasma treatment, underfilling, and curing.

III. Results and Discussion

Figure 3 shows the SEM images of formed solder bump arrays using the SBM with the variations of the volumetric mixing ratio of resin and solder. The solder bumps using the SBM with a large portion of solder tend to form a higher volume of bumps because many solder droplets can participate in forming the bumps on the UBM during the bumping process. As shown in Fig. 3, the solder bump arrays using the SBM with the mixing ratios of 80:20 and 85:15 show solder bumps with excessive volume. In contrast, in the case of a 95:5 mixing ratio, solder bumps with insufficient volume are observed. The solder bump array formed using the SBM with the ratio of 90:10 shows a uniform solder bump array. Its standard deviation is 2.8, which is much smaller than 9.1 and 8.0, the standard deviations of 80:20 and 85:15, respectively.

To understand that the uniformity of the solder bump array depends on the ratio of the resin and solder powder, the SBM on the TSV chip is observed before the cleaning process, as shown in Fig. 4. Large and small solder particles are located in the middle of the resin, and the solder bump array is observed below them. The solder particles are considered resultant of the aggregation of molten droplets of solder during the process. They do not have a chance to join the solder bump array.

Since the tempearture and time during the bumping process are constrained, it seems that there is a specific region near the UBM on a substrate, in which the solder doplets can aggregate on the UBM and form solder bumps. If a solder droplet happens to be outside of the region, it cannot join a solder bump and encounter other droplets to form solder particles in the resin, as shown in Fig. 4(b). The mixing ratio between the resin and solder powder in the SBM determines the number of solder granules in the region. If the ratio is low, many solder droplets can join the solder bumps. If the raio is high, a small

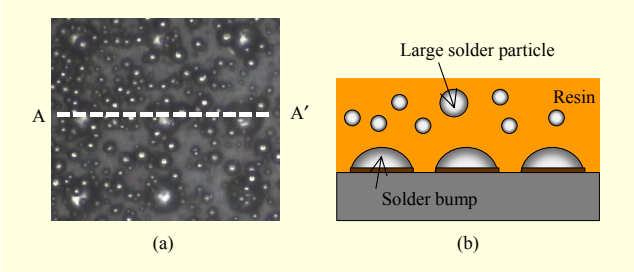

Fig. 4. (a) Photograph of bumping using SBM on Si substrate before cleaning process and (b) schematic diagram of cross-section of A-A' in (a).

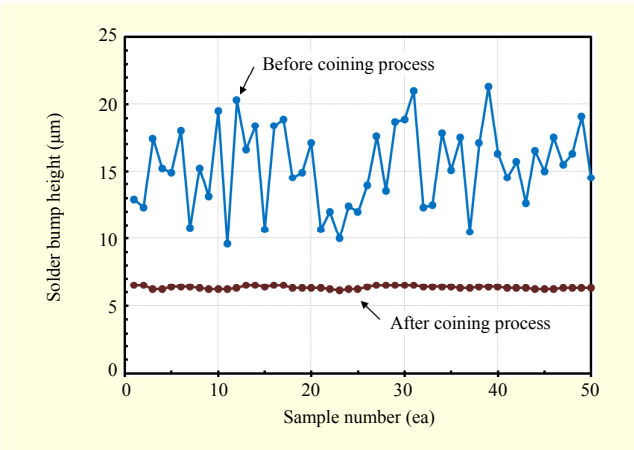

Fig. 5. Measured heights of solder bump before and after coining process.

number of droplets can join the solder bumps, which leads to solder bumps with insufficient volume. In conclusion, there is an optimum mixing ratio between the resin and the solder powder in the SBM to achieve a uniform solder bump array during the bumping process, which depends on the diameters and distributions of solder powder.

Though the optimal mixing ratio between the resin and powder to obtain a uniform bump array is determined, another solution is still needed because the standard deviation of the array is considered large for the stacking process of TSV chips. The coining process used in forming Au stud bump arrays is applied. Figure 5 shows the measured heights of the solder bumps across a Si substrate by an alpha-step. The average heights of the solder bumps before and after the coining process are about 14.6 μm and 6.3 μm, respectively. The standard deviation of the solder bumps is 3.3 μm before the coining process and 0.1 μm after the process. With the coining process, the height difference in the solder bump array is reduced less than ±1 μm, which is appropriate for the stacking process.

Figure 6 shows the cross-sectional SEM images of the solder bumps before and after the coining process and their

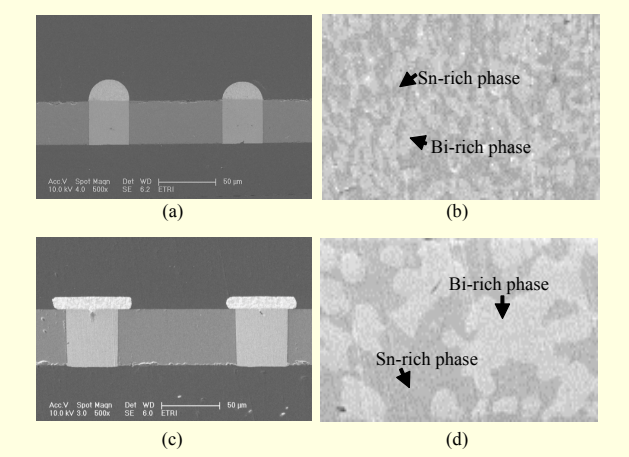

Fig. 6. Cross-sectional SEM images of (a) solder bumps and (b) its microstructure before coining process, and (c) solder bumps and (d) its microstructure after coining process.

microstructures. The shape of a solder bump changes from semicircle to rectangle because of the heat and pressure applied in the coining process. The solder brims over the silicon near the TSV, which may raise a concern that a leakage current can flow through the silicon. However, there is a silicon dioxide layer deposited on the silicon near the TSV that plays the role of an electrical insulation layer so that the solder over the silicon cannot cause an electrical problem. In addition, the brimmed solder has a larger surface area due to the interconnected parts used in 3D IC integration. Therefore, it can help increase the processing tolerance during the alignment and stacking process. The microstructures of the solder bumps before and after the coining process are shown in Fig. 6(b) and (d). The grain sizes in the solder bump before the coining process are relatively uniform, which means that the aggregation of molten droplets in the SBM during the bumping process enables the development of the stable microstructures without irregular grain size and voids in the grain boundaries. After the coining process, the grains in the bumps are coarsened because of the grain growth during the process. This microstructure change, caused by the coining process, is considered to have little effect on the process of the 3D IC integration because the reflow profile applied in the stacking process leads to the development of a fine microstructure of the solder bumps.

Figuire 7 shows the measured DSC and DMA scans of fluxing underfill with a heating rate of 10°C per minute. The chemical reactions of the fluxing underfill occur between 120°C and 200°C. The viscosity of the fluxing underfill slowly decreases 0.1 Pa·s at 160°C, a level of viscosity similar to that of olive oil, which is low enough for fluxing underfill to spread by a capillary force between a chip and a substrate in the stacking process. The viscosity increases sharply above 160°C

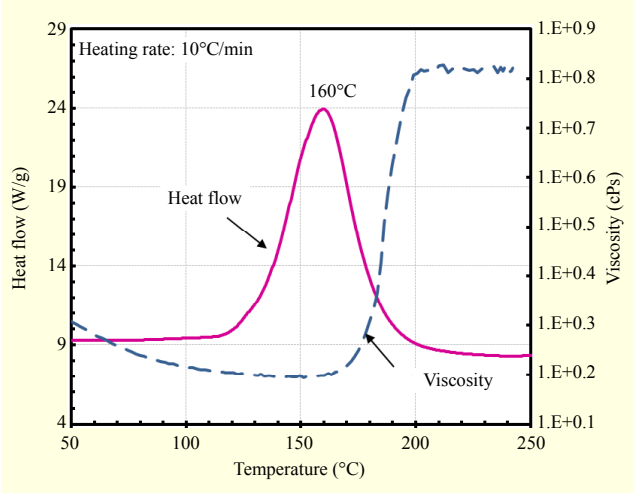

Fig. 7. Dynamic DSC and DMA scans with 10°C/min of fluxing underfill.

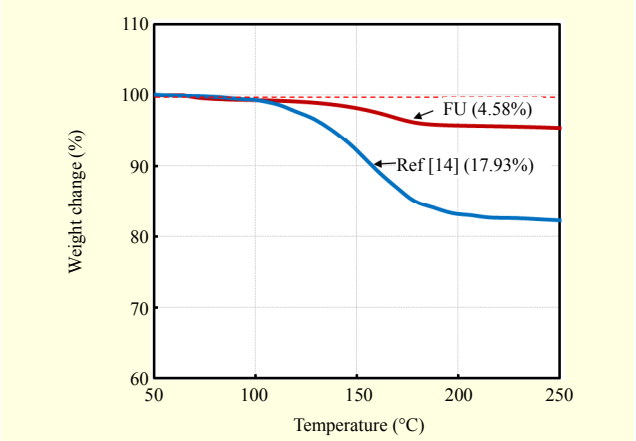

Fig. 8. Weight loss measured by TGA scan of fluxing underfill compared with no-flow underfill in [14].

because of the chemical reactions in the fluxing underfill. The chemical reactions of the fluxing underfill mainly come from the reactions between the epoxy-based thermoset and the hardener, which leads to the curing of the fluxing underfill. Since the heating rate of the reflow profile used in the stacking process is much higher than that used in the DSC, the curing of the fluxing underfill occurs above the melting point of the solder bumps. This sequence is one of the important parameters in designing the hardener. Figure 8 shows the measured TGA scan with 10°C per minute of fluxing underfill and that of a no-flow underfill reported in [14]. The weight loss of fluxing underfill and no-flow underfill begins above 120°C, and the weight loss of fluxing underfill and no-flow underfill at 200°C is about 4.6% and 18.0%, respectively. The amount of the weight loss due to temperature is one of the important factors in that the less weight loss, the less voids form in the underfill during the stacking process. The weight loss of the

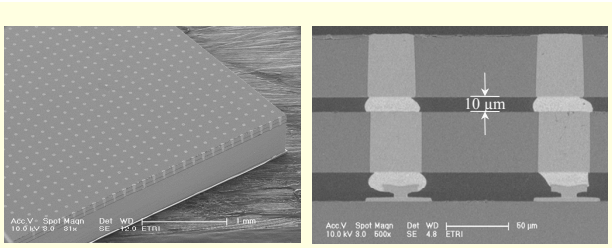

Fig. 9. (a) SBM image of two-tier stacked TSV chips on a silicon substrate and (b) cross-sectional SEM image of (a).

fluxing underfill is small enough to obtain the void-free underfill by the optimization of the stacking process, such as through reflow profiling.

The bumping process using the SBM and the chip-to-chip stacking process using the fluxing underfill are performed with TSV chips and a Si substrate under the developed process conditions. Figure 9(a) shows an SEM image of two-tier stacked TSV chips on a silicon substrate. Its cross-sectional SEM image is shown in Fig. 9(b). Since the gap between the chips is controlled to be about 10 μm, the total thickness of the stacked chip is 130 μm, which is measured from the surface of the substrate. It should be noted that the solder bump has a spherical shape, meaning that the behavior of the solder bump is governed by the surface tension between the solder bumps, fluxing underfill, and exposed Cu on the TSV in the chip during the reflow process. No pressure is applied during the reflow process so that the solder bumps can comply with the surface tension, making possible the effect of the self-alignment during the reflow process. Otherwise, the solders might be squeezed out to be bridged to the adjacent bumps because of the pressure on the TSV chips. This means that the stacking process using fluxing underfill can be simplified, which is made possible by the fact that the deoxidizing agent and additives in the fluxing underfill can reduce the oxide layer on the solder bump array and the exposed Cu on the TSV in the TSV chip simultaneously. Another important advantage of this process is that pressure on a TSV chip is not necessary if the chip does not exhibit exceptional warpage. Therefore, a mass reflow process using fluxing underfill can be applied for the mass production of the 3D IC. Trapped voids in the fluxing underfill are not observed in the stacked chips.

IV. Conclusion

A bumping process using the SBM on a TSV chip was successfully developed by optimizing the volumetric mixing ratio between resin and solder powder and introducing the coining process. The height deviations of the solder bump array

were less than ±1 μm. Its advantages are a maskless process, low-cost process, and no additional surface treatment on the Cu-filled TSV. For a simplified stacking process of the 3D IC integration, the fluxing underfill technology was developed. With fluxing underfill, only three steps are necessary to perform the chip-to-chip stacking process: dispensing of fluxing underfill on a substrate, pick and place of TSV chips, and reflow. Because of its low weight loss with temperature, meaning less out-gassing from the fluxing underfill, no void in the underfill was obtained after stacking two-tier TSV chips on a Si substrate. Using the SBM and fluxing underfill, a low-cost bumping and stacking process can be easily realized.

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