5.2 mW 61 dB SNDR 15 MHz Bandwidth CT ΔΣ Modulator Using Single Operational Amplifier and Single Feedback DAC

Young-Kyun Cho, Bong Hyuk Park, and Choul-Young Kim

We propose an architecture that reduces the power consumption and active area of such a modulator through a reduction in the number of active components and a simplification of the topology. The proposed architecture reduces the power consumption and active area by reducing the number of active components and simplifying the modulator topology. A novel second-order loop filter that uses a single operational amplifier resonator reduces the number of active elements and enhances the controllability of the transfer function. A trapezoidal-shape half-delayed return-to-zero feedback DAC eliminates the loop-delay compensation circuitry and improves pulse-delay sensitivity. These simple features of the modulator allow higher frequency operation and more design flexibility. Implemented in a 130 nm CMOS technology, the prototype modulator occupies an active area of 0.098 mm^2 and consumes 5.23 mW power from a 1.2 V supply. It achieves a dynamic range of 62 dB and a peak SNDR of 60.95 dB over a 15 MHz signal bandwidth with a sampling frequency of 780 MHz. The figure-of-merit of the modulator is 191 fJ/conversion-step.

Keywords: ΔΣ modulator, single operational amplifier resonator, second-order loop filter.

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Young-Kyun Cho (ykcho@etri.re.kr) and Bong Hyuk Park (bhpark@etri.re.kr) are with the 5G Giga Communication Research Labaratory, ETRI, Daejeon, Rep. of Korea.

Choul-Young Kim (corresponding author, cykim@cnu.ac.kr) is with the Department of Electronics Engineering, Chungnam National University, Daejeon, Rep. of Korea.

I. Introduction

Continuous-time (CT) delta-sigma (ΔΣ) modulators have received increasing attention for use in broadband wireless communication systems [1], [2]. Compared with discrete-time modulators, CT ΔΣ modulators have the advantages of lower power consumption and inherent anti-aliasing filtering, exhibiting improved power efficiency and reduced system complexity. Moreover, the CT modulator design alleviates the stringent settling requirement of the operational amplifier (opamp), obtaining feasible input bandwidths of up to a few tens of megahertz with a medium resolution [3]–[8].

The signal-to-quantization-noise ratio (SQNR) and the bandwidth of a CT ΔΣ modulator depends on three main parameters — the loop filter (LF) order, quantizer resolution, and sampling frequency (f_s). Maximizing the modulator bandwidth and achieving a high resolution can be accomplished by increasing the LF order, quantizer resolution, and f_s. However, to achieve a practical bandwidth and resolution in a power-efficient manner, ΔΣ modulator designs have to address several challenging problems.

First, although an increasing LF order is recognized as one of the most effective ways to improve a modulator's SQNR, this approach requires employing more integrator stages with more demanding circuit requirements, which causes a higher power and larger area consumption. Single opamp resonators [3], [9]–[11] have been proposed to overcome these drawbacks, but prior works have difficulty in controlling the resonance condition and the relatively large area for passive elements. Second, multibit designs suffer from digital-to-analog

converter (DAC) nonlinearities. Owing to the inherent mismatch among DAC elements, multibit DACs require complicated DAC shuffling [10] or calibration [4]. Moreover, a finite delay between the quantizer and DAC causes an excess loop delay (ELD). To compensate the ELD, an extra loop comprising a direct path around the quantizer using a summing amplifier and a DAC has been proposed; however, this implementation consumes more power and area [10]. Finally, for CT ΔΣ modulators, a high f_s means that a high opamp bandwidth is inevitable, to reduce the LF delay for stability [12]. The maximum f_s is limited by the parasitic LF pole caused by the LF's input capacitance and the quantizer's latency. Thus, it is known that increasing the f_s of a CT ΔΣ modulator requires either the use of the latest deep-submicron technologies or high power consumption, which does not lead to a power-efficient operation. Nevertheless, one advantage of this approach compared to the former is that it does not require any extra components in the system to compensate for the high-frequency operation. This means that if the number of active elements is reduced and the modulator topology is simplified for a given f_s, then the modulator can be operated in a power-efficient manner. Therefore, reducing the number of opamps, quantizer levels, and DACs during a high f_s operation improves the figure-of-merit of the modulator, reduces the area overhead, and allows more flexibility in the circuit design.

This paper describes a second-order CT low-pass ΔΣ modulator with an internal 1.5-bit quantizer clocked at 780 MHz with an oversampling ratio of 26 to attain a signal-to-noise and distortion ratio (SNDR) of 60 dB. The proposed architecture contains a novel second-order LF that uses a single amplifier and a single trapezoidal-shape half-delayed return-to-zero (HRZ) feedback DAC to reduce the power consumption and die area by minimizing the number of active components and simplifying the modulator topology. Elements that compensate the ELD and DAC mismatch are not needed, further reducing the area and complexity. Implemented in a 130 nm CMOS process, the prototype modulator occupies an active area of 0.098 mm^2 and consumes 5.23 mW power from a 1.2 V supply.

The rest of this paper is organized as follows. Section II presents the architecture of the proposed modulator. Section III describes the details of the circuit design and implementation. Section IV shows the experimental results of the prototype modulator and presents a comparison with prior works. Finally, Section V ends this paper with some concluding remarks.

II. ΔΣ Modulator Architecture

We start our discussion with a general ΔΣ modulator

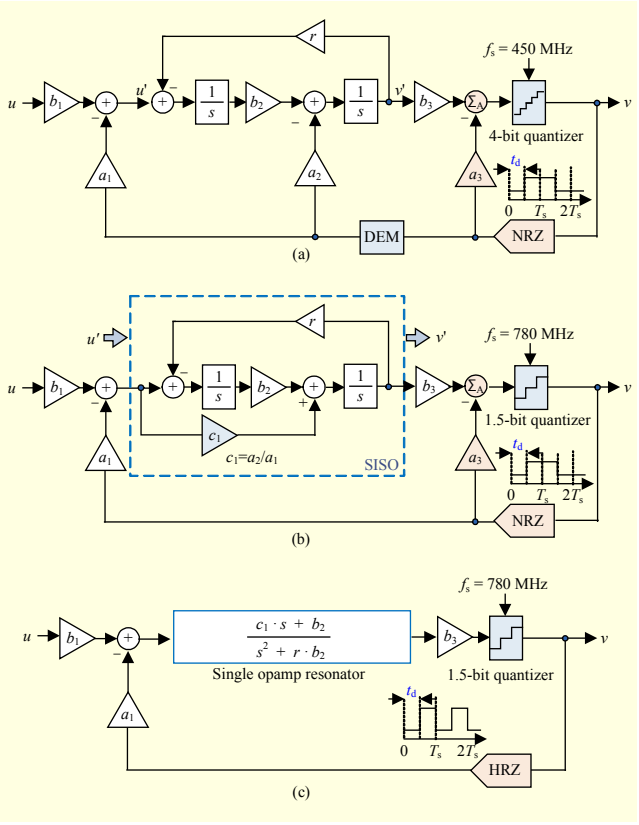

Fig. 1. Second-order CT ΔΣ modulator: (a) conventional feedback architecture, (b) simplified architecture with SISO LF and 1.5-bit quantizer, and (c) proposed architecture with single opamp resonator, 1.5-bit quantizer, and HRZ DAC.

architecture that utilizes a second-order feedback structure with multibit quantizer. Figure 1(a) shows a top-level block diagram of such a modulator. A time delay (t_d) is introduced between the corresponding non-return-to-zero (NRZ) feedback DACs to provide a sufficient decision time for the multibit quantizer. Dynamic element matching (DEM) is applied to decrease the nonlinearity of the feedback DACs (a_1 and a_2). ELD compensation is realized by providing a feedback path around the quantizer using an additional summing amplifier (Σ_A) and a DAC (a_3). The noise transfer function (NTF) zero is implemented by incorporating a feedback coefficient, r. To attain an SQNR of greater than 60 dB in a signal bandwidth of 15 MHz, the f_s of the modulator should be at least 450 MHz. This conventional feedback architecture has three opamps, three DACs, and 15 comparators with DEM as its main components. The use of such a large number of active elements requires significant power and area overhead and makes the circuit design complex. Simplifying the circuit is essential for power-efficient operation with a compact die area and can be achieved by reducing the number of active elements.

To simplify the circuit, we focus on three main aspects. First, two opamps of the first and second LF can be replaced with a

single opamp resonator using a single-input and single-output (SISO) transfer function (TF). To implement the SISO structure, the feedback path to the second integrator input, a_2 in Fig. 1(a), is replaced by the feedforward path, c_1 in Fig. 1(b). The value of c_1 is determined by a loop equation and is calculated as a_2/a_1. The TF for this SISO structure is described through the following equation:

$$H(s) = \frac{v'}{u'} = \frac{c_1 \cdot s + b_2}{s^2 + r \cdot b_2}. \quad (1)$$

Now, the main challenge is to design a single opamp resonator with a suitable resistor and capacitor network, which needs to be consistent with the TF. These procedures eliminate one LF opamp and one feedback DAC. In the next section, we demonstrate the proposed solution with a detailed circuit diagram. Reducing the number of opamps and DACs decreases the power consumption and area of the modulator.

Second, for the same SQNR, the quantization level of the modulator can be reduced through an increase in the sampling rate, as shown in Fig. 1(b). A 4-bit quantizer (15 comparators) clocked at 450 MHz is replaced by a 1.5-bit quantizer (two comparators) clocked at 780 MHz. Although a high f_s requires a high bandwidth opamp, the 1.5-bit quantizer design has several attractive features [13]. The 1.5-bit quantizer decreases the quantization noise by about 6 dB, has a larger stable input range of 1.6 dB compared to a single-bit quantizer, and can be implemented with high linearity. The implementation of the quantizer and feedback DAC is simple, resulting in reduced area and power consumption. A 1.5-bit DAC that is linear, as is a single-bit DAC, is used, thus eliminating the need for any elements to compensate DAC mismatch. This further reduces the circuit's area and complexity.

Finally, Σ_A and a_3, used for ELD compensation, can be eliminated from the circuit by utilizing an HRZ DAC pulse, as explained herein. A problem encountered when using a conventional NRZ DAC pulse is that any delay, $t_d > 0$, pushes the falling edge of the DAC pulse beyond the clock period, T_s. As a result, the second-order modulator actually becomes a third-order LF, which leads to a reduced stability and relatively poor noise-shaping performance, thus necessitating ELD compensation circuitry. To address this problem, one solution suggested in [14] is to use an HRZ pulse instead of an NRZ pulse, as shown in Fig. 1(c). When an HRZ DAC pulse is used, the falling edge of the DAC could remain inside T_s; the LF then remains of second order. Therefore, Σ_A and a_3 are not needed, improving the efficiency in terms of both power and area. The HRZ DAC also suppresses the inter-symbol interference problem caused by unequal rising and falling edges of the feedback DAC waveform. However, a HRZ DAC pulse is more sensitive to clock jitter. For a 60 dB SNDR target with the HRZ DAC, the root-mean-square jitter requirement of the proposed modulator is calculated to be about 5 ps (0.4% relative to the clock period) by [15], which is stringent but similar to the requirement of current state-of-the-art single-bit modulators [5]–[7] and is acceptable in a system with a high-precision clock source. Considering these three aspects, the architecture of the proposed modulator is as shown in Fig. 1(c).

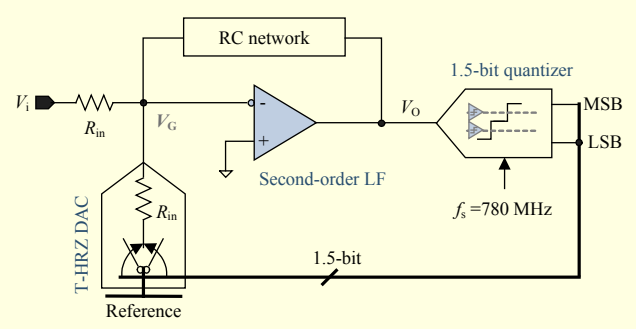

Fig. 2. Block diagram of implemented CT ΔΣ modulator.

III. Circuit Implementations

A circuit-level block diagram of the implemented CT ΔΣ modulator is shown in Fig. 2. The main components of the modulator are a second-order LF, a 1.5-bit quantizer, and a trapezoidal-shape HRZ DAC in a feedback loop. One can immediately notice the simplicity of this structure — active components consist of just one opamp, one DAC, and two comparators. The simplicity of this circuit allows a high-speed operation of 780 Ms/s with a compact area and low power consumption. The circuit implementation details of the key building blocks of the modulator are discussed next.

1. Loop Filter

The LF, the main building block in CT ΔΣ modulators, consumes most of the power and area of the system. The number of opamps is generally equal to the order of the LF in active RC-based LFs [16], [17]. Thus, the power consumption of the LF can be reduced by decreasing the number of amplifiers for a desired order. As described in the previous section, it is a second-order LF with resonating TF and single opamp that facilitates this configuration.

The proposed single-opamp second-order LF with a fully differential structure is illustrated in Fig. 3 [18]. The LF output applied to C_2 through the cross-coupled connection from the opposite terminal removes the first-order Laplace term in the denominator. The transfer function of this LF is calculated through the following equation:

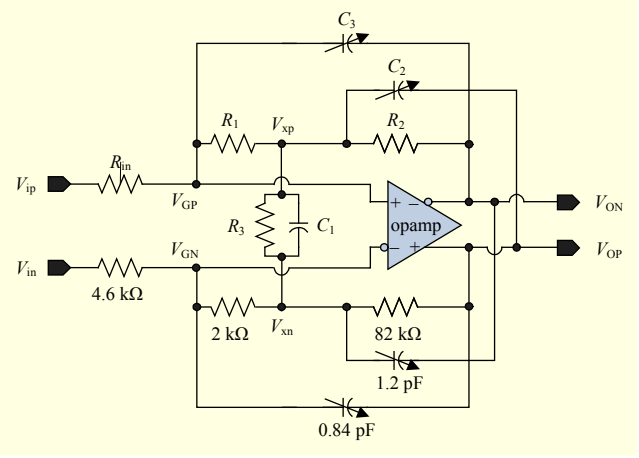

Fig. 3. Proposed single-opamp resonator with fully differential structure.

$$\frac{V_o}{V_i}=\frac{1}{\left(C_1C_3+C_2C_3\right)R_{in}}\times\frac{\left(C_1+C_2\right)s+\left(1/R_1+1/R_2+1/R_3\right)}{s^2+\left(1/\left(C_1+C_2\right)C_3R_1R_2\right)}. \quad (2)$$

This equation has the same form as (1) and includes a resonating condition that appears from the first-order Laplace term in the denominator. The conditions are determined as follows:

$$C_2\left(R_2R_3\right)=C_3\left(R_1R_2+R_2R_3+R_3R_1\right). \quad (3)$$

The proposed structure has many advantages compared to earlier works [3], [9]–[11]. First, the resonating condition can be effectively controlled using the feedback capacitors of C_2 and C_3 because the capacitors are separated and operated independently. Second, C_3 and R_3 change the poles and zero independently; thus, it is easy to calibrate the transfer function of the LF. In addition, the parasitic capacitance and resistance at the internal node V_x is easily controlled by capacitor C_1 and resistor R_3, which can reduce the parasitic effects of the internal node. Finally, despite the more complicated structure, this proposed LF exhibits a relatively smaller total capacitance and resistance by about 30% at the same f_s. On the basis of these results, we conclude that the proposed LF architecture is more suitable for many purposes, especially for low-power and small-area applications with high controllability as compared with conventional LFs.

An important design consideration for CT modulators is that the LF coefficients depend on the absolute RC values. A large RC time-constant variation introduces a mismatch between the analog noise-shaping transfer function and digital noise-cancellation characteristics, causing a significant deterioration of the SNDR [19]. Figure 4 shows the maximum achievable SQNR of the proposed ΔΣ modulator versus the normalized RC product. If the normalized RC product is greater than 1.0,

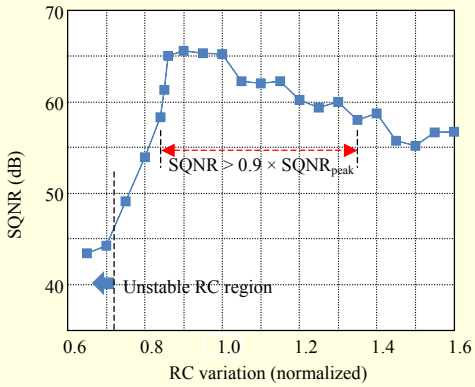

Fig. 4. SQNR vs. normalized RC product.

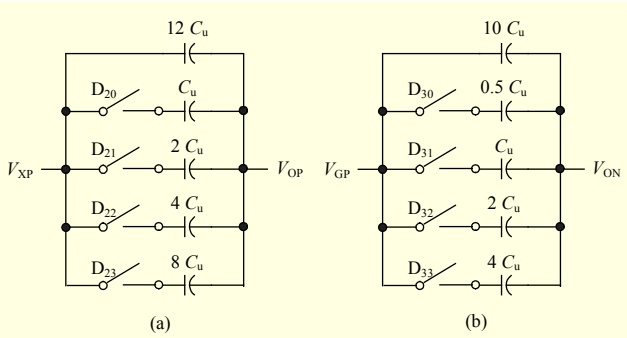

Fig. 5. Tunable capacitor banks: (a) C_2 and (b) C_3.

then the loop gain decreases so that the SQNR drops gradually. When the normalized RC product decreases by more than 25%, the loop becomes unstable. For a normalized RC constant ranging from 0.85 to 1.35, the modulator can achieve more than 90% peak SQNR performance. To extend the tolerable RC time-constant variation and control the location of the NTF zero point, the capacitors C_2 and C_3 comprise a 4-bit binary-weighted tunable capacitor bank, as shown in Fig. 5. These banks are controlled externally based on the signal transfer function and can compensate for RC shifts of up to 30% from the nominal values, thereby minimizing the process-dependent RC time-constant variations. The nominal values of C_2 and C_3 are 1.2 pF and 0.84 pF, respectively, with a unit capacitance (C_u) of 60 fF.

As the modulator uses only one opamp, the gain–bandwidth product (GBW) requirement is determined based on the linearity characteristic of this opamp. Figure 6 shows the simulated SQNR over a finite GBW variation. The DC gain and unity–gain bandwidth of the opamp required to reach about a 60 dB SQNR are 55 dB and 1.15 GHz, respectively. It has been shown that a unity–gain bandwidth of about 1.5 f_s is already sufficient for tackling the linearity problem.

To satisfy the GBW requirement, the opamp employs a two-stage topology with feedforward-compensation [20], as shown

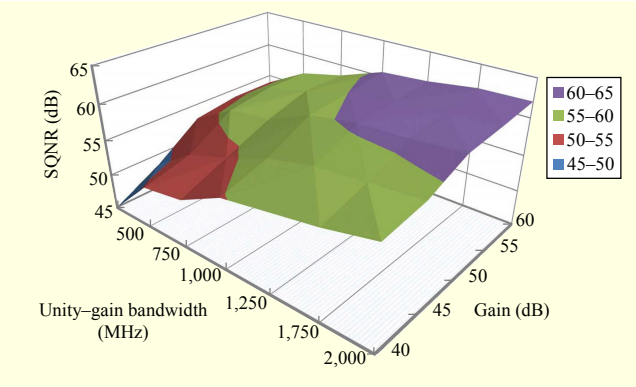

Fig. 6. SQNR vs. finite gain-bandwidth variation.

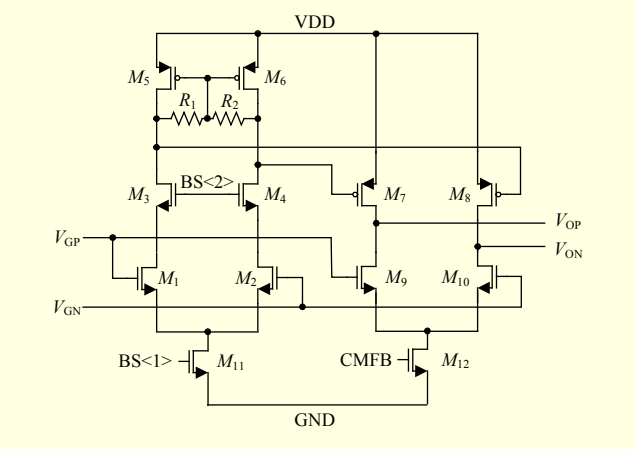

Fig. 7. Opamp with feedforward compensation scheme.

in Fig. 7. The feedforward compensation scheme is more power efficient than a Miller-compensated structure, because current is not wasted in charging and discharging a compensation capacitor. The NMOS input transistors, M_1, M_2, with cascode transistors, M_3, M_4, and load transistors, M_5, M_6, form the input stage of the amplifier, whereas transistors M_7–M_{10} constitute the output stage. Transistors M_9 and M_{10} produce a high-frequency feedforward path between the input and output, thus stabilizing the amplifier. The common-mode voltage of the input stage is sensed by resistors R_1 and R_2, which are used to set the common-mode gate voltages of M_7 and M_8. The common-mode voltage of the output stage is controlled by an auxiliary common-mode amplifier (not shown in Fig. 7), which controls the current source, M_{12}. The designed opamp achieves a 57 dB DC gain and 1.25 GHz unity–gain bandwidth under full load conditions while consuming 1.96 mA from a 1.2 V supply.

2. 1.5-bit Quantizer

The 1.5-bit internal quantizer shown in Fig. 8 is realized by two comparators with the corresponding sample-and-hold

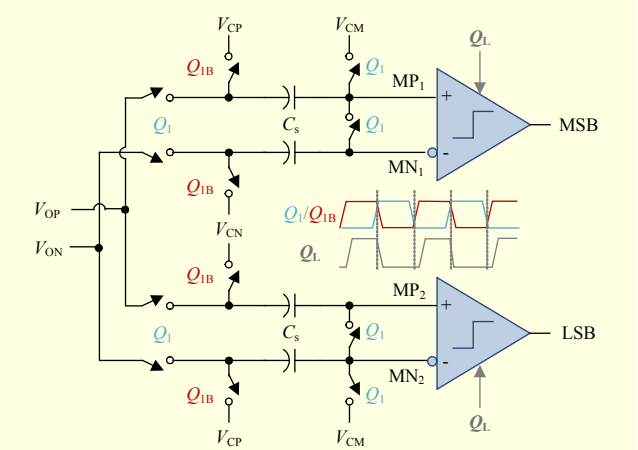

Fig. 8. 1.5-bit quantizer with sample-and-hold circuit.

(S/H) circuits. The differential outputs of the LF (V_{OP} and V_{ON}) are sampled with S/H circuits by the 780 MHz master clock and are regenerated by the comparators. As the output range of the LF is only one-third of the full-scale range, the reference voltages to the quantizer only span one-third of the input full-scale range; that is, V_{CP} = 642 mV and V_{CN} = 558 mV. The reference voltages are subtracted from the output voltages of the LF by means of the switched sampling capacitors of C_s at the inputs of the comparators. Here, C_s must be chosen carefully because this capacitor and its parasitic capacitance contribute to the load seen by the LF. For the 25 fF of C_s, a simulation with the sampling circuit shows that the overall input-referred offset of the comparator under the worst case is less than half a least significant bit (LSB). The S/H circuits and comparators use a single phase clock [21], avoiding the need to generate non-overlapping clocks at high speeds. This reduces the power consumption in the clock-generation circuitry.

The comparator circuit used in the quantizer, shown in Fig. 9, is based on a regenerative latch. As a dynamic latch does not consume static current, it is suitable for an energy-efficient design. To speed up the comparator, we add a separate regenerative branch along with the output branch [8]. This additional latch helps the dynamic latch to turn on rapidly from the reset phase by discharging the output node more quickly; in addition, it reduces the latching delay. The operation of the comparator is described as follows. When the latching clock (Q_L) is low, the comparator is inactive and both outputs (OP and ON) are reset to VDD. Transistors M_9 and M_{12} are switched off and the comparator does not dissipate static power. As soon as Q_L becomes high, the differential pair, M_1 and M_2, compares the two input voltages. The latch regeneration forces one output to high and the other to low according to the comparison results. The additional latch improves the regeneration speed by about 10%. With the flag signal (FLG),

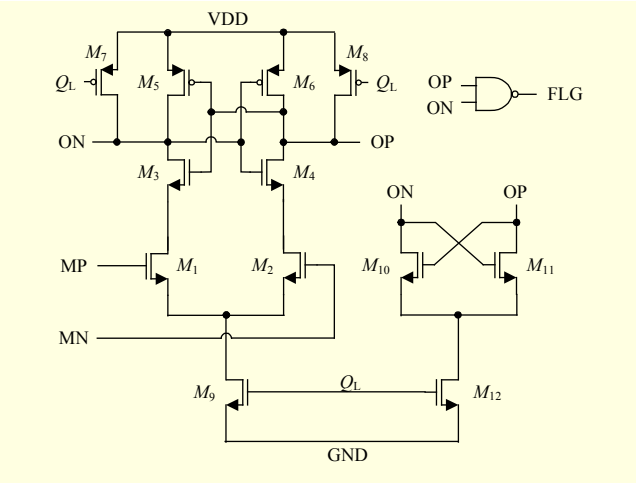

Fig. 9. Regenerative latch.

the output of the comparator is transferred to the feedback DAC.

3. Trapezoidal-Shape Feedback DAC

Figure 10(a) shows a schematic of the proposed 1.5-bit feedback DAC, which employs a switched-resistor scheme [16]. An HRZ topology is chosen for the DAC to provide additional compensation of ELD introduced by the quantizer, and to minimize the impact of inter-symbol interference at a high f_s. The trapezoidal pulse shape [22] is also adopted in the proposed DAC to reduce the pulse-delay sensitivity by controlling the discharge time. The architecture has an additional benefit of reducing the typically high switched-capacitor DAC output peak currents, resulting in reduced slew-rate requirements for the LF integrator. Further details of the DAC structure and operation are discussed next, with a timing diagram shown in Fig. 10(b) (which was generated from transistor-level simulations).

The proposed DAC switches its operation mode between "active" and "inactive" depending on the main clock (Q_{1B}) and outputs of the comparators (MSB and LSB). When Q_{1B} is low and MSB and LSB have the same value, the DAC operates in active mode. Active mode can be further divided into two operation phases — constant-current and exponential-discharge phases. In the constant-current phase, depending on the output data of the comparators, nodes V_P and V_N are switched to V_{REFN} or to V_{REFP}, through switches M_1–M_4. Because the digital data from the quantizer can arrive at arbitrary times within a sample period, NAND gates (N_1 and N_2) are used to enable the data and generate differential data signals. The data-dependent DAC output voltage is converted into a current by R_{in}, resulting in a positive or negative feedback current, I_{DAC}. The input resistor R_{in} in the DAC was

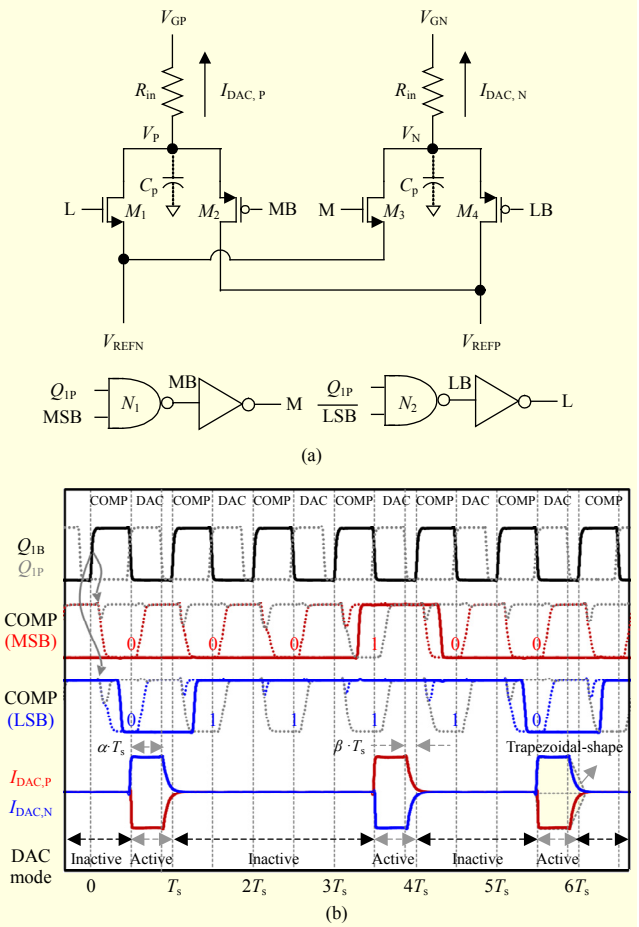

Fig. 10. HRZ Feedback DAC: (a) circuit diagram and (b) simulated timing diagram of quantizer and DAC.

designed with the same value as the LF's input resistor so as to be immune against a device mismatch. The feedback current is subtracted from the input current at the virtual ground node (V_{GP} and V_{GN}) and integrated on the capacitors of the LF. This phase is held constant from $T_s/2$ to $T_s/2 + \alpha \cdot T_s$ during one period. In the discharging phase, V_P and V_N are not connected to any reference voltage, and the output current of the DAC is exponentially discharged to the zero level with a time constant of $R_{in} \cdot C_p$ ($= \tau$), where C_p is the parasitic capacitor at nodes V_P and V_N. This phase maintains the falling edge of the Q_1 prime clock (Q_{1P}) to T_s. Therefore, the DAC current has a trapezoidal pulse shape in active mode, as shown in Fig. 10(b).

In [16], this feature is pointed out as a drawback. However, by virtue of Q_{1P}, the current tail stays within a single clock period, resulting in an improvement of the sensitivity of the pulse delay, which could be induced from the clock and DAC driver. In Fig. 11, the effect of the pulse delay on the modulator with the proposed DAC is simulated and compared with that on the conventional HRZ DAC. With a pulse delay of $0.1T_s$, the proposed DAC improves the SQNR by about 3 dB

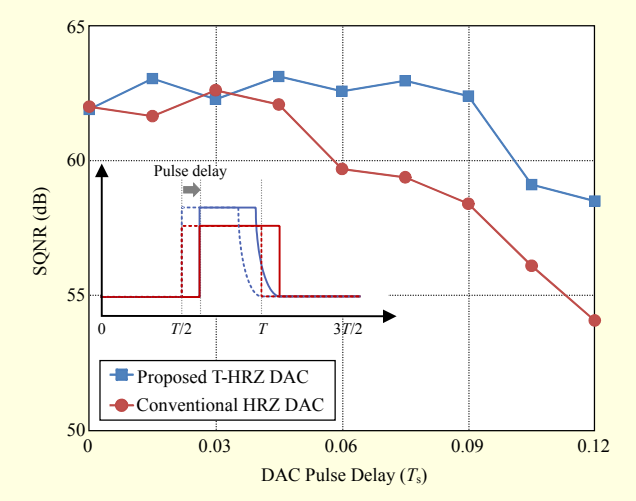

Fig. 11. DAC pulse-delay effect on modulator.

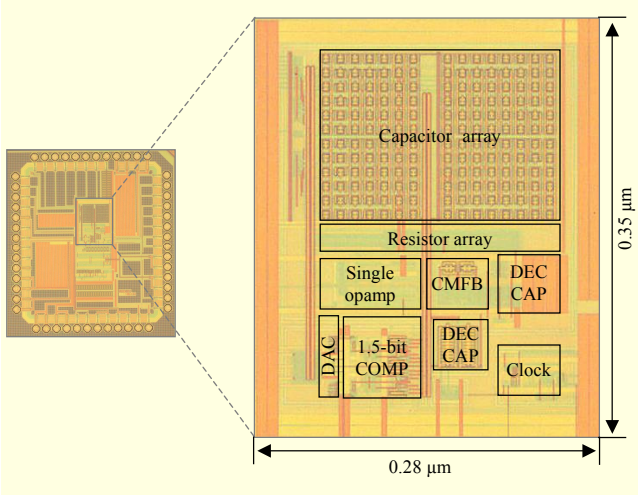

Fig. 12. Chip photograph.

compared with that of the conventional HRZ DAC owing to the exponentially decaying tail of the current.

When Q_{1B} is high or MSB and LSB are "0" and "1," respectively, the DAC operates in inactive mode. During the inactive mode, nodes V_P and V_N are not connected to any reference voltage, but are open-circuited and left floating. Therefore, the currents flowing from the internal nodes to the virtual ground node is zero. As the output currents of the DAC are reset to zero in every Q_{1B} phase, signal-dependent charges may not be stored in C_p, thus minimizing the impact of inter-symbol interference.

IV. Measurement Results

A prototype chip was implemented in a 130 nm 1-Poly 8-Metal CMOS process with metal–insulator–metal capacitors. Figure 12 shows a photograph of the chip and its active area. The active area of the modulator is only 0.098 mm^2, including power supply decoupling capacitors and the guide ring. The capacitor and resistor arrays occupy 57% of the active area, and the remaining circuit, including the opamp, comparators, and DAC, occupies only 27% of the core area. To reduce the effect of parasitic capacitances and resistances, high-speed blocks are placed close to each other. At 780 Ms/s, the modulator consumes 5.23 mW from a 1.2 V supply. By reducing the number of active components used, the power consumption of the modulator can be reduced significantly. In our prototype, power is consumed mostly by the LF and quantizer. The LF and quantizer use about 45% and 37% of the power, respectively.

The output data stream of the modulator was captured through a high-speed oscilloscope and the post-processing of the data was performed with MATLAB. As mentioned earlier,

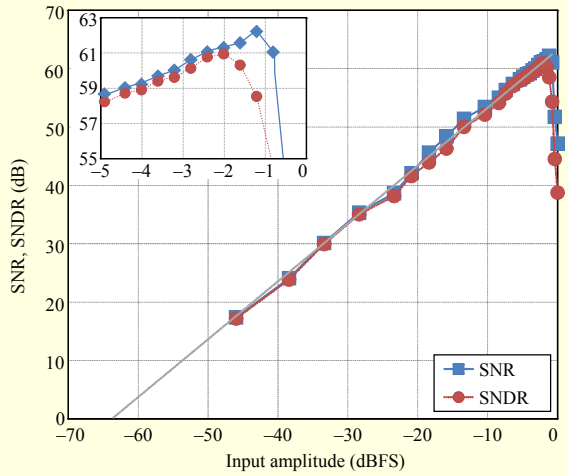

Fig. 13. Measured SNR and SNDR vs. input power at 780 Ms/s and 15 MHz bandwidth.

the problem of clock jitter, which strongly influences the SNDR of any high-speed CT ΔΣ modulator architecture, was addressed by using a low-noise, off-chip clocking source. The measured signal-to-noise ratio (SNR) and SNDR for different input signal powers are plotted in Fig. 13. A peak SNR of 62.22 dB is achieved at an input of −1.2 decibels relative to full scale (dBFS), whereas a peak SNDR of 60.95 dB is obtained at a −2 dBFS input. The full-scale signal (0 dBFS) refers to a sine wave at the input with a 1 $V_{p\text{-}p}$ differential. The modulator achieves a 62 dB dynamic range in a 15 MHz signal bandwidth.

Figure 14 shows a 131,072-point fast-Fourier-transform output spectrum of the modulator with an input of −2 dBFS at 1 MHz. The second-order noise shaping is visible from 10 MHz to 100 MHz. Because the input signal frequency is 1 MHz, up to the 14th harmonics of the input signals are

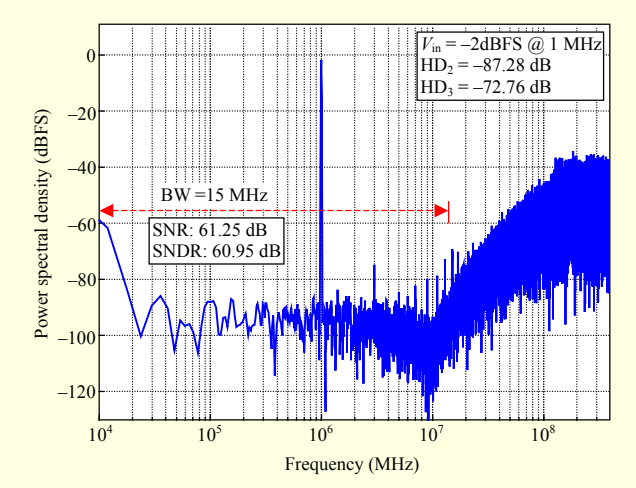

Fig. 14. Measured output spectrum (131,072 points) of modulator.

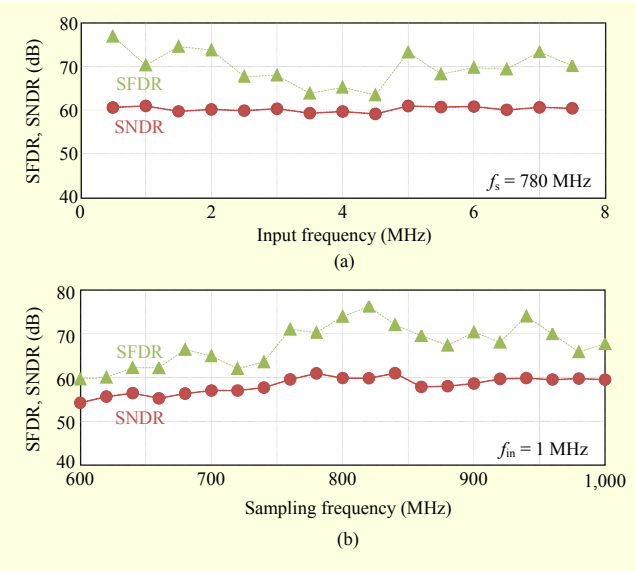

Fig. 15. Overall dynamic performances.

included in the output spectrum. The third-order harmonic distortion (HD_3) is 73 dB below the signal tone, which demonstrates the high linearity properties of both the LF and the DAC. The measured SNR is 61.25 dB and the spurious-free dynamic range is 72.76 dB over the 15 MHz signal bandwidth.

The overall dynamic performance is summarized in Fig. 15. It can be seen that the dynamic performance does not deteriorate when the signal frequency is increased up to the Nyquist input bandwidth. Beyond the Nyquist bandwidth, the measurement is not performed, because the harmonics cannot be included in the output spectrum. The performance of the prototype was also measured over f_s from 600 MHz to 1000 MHz without any reconfiguration of the prototype. The

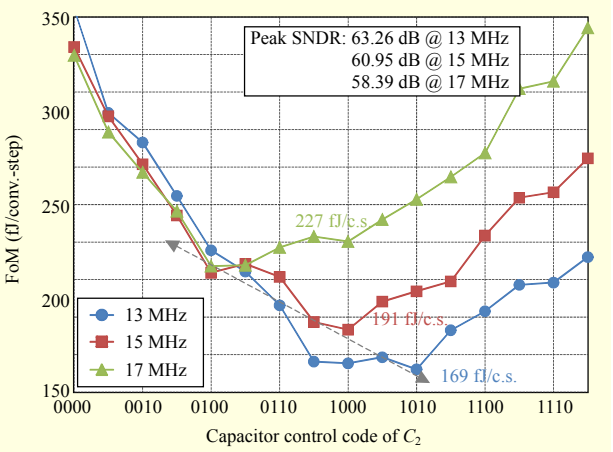

Fig. 16. Measured FoM vs. C_2 variation.

performance is almost constant with the sampling frequency at up to 1,000 MHz but should be improved further because of the high oversampling ratio. A simulated SQNR of 68 dB can be achieved at 1,000 MHz f_s. However, the limitations (that is, a mismatch of the transfer function, the GBW requirement of the LF, and the regeneration time of the comparator) may cause significant performance deterioration at 1,000 MHz f_s.

The location of the NTF zero point and the transfer function of the LF can be changed through the capacitances of C_2 and C_3 in the LF. If C_2 and C_3 have smaller values, then the poles and zero of (2) shift to a higher bandwidth. Therefore, to have a peak figure-of-merit (FoM) in a given signal bandwidth, the control codes of C_2 and C_3 are moved to the opposite direction of the signal bandwidth variation. Figure 16 shows the measured FoM versus the value of C_2. Here, C_3 was set to achieve a peak SNDR. The FoM is defined as follows:

$$\mathrm{FoM} = \frac{P_w}{2^{\mathrm{ENOB}} \cdot \left(2 \cdot f_{\mathrm{BW}}\right)}, \tag{4}$$

where P_w is the power consumption of the modulator, ENOB is the effective number of bits, and f_{BW} is the signal bandwidth.

The modulator produces a peak SNDR of 63.26 dB within a bandwidth of 13 MHz at C_2/C_3 = 1010/1000, a peak SNDR of 60.95 dB within a bandwidth of 15 MHz at C_2/C_3 = 1000/0101, and a peak SNDR of 58.39 dB within a bandwidth of 17 MHz at C_2/C_3 = 0100/0010. The prototype modulator achieves a peak FoM of 169, 191, and 227 fJ/conversion-step in a 13 MHz, 15 MHz, and 17 MHz signal bandwidth, respectively. Table 1 shows a comparison between the proposed ΔΣ modulator and recently reported modulators implemented using similar technologies. The prototype modulator occupies less area, and a measured FoM of nearly 200 fJ/conversion-step is shown to be very competitive when compared with that of other current state-of-the-art modulators.

Table 1. Performance table and comparison to prior works using similar technologies.

Ref.	Order	# of bits	f_s (MHz)	BW (MHz)	SNDR (dB)	ENOB (bits)	Power (mW)	Size (mm^2)	Tech. (nm)	FoM (fJ/conv.-step)	Note
[1]	3	4	640	20	74.00	12.0	20.00	8.60	130	122	Multi-bit
[3]	5	3	300	10	62.50	10.1	5.32	0.32	110	244	
[10]	4	4	185	7.2	76.80	12.5	13.70	1.30	130	168	
[11]	3	3	300	8.5	67.20	10.9	4.30	0.12	90	135	
[5]	4	1	1,000	15.6	59.80	9.6	4.00	0.38	130	161	Single-bit or 1.5-bit
[6]	3	1	640	10	65.00	10.5	6.80	0.40	90	234	
[8]	3	1	404	17	58.60	9.4	25.20	0.10	130	1,066	
This work	2	1.5	780	13	63.26	10.2	5.23	0.10	130	169	1.5-bit
				15	60.95	9.8				191	
				17	58.39	9.4				227	

V. Conclusion

This work demonstrates the implementation of a second-order CT ΔΣ modulator in a 130 nm CMOS technology that achieves a 60.95 dB SNDR and 62 dB DR over a 15 MHz signal bandwidth with 780 MHz f_s. The modulator occupies an active area of 0.098 mm^2 and consumes 5.2 mW power from a 1.2 V supply. This CT ΔΣ modulator is one of the smallest among the reported ΔΣ modulators. It also achieves an FoM of 191 fJ/conversion-step, which is one of the lowest rates achieved in high-speed single and 1.5-bit designs. These characteristics are mainly attributed to a reduction of the active components with the corresponding circuit techniques. With a single-opamp resonator, two opamps of the second-order LF can be reduced by one, yielding better controllability of the zero and pole of the transfer function. The pulse delay sensitivity of the feedback DAC can be improved by adopting a trapezoidal-shape HRZ feedback topology. In addition, the proposed architecture does not require any additional building blocks to compensate both the ELD and the DAC mismatch. Therefore, the presented modulator can allow a power-efficient operation along with the benefits of a compact area and flexible design.

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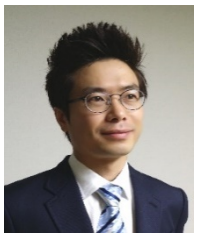

Young-Kyun Cho received his BS degree from Ajou University, Suwon, Rep. of Korea, in 2001 and his MS degree from POSTECH, Pohang, Rep. of Korea, in 2003, both in electrical and electronics engineering. He is currently working as a senior researcher at ETRI and is pursuing his PhD degree in electrical engineering at Chungnam National University, Daejeon, Rep. of Korea. His research interests are novel devices; mixed-signal circuits; Nyquist and oversampling rate ADCs; and transceivers. He was the recipient of the Best Paper Award at the IEEE Nanotechnology Materials and Devices Conference in 2006 and was twice awarded the Minister of Knowledge Economy and President Prize of Rep. of Korea at the National Semiconductor Design Contest in 2009 and 2014, respectively.

Bong Hyuk Park received his BS degree in electrical engineering from Kyungpook National University, Daegu, Rep. of Korea, in 1996; his MS degree in mechatronics from Gwangju Institute of Science and Technology, Rep. of Korea, in 1998; and his PhD degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 2010. From 1998 to 1999, he was an RF application engineer with Ansoft Corporation, Seoul, Rep. of Korea. Since 1999, he has been with ETRI. His main research interests are ultra-wideband RF transceiver front-end circuit design, fractional-N phase-locked loop design, system-level integration of transceivers, and 5G RF technology.

Choul-Young Kim received his BS degree in electrical engineering from Chungnam National University, Daejeon, Rep. of Korea, in 2002 and his MS and PhD degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 2004 and 2008, respectively. From March 2009 to February 2011, he was a postdoctoral research fellow at the Department of Electrical and Computer Engineering, University of California, San Diego, USA. Currently, he is working an assistant professor of electronics engineering at Chungnam National University. His research interests include RF/mm-wave integrated circuits and systems for short-range radar and phased-array antenna applications, and analog front-end readout integrated circuits for radar applications.