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Origin of the dry etch damage in the short-channel oxide thin-film transistors for high resolution display application

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ABSTRACT

The demand for high-resolution displays with fine pitch has been continuously increased. Source/drain (S/D) dry etching is indispensable when defining very narrow patterns, but back-channel damage is inevitable when it is carried out, which can lead to deterioration in the performance of devices made with them. Nevertheless, thorough analysis on the etch damage was not yet conducted in depth. In this study, the phenomenon and the reason of etch damage occurring in S/D dry etch procedure of back-channel-etched oxide thin-film transistors were evaluated. Right after S/D dry etching process, small amount of molybdenum (S/D metal) and chlorine (main etching gas) were detected on the back-channel surface. The changes in the chemical bonding state of the back-channel surface and the resulting degradation of device performance were examined in detail. Furthermore, a highly efficient wet treatment method was introduced to restore the etch damage. By doing so, all of the device characteristics were notably enhanced compared to a device not subjected to the wet treatment process.

1. Introduction

Over the past decade, amorphous oxide semiconductors (AOSs) have been in the spotlight as good switching unit candidates for thin-film transistor (TFT) backplanes in active matrix flat panel displays because of their superior characteristics [1–4]. Moreover, the AOS field has continued to evolve through studies on channel layers based on double-layered channel and super-lattice structure, and on passivation layers through optimization of various materials and process conditions [5–13]. As the display industry evolves, the demand for high-resolution displays also continues to grow. Self-aligned devices have been thought as good candidates for switching units for high-resolution displays with small pixel pitches due to their small footprint and low parasitic capacitance based on near-zero gate to source/drain (S/D) overlap [14–17]. However, since the aperture ratio decreases at the same time as the pixel pitch decreases, the importance of reflective-mode devices for ultra-high resolution panel has been increased considerably. For this reason, back-channel etch (BCE) structures capable of transporting data voltage to the reflection layer are more necessary than self-aligned top-gate device.

In the past, transistors were easily patterned by highly selective wet etching process because the pixel pitch of the display was large at over tens of micrometers [10,18]. Recently, there has been intense demand for higher resolution displays with very small pixel pitches such as near-eye light field display, head-mounted display or spatial light modulator for digital holography. Nevertheless, it is difficult to use wet etching method to define fine patterns because of their isotropic characteristics, and so it has become necessary to introduce anisotropic dry etching scheme. Unlike wet etching with a high selectivity ratio, dry etching process involves not only chemical but also physical action, which inevitably causes damage to the back-channel of the BCE transistor, and it directly degrades the device performance as well. Sub-threshold slope, field-effect mobility, and reliability of the transistor can be deteriorated. Nevertheless, an in-depth study of how the back-channel impairment occurs and why this etch damage degrades the device performance has not yet been conducted. The dry etch damage for etch stop BCE TFT was reported in 2016 [19], There is no report in regard to the direct influence of S/D dry etch damage on the back channel surface of the BCE TFT. The etch damage may be a serious obstacle to the implementation of ultra-fine devices with sub-micron channel lengths. Therefore, it is necessary to analyze and solve the problem.

In this study, the origin of S/D dry etch damage on the back-channel surface of BCE oxide TFT was demonstrated. It was confirmed by analyses on the composition and bonding structure of the back-channel surface after the S/D dry etching process. In addition, the effect of these problems of the back-channel surface on the electrical properties of

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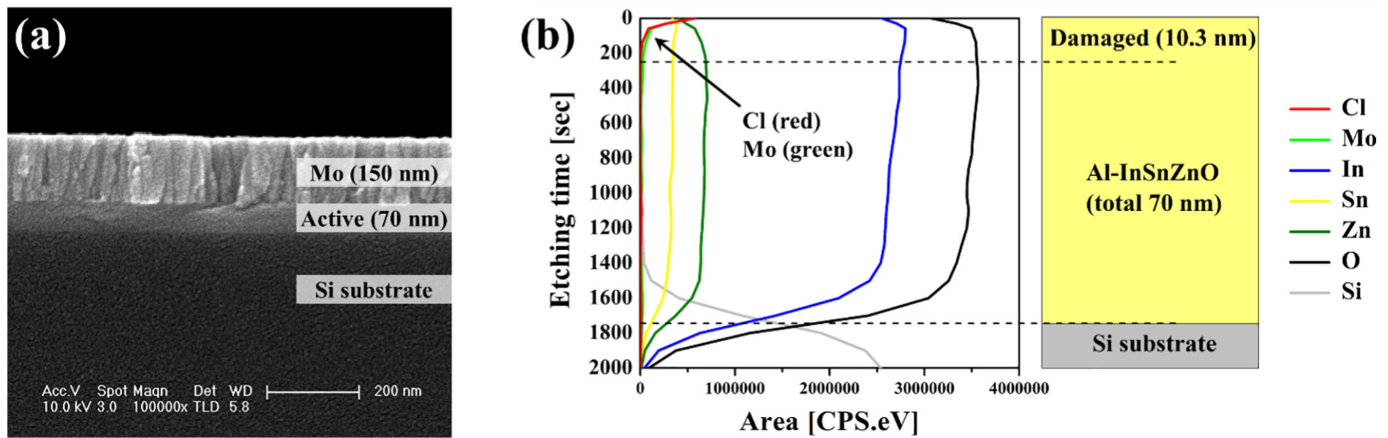

Fig. 1. (a) A thin-film laminated structure fabricated in order of silicon substrate-active material-molybdenum (Mo). (b) Depth profile of active layer after Mo dry etching process. Mo and Cl were detected at the back-channel surface.

device was also examined. Finally, a highly effective wet treatment process was introduced, which improved the device performance remarkably. On the basis of wet treatment, a high-performance back-channel-etched oxide TFT with 2-μm channel length was fabricated.

2. Experimental details

To verify the status of the back-channel surface after S/D dry etching step, a simple thin-film laminated structure of Si substrate-metal oxide film for active material in the transistor-molybdenum (Mo) for S/D metal sequence was fabricated as shown in Fig. 1(a). For the active material (channel layer) formation, 70-nm-thick aluminum-doped indium-tin-zinc-oxide (Al-InSnZnO) film was deposited by RF sputtering under process pressure of 0.08 Pa and power of 400 W with a gas flow of 40% O_2/(Ar + O_2) atmosphere. Meanwhile, the S/D layer was dry etched with a mixture of chlorine (Cl) and oxygen gases at the pressure of 1.33 Pa. After the metal dry etching procedure, a depth profile analysis was conducted on the open back-channel surface.

The depth profile analysis at the back-channel surface after S/D dry etching process was conducted by Auger electron spectrometry (AES). The AES measurement was conducted through MICROLAB 350 equipment with field emission gun (10 kV, 1.5 nA, 12 nm) under 6.65×10^{-7} Pa of base pressure. Constant retard ratio energy mode was used. The microscopic image was obtained by scanning electron microscopy through FEI SIRION 400 equipment with 10 kV of operating voltage. The element analysis was conducted by energy-dispersive x-ray spectroscopy (EDS) measurements through XFlash Detector 4010 equipment from Bruker with 15 kV condition. The chemical bonding states of the devices were analyzed by X-ray photoelectron spectroscopy (XPS) and the binding energies were calibrated using the carbon 1 s peak (284.5 eV). The XPS measurement was conducted through ESCALAB 200R equipment with 5 keV/5 mA Ar^+ ion beam under 6.65×10^{-7} Pa of base pressure. Concentric hemispherical analyzer and constant analyzer energy mode were used. For the peak fitting, Advantage analysis software was used with Gauss-Lorentzian function. Background was linear. The detailed information of X-ray source was Al-Kα (1486.6 eV), 12.5 kV, 20 mA and 250 W. The dataset were referenced by Au 4f (84 eV). The full width half maximum of the synthetic peaks between spectrums were matched.

Two types of devices were fabricated to clarify the effect of wet treatment to electrical characteristics of oxide TFTs. One was subjected to the wet treatment, and the other was not. In this work, an inverted staggered BCE configuration was adopted for oxide TFT fabrication. 150-nm-thick DC-sputtered Mo was used for the gate, source and drain electrodes, while 100-nm-thick silicon dioxide (SiO_2) grown by plasma-enhanced chemical vapor deposition (PECVD) at 380 °C was employed as the gate dielectric layer. For the active material, 70-nm-thick Al-InSnZnO film was deposited. After S/D patterning, back-channel region of one device was treated by dipping the device into an oxalic-acid-based active wet etchant solution for 10s. For the passivation layer, 100-nm-thick SiO_2 was deposited by PECVD at 300 °C. Finally, the fabricated TFTs were annealed at 200 °C for 2 h under vacuum condition. All the layers were patterned by stepper-based photolithography and dry-etching process to define the short-channel transistor. The defined channel width (W_{CH}) and length (L_{CH}) in this work was 2/2 μm. The electrical characterization was obtained with an Agilent B1500A semiconductor parameter analyzer. The field-effect mobility (μ_{FE}) in the linear region was extracted using the transconductance (g_m) maximum method and the *SS* was calculated as a minimum of $dV_g/d\log(I_d)$ in the range of $V_g > V_{on}$. V_g is the gate bias and I_d is the drain current of the device. V_{on} was defined as V_{gs} at $I_d(V_g) = 1$ pA.

3. Result and discussion

3.1. Depth profile analysis after S/D dry etch

It was discovered that a considerable amount of Mo and Cl was observed from the back-channel surface as described in Fig. 1(b). Those components, which were widely distributed on the back-channel surface, decreased gradually toward the inside of the channel, and eventually almost disappeared at a depth of about 10 nm. It is believed that Mo slightly contaminated the active surface when the metal layer was deposited by sputtering method and some etch by-products remain after the etch process. For Cl, which is one of the main etching gases, it is presumed that this component was adsorbed on the channel surface or remained by bonding on the surface during the S/D metal dry etching process.

3.2. Etch damage after S/D dry etch

The microscopic structure analyses were performed for in-depth observation of the post-etch condition. Especially, the condition of the back-channel surface between the S/D patterns right after the dry etching process was very dirty as shown in Fig. 2(a). A by-product of Mo layer which was generated during the S/D metal etching was reported acts as a charge generation layer [20], and it was confirmed that this was indeed the case by finding a small amount of Mo content on the back-channel surface from the results of the EDS analysis as shown in Fig. 2(b). The concentration of Mo was calculated as the ratio of the mainly detected units: oxygen and Si (substrate). The presence of such undesirable metal-etching by-products could deteriorate the performance of the device since an irregular conductive path on the back-

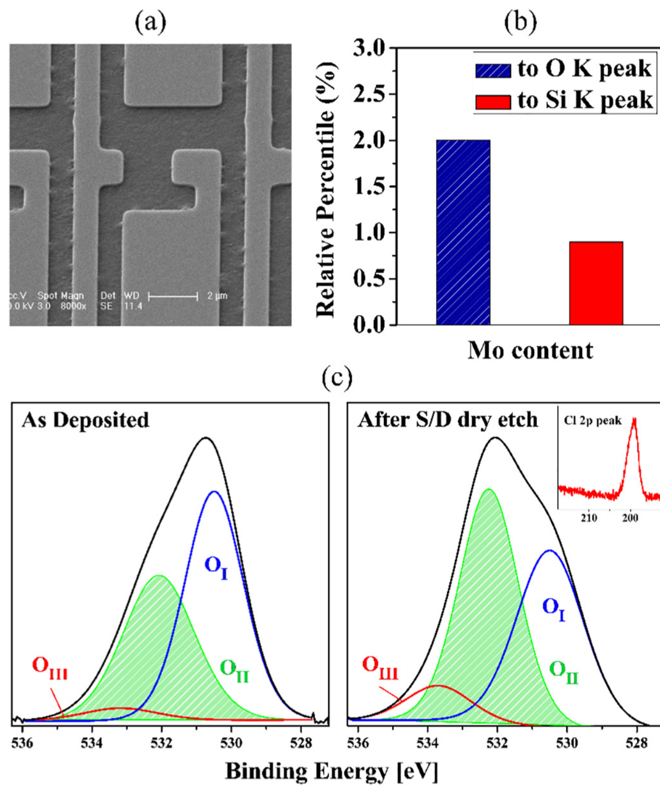

Fig. 2. (a) Microscopic structure right after S/D dry etching. (b) EDS analysis of Mo content on the back-channel surface. (c) XP spectra of the O 1s core level of the channel for the condition of 'as deposited' and 'after S/D dry etching.' The inset Figure is XP spectra of the Cl 2p level.

channel surface weakened the gate control for the device, thereby increasing sub-threshold slope (*SS*) and shifting turn-on voltage (V_{on}) in the negative direction. Shortly, this problem greatly affects the switching characteristics of device.

For further in-depth investigation of the detailed bonding states before and after S/D dry etching process, the O 1 s peaks were carefully deconvoluted into three different peaks of O_I, O_{II}, and O_{III} through XPS measurement as depicted in Fig. 2(c). The lowest binding energy peak (O_I) at 530.5 eV was associated with O^{2-} ions of metal oxides, indicating the oxygen surrounded by In, Sn, and Zn at the channel surface. Since the concentration of the Al component in the channel layer is as low as around 1 atomic percent, the information for the O—Al bonding could not be attained. The middle binding energy peak (O_{II}) of around 532 eV was related to O^{2-} ions, which indicated the oxygen-related defects in the Al-InSnZnO matrix at the channel surface [21,22]. The changes in this component had a great influence on the device performance. Finally, the peak at the highest binding energy of the O 1 s spectrum (O_{III}) around 533 eV was attributed to the impurities in the Al-InSnZnO films such as O—H, O—C, and O—Cl species. After the S/D dry etching process, the metal-oxygen bond (O_I) was severely decreased, while the defect-related bond (O_{II}) was significantly increased more than O_I. This means that a considerable portion of the stable metal-oxide bond was broken, and concentration of oxygen vacancies was increased, thereby an unintentional conductive path could be formed in the back-channel region, which can aggravate the electrical characteristics of oxide TFTs. Furthermore, it was found that the Cl (the main etching gas) contaminated the surface during the S/D dry etching stage and a large amount of Cl components remained after the dry etching process, which is evident from the significant increase in the O_{III} component in the O 1 s peaks. The inset in the Fig. 2(c) indicates a steep peak around 200 eV, and it is a clear evidence that Cl remained on the back-channel surface after the S/D dry etching.

3.3. Damage removal process

To remove the back-channel damage, the device was immersed into the active wet etchant solution for a brief period. Since the wet etching rate of the active wet etchant for channel material was as fast as around 1 nm/s, the damaged back-channel surface was substantially restored after just 10 s of wet treatment process by easily recessing the damaged surface as depicted in Fig. 3.

3.4. Restored channel surface

Fig. 4(a) demonstrates the S/D patterns and etched back-channel surface of the device adopting the wet treatment process. When the wet treatment was applied for only 10 s, the back-channel surface of the device was remarkably enhanced by the process. It can be certainly seen that the surface state of the device was significantly refined. Furthermore, the boundaries of the dirty patterns became very clear and the etched surface was considerably improved. Above all, Mo contents on the back-channel surface was reduced by around 80% compared to the condition not subjected to the wet treatment, as exhibited in Fig. 4(b). Hence, even though the wet treatment process time is as short as only 10 s, the damaged part of the back-channel surface caused by dry etching was almost eliminated and the condition of the device was returned to a normal state. After applying the wet treatment, all of deconvoluted three peaks of O 1 s peak in the XP spectra were almost completely recovered to the state immediately after active material deposition, as shown in Fig. 4(c). The decreased metal-oxygen bonding after S/D dry etching process was increased in addition to the oxygen-related defects being reduced via wet treatment. Above all, the effective removal of Cl had dramatically decreased the O_{III} peak. Considering the comparative analysis, it can be seen that the condition of the back-channel surface after application of wet treatment almost returned right after the channel deposition. The impurities (Mo, Cl) were removed well by the wet treatment, but it was discovered that the oxygen vacancies due to the physical dry etch damage still remained from the O_{II}

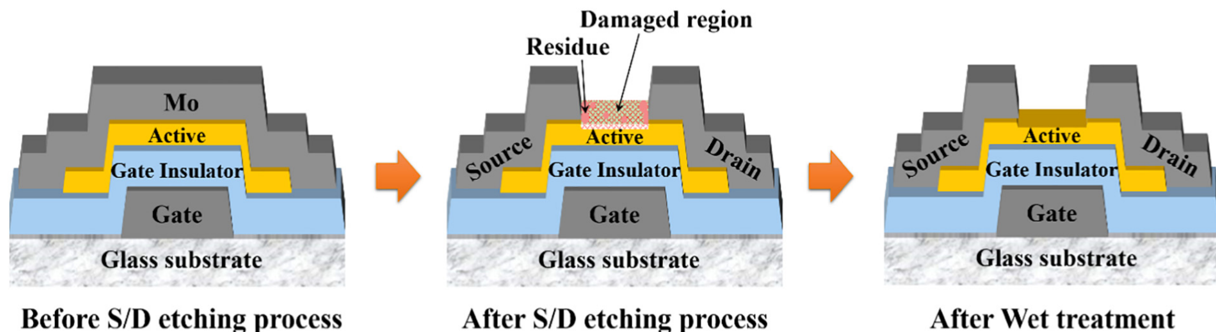

Fig. 3. The procedure of wet treatment process. The damaged region generated during S/D dry etching can be easily recovered by 10-s wet treatment.

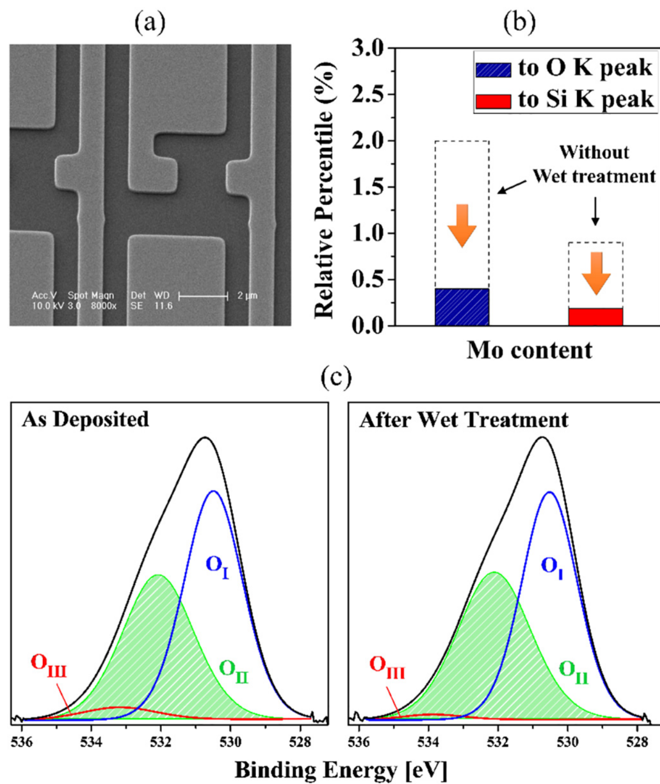

Fig. 4. (a) Microscopic structure adopting wet treatment. (b) EDS analysis of Mo content on the back-channel surface. (c) XP spectra of the O 1s core level of the channel for the condition of 'as deposited' and 'after wet treatment.'

peak. It will be presumed to be improved by thermal annealing after fabrication of the device. The results of the EDS and XPS analyses after the S/D dry etching indicated contamination of the back-channel surface, as was expected from the depth profile. In addition, it can be confirmed that the condition of the back-channel surface was greatly improved, indeed almost recovered, through the very short and simple wet treatment process.

3.5. Device characterization

Fig. 5(a) shows the transfer characteristics of the fabricated TFT without the wet treatment process, which indicated particularly large negative V_{on} and high SS, and also suffered from a large V_{on} difference in the range drain bias (V_D) = 0.1 V to V_D = 10 V. Furthermore, large V_{on} shifts of 0.76 V occurred in the positive direction under positive-bias stress (PBS) stability and 1.17 V in the negative direction under negative-bias stress (NBS) stability, as shown in Fig. 5(b). Notably, it is sure that these demonstrably poor device characteristics were definitely caused by the back-channel etching damage and etching residue during the S/D dry etching process. In contrast, all the device performance were remarkably improved after employing the wet treatment. The device shows a near-zero V_{on} of −0.3 V, a high μ_{FE} of 42.1 cm^2/Vs, a low SS of 0.12 V/decade, and a high on/off ratio of over 10^9, as shown in Fig. 5(c). In particular, V_{on} shifts during reliability test were dramatically improved from 0.76 to 0.17 V in the positive direction for the PBS test and from 1.17 to 0.19 V in the negative direction for the NBS test, as shown in Fig. 5(d). They were controlled under 0.2 V for all conditions. This is due to the effective surface modification through the wet treatment process. The comparisons of the characteristics for the TFTs are summarized in Table 1.

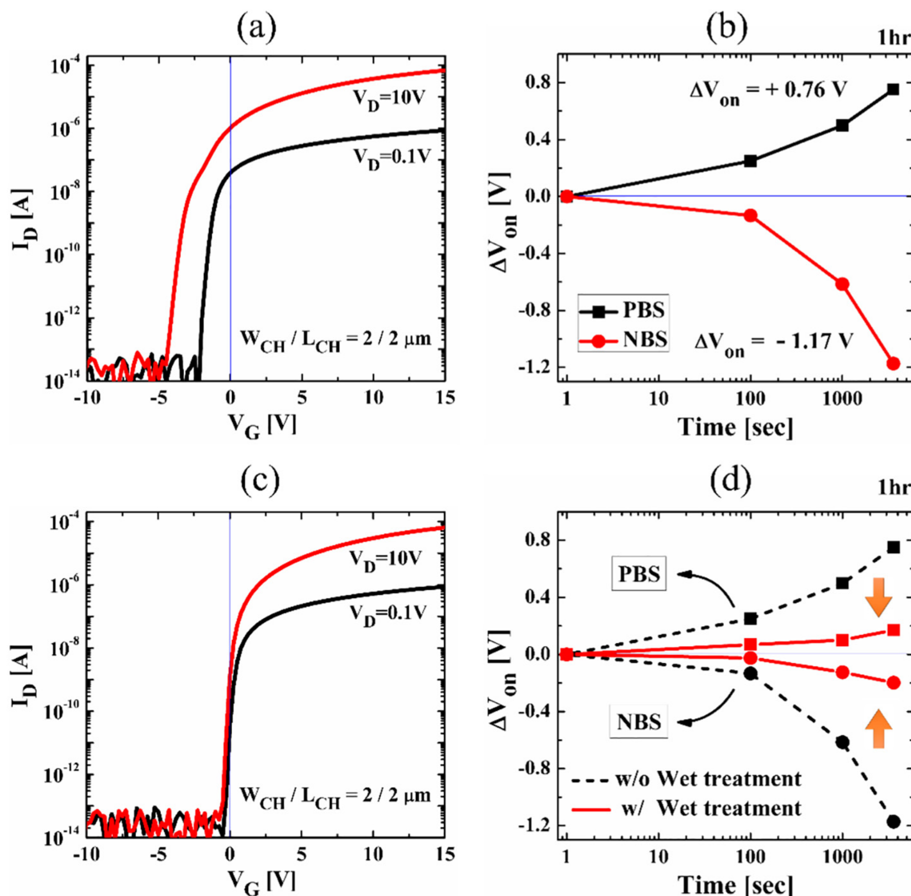

Fig. 5. Electrical characteristics of the fabricated oxide TFTs with 2 μm of channel width (W_{CH}) and channel length (L_{CH}). Transfer characteristics with low (0.1 V) and high (10 V) drain bias for the devices (a) without wet treatment and (c) applying wet treatment for the range of −10 V ≤ gate bias (V_G) ≤ 15 V. Reliability characteristics under PBS and NBS test for 1 h of the devices (b) not subjected to wet treatment and (d) adopting wet treatment. The bias condition for reliability test were V_G = ± 20 V.

Table 1
Device characteristics with and without wet treatment process.

Characteristic	V_{on} [V] (@ V_D = 10 V)	μ_{FE} [cm^2/Vs]	SS [V/decade]	ΔV_{on} @ PBS [V]	ΔV_{on} @ NBS [V]
Without treatment	−4.2	36.5	0.24	+0.76	−1.17
With treatment	−0.3	42.1	0.12	+0.17	−0.19

4. Conclusions

In conclusion, the origin and the phenomenon of back-channel etch damage caused by dry etching which is indispensable for fabrication of short-channel oxide TFT were thoroughly investigated. It was confirmed that metal-oxide bonds were notably reduced and metal-defect bonds were seriously increased after the S/D dry etching. Furthermore, a powerful wet treatment method was introduced to restore the damaged back-channel surface. By doing so, a high-performance 2-μm-length short-channel oxide TFT was fabricated by an active wet-etchant-based treatment process that proved to be a very simple and powerful way to refine the back-channel surface of the transistor. Based on this work, it was concluded that a suitable wet treatment system to restore etch damage has become essential as the need for dry etching process becomes ever greater in the fabrication and implementation of transistors with shorter channel lengths and displays with increasingly narrower pixel pitches. Therefore, this work is likely to be an important contribution to research on very short channel oxide TFT fields for ultra-high resolution display applications requiring very small pixel pitches as a particularly effective treatment characteristics.

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