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Design and Characterization of N-MCT with Low V_{th} Off-FET for High Current-drive Capability

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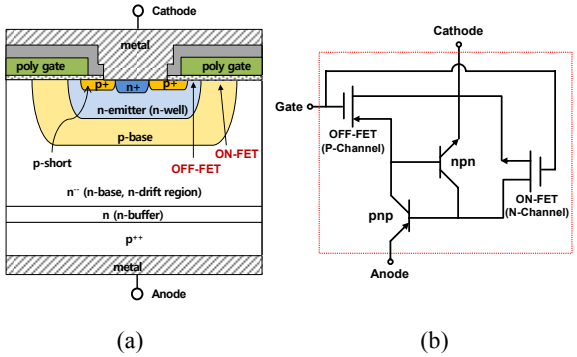
***Abstract*—In this paper, an N-MCT with a low threshold voltage of off-FET has been investigated by simulation and experiment. We have demonstrated the MCT with self-aligned spacer formation and recess process, which results in uniform off-FET channel length. And boron is implanted to adjust the threshold voltage of off-FETs. The threshold voltage of non-doped and proposed MCT was -1.2 V and 0.6 V, respectively. The forward blocking voltage of both MCTs was similar to 1800 V and the turn-on voltage of MCTs was 0.2 V and 0.75 V, respectively. The non-doped and proposed MCTs exhibit the same *di/dt* around 35.7 kA/μs and peak current of 2.69 kA. That is pointed out that this proposed MCT structure is promising because the current driving capability is improved without degradation of on-state characteristics.**

***Index Terms*—N-MCT(MOS controlled thyristor), pulse power, power device, turn-off, V_{th} implantation**

I. INTRODUCTION

Power semiconductor devices including MOSFET, BJT, IGBT, and thyristor are essential components in a wide variety of power electronics applications such as motor drivers, UPS (uninterrupted power supplies), pulse power system, and so on [1, 2]. Among them, MCT (MOS controlled thyristor) has the high current driving capability and low forward voltage drop because of its thyristor-like action. Besides, MCT with highly interdigitated gate structure has high current rise rate (*di/dt*) and high peak current (I_{peak}) characteristics, and it is mainly applied to semiconductor switches in the pulsed power system such as electromagnetic launchers, flash lamps, nuclear fission driver, ozonizer and CES (capacitive energy storage) as power supply [1-3].

Fig. 1 shows a schematic cross-section and its equivalent circuit of an n-MCT of which a lower base is n-base [4, 5]. MCT is basically an NPNP thyristor with two MOSFET's (on-FET and off-FET) built into the gate structure. Thus, it has high input impedance and it can be turned-on and turned-off by driving on-FET and off-FET at different gate voltages. In the MCT, the conducting state is maintained by the regenerative action of the



(a) (b)

Fig. 1. Conceptual illustration of n-MCT (a) Schematic cross-section of a cell unit, (b) equivalent circuit.

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thyristor even when the gate bias is removed, so the turn-off performance determines the current driving capability of the MCT. To improve the turn-off characteristics of the MCT, it is needed to improve the off-FET performance by implementing uniform and a relatively short channel length of a few ㎛ with low threshold voltage (V_{th}) [5]. Uniform off-FET performance over the whole device area is also needed to avoid device failure when the thyristor is turned off [5]. However, a too short length of the off-FET channel degrades the performance of the on-FET because the off-FET channel region simultaneously acts as a source of the on-FET.

Some efforts have been reported to implement uniform and short length of the off-FET channel by using the self-align process with poly-Si gate as a mask [5-7]. However, it is difficult to achieve a low surface concentration of n-well (i.e. doping concentration of the off-FET channel) inside the p-base region, so a large negative gate voltage below -5 V is applied to turn off the device.

In this paper, an 1400V/5A-rated MCT has been studied for application to the pulsed power systems. The uniform and short length of off-FET channel with low threshold voltage were obtained by self-aligned process using spacer formation and recess process. Electrical characteristics including turn-on and turn-off behavior of the MCT were analyzed by simulation. And the simulation results have been validated by experimental results. Pulse power characteristics such as I_{peak} and *di/dt* were also evaluated using a capacitive discharge test system. From the simulation analysis and experimental results, the proposed MCT has off-FET with small or even positive threshold voltage and has a high turn-off current-drive capability.

II. DEVICE DESIGN AND SIMULATION RESULTS

1. Proposed Off-FET Channel Design

The channel of off-FET is designed by self-aligned process using spacer formation and recess process as shown in Fig. 2. To define the off-FET channel region, we formed spacers on both sides of thermal oxide. The channel length of off-FET is determined by the thickness of the spacer and lateral diffusion of n-well. And then, to obtain a low threshold voltage of off-FET, the oxide was removed by the recess process using wet etching, and the exposed region was count-doped with boron to control the threshold voltage.

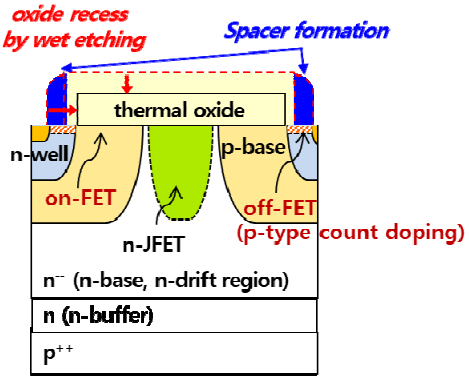
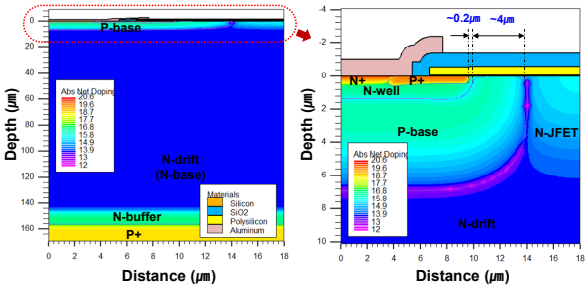


Fig. 2. Cross-sectional view of MCT structure using self-aligned spacer formation and oxide recess process.



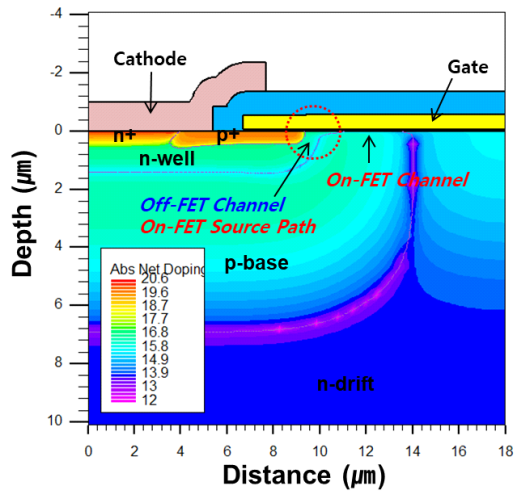
(a) (b)

Fig. 3. The illustrations of (a) conventional n-MCT cell structure in the simulation, (b) 2D doping profile.

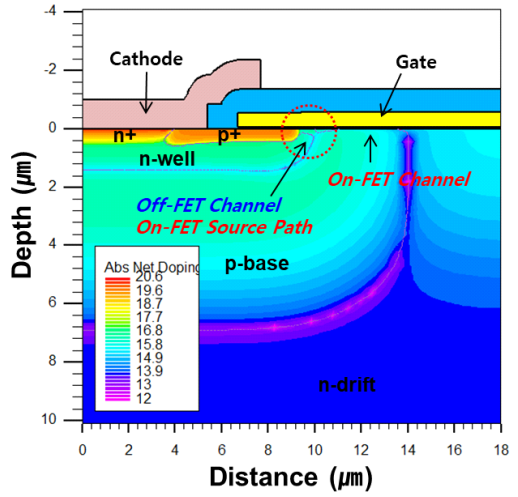
2. TCAD Simulation Results

Two-dimensional numerical simulations have been carried out with SILVACO program to validate our self-align process using spacer formation and recess process, and to analyze the turn-on and turn-off characteristics with various boron implantation dose after spacer recess.

Fig. 3 shows a cross-section of conventional MCT cell structure for simulation. The conventional MCT structure is consists of the vertical four layers designated by the n-emitter/p-base/n-base/p++ without self-align process using the spacer. The turn off function is performed when the gate polarity activates the short FET channel between the p^+ (p-short) and the p-base. For the optimization of the MCT structure, 'p-base and n-well' have an optimal value to avoid break down by the reach through and the surface doping concentration of p-base and n-well determines the threshold voltages of on-FET



(a)



(b)

Fig. 4. Cross-sectional illustration of simulated MCT cell structure (a) without V_{th} implantation, (b) with V_{th} implantation.

and off-FET, respectively.

Fig. 3(b) shows the doping profile of conventional MCT at the surface regime. Above the staked epi layer of p^{++}-sub/n-buffer/n-drift, boron was implanted and annealed at 1150 ℃ for 300 min. Then, phosphorus was formed at 1150 ℃ for 300 min. The depth of p-base and n-well are ~7 ㎛ and ~1.5 ㎛, respectively. The off-FET has a channel length of ~0.2 ㎛ and on-FET has a channel length of ~4 ㎛. The channel length of 0.2 ㎛ for off-FET is too short. This short channel length causes poor gate controllability and increases source resistance of on-FET which degrades the on current characteristics.

Fig. 4 shows the cross-sectional view of proposed

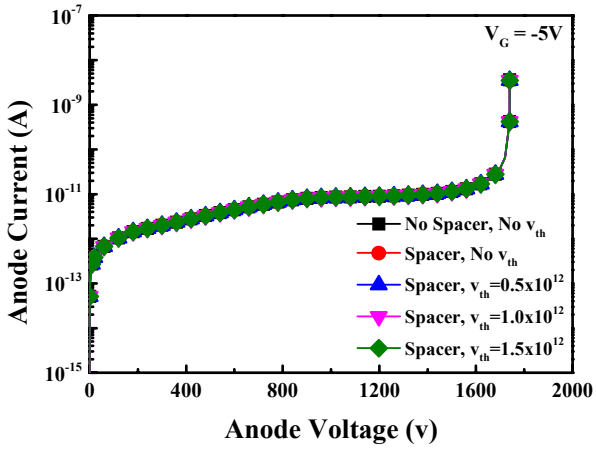


Fig. 5. Simulated forward blocking characteristics at the gate voltage of -5 V.

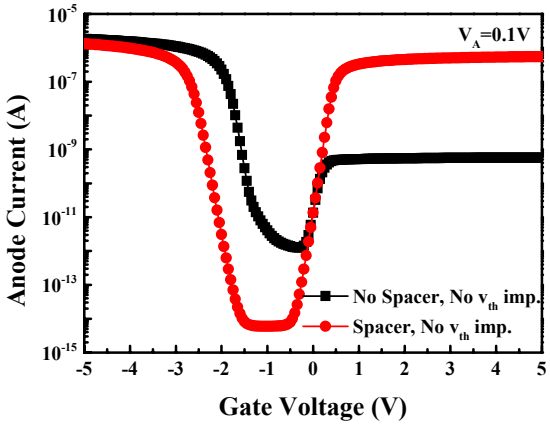


Fig. 6. Simulated I-V characteristics of on/off-FETs with or without the spacer.

MCT structures with self-aligned spacer formation and recess process. The ~1 ㎛ of the off-FETs channel region is formed by the proposed structure. Fig. 4(a) shows the device without boron implantation at the off-FET channel region. And boron is implanted to reduce V_{th} of the off-FET and either to make depletion-mode pMOS channel at the off-FET channel region as shown in Fig. 4(b). A pMOS with low threshold voltage is easy to turn off an MCT and improves the current-drive capability of the MCT.

The simulation results of breakdown characteristics with different structures and V_{th} doping concentrations are shown in Fig. 5. The off-FET channel doping concentration varies from 0.5×10^{12} cm^{-2} to 1.5×10^{12} cm^{-2}. The forward blocking voltage of MCTs is the same as 1750 V regardless of the conditions. Thus, the formation of an off-FET channel with self-aligned spacer process

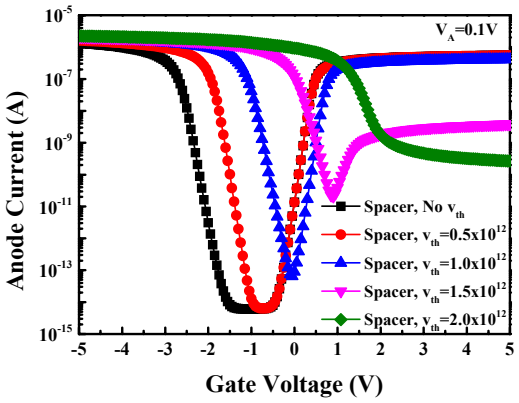


Fig. 7. Simulated I-V characteristics of on/off-FETs with varying boron doping concentration.

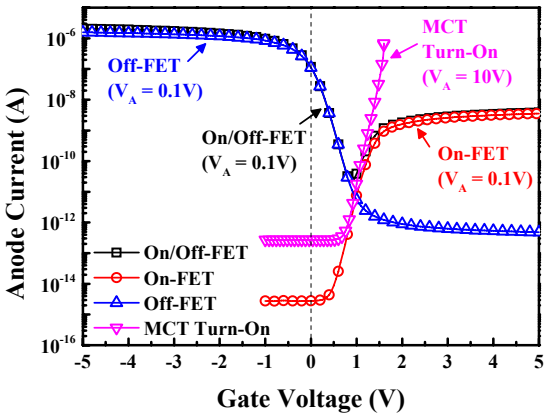


Fig. 8. Simulated I-V characteristics of on/off-FETs at V_A= 0.1 V and turn-on characteristics of MCT at V_A=10 V.

and counter doping to decrease the threshold voltage of off-FETs do not degrade the forward blocking capability of MCTs.

Fig. 6 shows the transfer characteristics of on-FET and off-FET with gate voltage at the structure of Fig. 3(b) and 4(a). To analyze the on-off characteristics of MCT, p-base and n-drift are selected simultaneously as an anode electrode. A small anode voltage of 0.1 V is applied to simulate the characteristics of on-FET and off-FET and to prevent operating as an MCT. As mentioned earlier, the off-FET without spacer has a shorter channel length than with spacer. The threshold voltage of off-FETs with a spacer is larger than that of without spacer due to the longer channel length and higher n-type doping concentration at the off-FET channel region. However, the on-FET current is significantly improved because the current path at the source of on-FET is achieved.

The threshold voltage of off-FET can be modulated with V_{th} doping on the channel region. To decrease the V_{th} of off-FET, we change the doping profile of the off-FET channel region by counter doping with boron implantation. The simulated I-V characteristics of on/off-FETs with different doping concentrations are shown in Fig. 7. With increasing V_{th} doping concentration, the threshold voltage of the off-FET is reduced due to the lower net doping concentration of n-well by counter doping effect. Almost 0 V of the off-FET threshold voltage can be achieved at V_{th} implantation dose of 1.0×10^{12} cm^{-2}.

A depletion-mode pMOS is formed when the dose of V_{th} implantation is 1.5×10^{12} cm^{-2}, and this causes the off-FET to have a positive threshold voltage. These results allow a 0 V turn-off MCT which simplifies a gate-drive circuit and acquires high current-drive capability. However, the on current characteristics are degraded because the surface of n-well is converted to the p-type by the boron counter-doping and a barrier for current flow is formed between the source (n-well) and the channel of the on-FET.

To verify the MCT operation when the V_{th} implantation is 1.5×10^{12} cm^{-2}, we simulated turn-on characteristics of MCT and compared it with on/off-FETs characteristics (Fig. 8). The simulated structure for analyzing on and off-FET is shown in Fig. 4(b). The n-drift region is defined as an anode to analyze the I-V characteristics of on-FET, and the p-base region is set to the anode for off-FET operation. Finally, the n-drift and p-base regions are selected simultaneously to enable both on/off-FETs. Each curve matches well with the combined curve. To verify turn-on characteristics of the MCT with low on-FET current, the anode voltage of 10 V is applied. As shown in figure, the on-FET current drives the thyristor and the MCT turns on normally. From the results, we can expect that the MCT with depletion-mode off-FET (pMOS) does not cause the problem on turn-on performance of the MCT, since the anode voltage of MCT is usually much higher than 10 V under operating condition. And it can be turned off at the gate voltage of 0 V, which is normally-off device.

III. Fabrication Process

Process flow and conditions for fabricating the MCTs

by self-align process using spacer formation and recess process are summarized in Fig. 9. 6-inch Si wafer consisting of p^{++}-substrate/n-buffer/n-drift layer was used as a starting material. The doping concentration and thickness of the n-drift layer determine the maximum allowable breakdown voltage of the MCT, and the concentration of 6×10^{13} cm^{-3} and the thickness of 150 ㎛ were chosen to ensure sufficient breakdown voltage for 1400 V-rated MCTs. Firstly, ion implantation of phosphorus on the n-JFET region is conducted to reduce on-FET resistance after align-key patterning. Then the ion implantation of boron and first drive-in process are carried out to form the p-base region, and ion implantation of phosphorus and second drive-in is carried out to form an n-well region inside the p-base region (Fig. 9(a)). In this step, the p-base region extends a significant distance in the lateral direction, but the n-well region only slightly extends in the lateral direction because of the previously formed p-type dopants. The surface between the end of the p-base and the end of the n-well becomes the channel of the on-FET. To define the off-FET channel region, we formed 0.4 ㎛-thick spacers on the side of thermal-oxide by LPCVD (low-pressure chemical vapor deposition) and etch-back process. And then, a high dose of boron was implanted to form p-short (p^{+}) after photolithography process (Fig. 9(b)). The channel length of the off-FET is determined by the thickness of the spacer and lateral expansion of n-well under the thermal-oxide. In this status, the net doping concentration at the end of n-well is relatively high resulting in a large negative threshold voltage of the off-FET. To obtain a low threshold voltage of the off-FET, the channel region of the off-FET was exposed by the recess process using wet etching of oxide. The spacers deposited by LPCVD have faster etch-rate than the thermal-oxide and the off-FET channel region can be easily exposed by wet etching in HF aqueous solution. And then the off-FET channel region was count-doped by boron implantation with the dose of 1.3×10^{12} cm^{-2} (Fig. 9(c)). The process described above that defines the off-FET channel is self-aligned to the thermal-oxide and enables uniform and short channels with small negative (or even positive) threshold voltage. An MCT without boron implantation was also fabricated as a control device. After removing the spacer and thermal-oxide, the general processes for gate dielectric, poly-Si gate, n^{+}

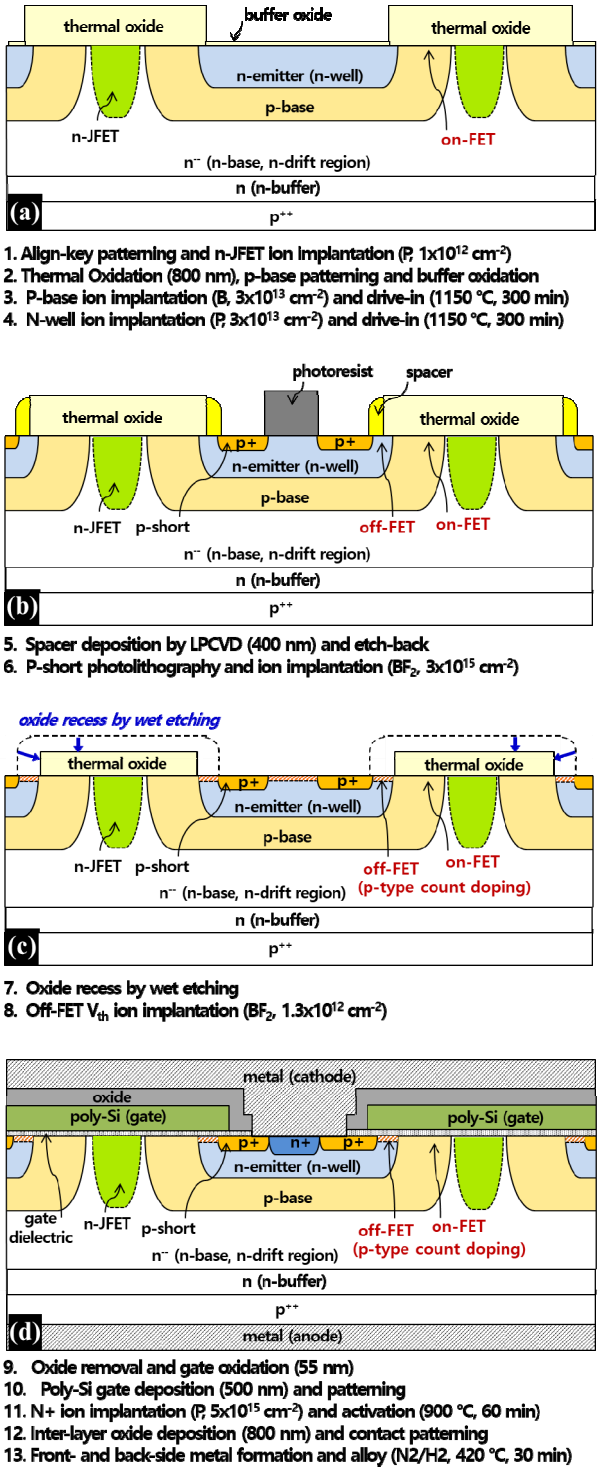
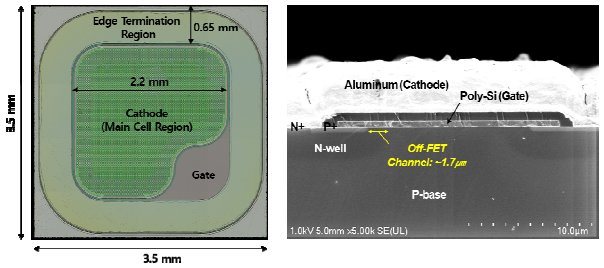


Fig. 9. Schematic cross-section of process flow and conditions for fabricating the MCTs by self-align process using spacer formation and recess process.

formation, an interlayer dielectric (oxide), and the formation of metal electrodes were performed to complete the fabrication of MCTs (Fig. 9(d)).

Fig. 10(a) shows a microscope image of the fabricated



(a) (b)

Fig. 10. The features of MCT (a) Optical microscope image, (b) cross-sectional scanning electron microscopy image of unit cell.

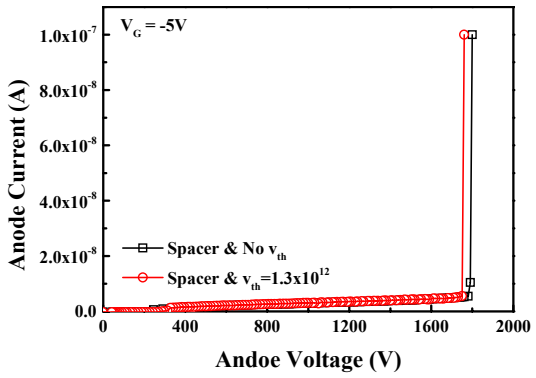
MCT with a size of 3.5 ㎜ × 3.5 ㎜. The area of a central main cell is about 2.2 ㎜ × 2.2 ㎜ including the gate pad region. The periphery of 0.65 ㎜ surrounding the main cell is edge termination region for blocking high voltage of the MCT, and twenty floating guardrings were implemented during the p-base process. Fig. 10(b) shows a cross-sectional SEM image of the main cell of the MCT, and p-base junction is not observed due to the low doping concentration, however, n-well junction with the depth of 3 ㎛ and the off-FET channel length of about 1.7 ㎛ are observed.

IV. Experimental Results

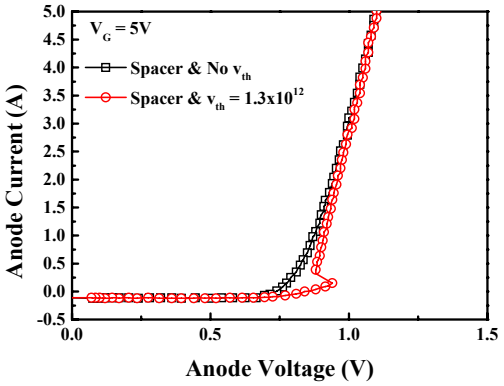
The measurements were done at the wafer level and the package level. The wafer level characteristics of MCT were analyzed by HP4156A semiconductor parameter analyzer. After each die is mounted on a TO247 package, the package level characteristics of MCT were studied by Tektronics 370A curve tracer.

Fig. 11(a) shows the comparison of the forward blocking characteristics of MCTs at the gate voltage of -5 V on both wafer and package level. The MCT without V_{th} implantation device shows a forward breakdown voltage of 1800 V and the proposed MCT device shows a breakdown voltage of 1750 V. The breakdown voltage difference between V_{th} implanted and non-implanted devices is not considerable. The forward blocking voltage strongly depends on the edge termination structure such as the number of guardrings, a width of rings, and space between rings not the doping density on the channel area.

The forward I-V characteristics of MCTs at the gate



(a)



(b)

Fig. 11. (a) Comparison of the forward blocking characteristics of MCT devices at the gate voltage of -5 V, (b) The forward conduction characteristics of MCTs at the gate voltage of 5 V.

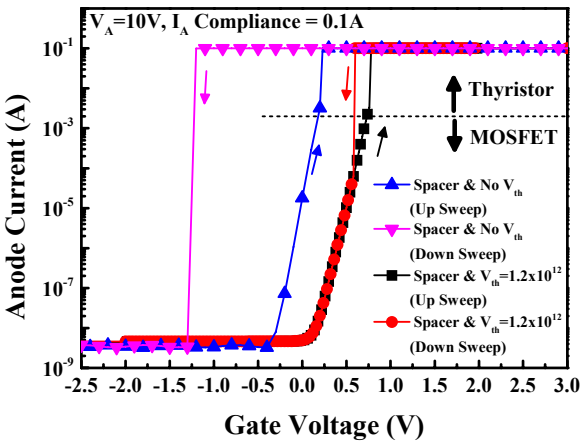


Fig. 12. On-off characteristics of the MCTs with or without V_{th} implantation.

bias of 5 V on package level are plotted in Fig. 11(b), as shown, the MCTs with and without V_{th} implantation exhibit an almost similar on-state curve except a small snapback region. It seems that the snapback occurs due to the barrier located on the source region of the on-FET by the counter doping as shown in Fig. 4(b). The on-state

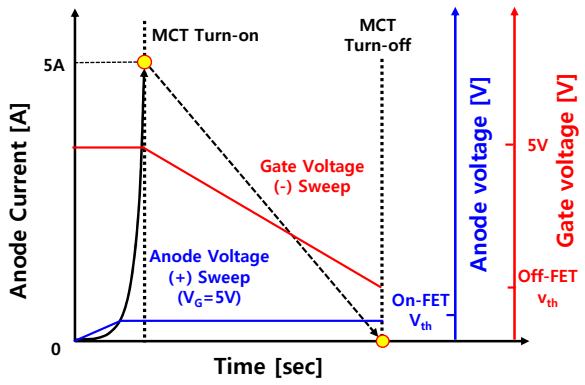


Fig. 13. Conceptual illustration for turn-off test of MCTs.

voltage drop of both devices is the same as ~1.1 V at anode current of 5 A.

Fig. 12 shows evaluation results of the MCT's on-off characteristics on the wafer level. The anode is biased for 10V while the gate is swept from -5 V to 5 V and vise versa. Without V_{th} implantation, MCT turns on ate the gate bias of 0.2 V(over ~3 mA of anode current) by the regenerative action as mentioned earlier. Whereas MCT with V_{th} implantation turns on at 0.75 V. The MCTs maintain on-state even the gate bias decreases below the V_{th} of on-FET once they have turned on and turns off at the gate bias under the V_{th} of off-FETs. The off characteristics of MCTs strongly depend on V_{th} implantation as shown in figures. The MCT without V_{th} implantation turns off at -1.2 V but with V_{th} implantation turns off at 0.6 V because the implanted boron into the channel region of off-FET shifts the V_{th} to a positive direction. The maximum controllable current of MCTs is determined by turn-off characteristics. Thus, the V_{th} adjustment on the channel region of off-FET lowers threshold voltage of off-FETs, enhances the performance of the off-FET, and improves the current-drive capability of MCT devices without degradation on the forward conduction characteristics.

Meanwhile, the characterization of turn-off properties on the wafer level with applying high current can lead to a thermal run away. To analyze turn-off performance at high current level of 5 A, the anode and gate voltage waveform across the TO-247-packaged MCT are applied as shown in Fig. 13. The anode voltage is swept until the MCT turn-on (at 5 A of anode current) at the gate voltage of 5 V. After the MCT turned on, the gate voltage decreases from 5 V to off-FET V_{th} voltage. If the gate

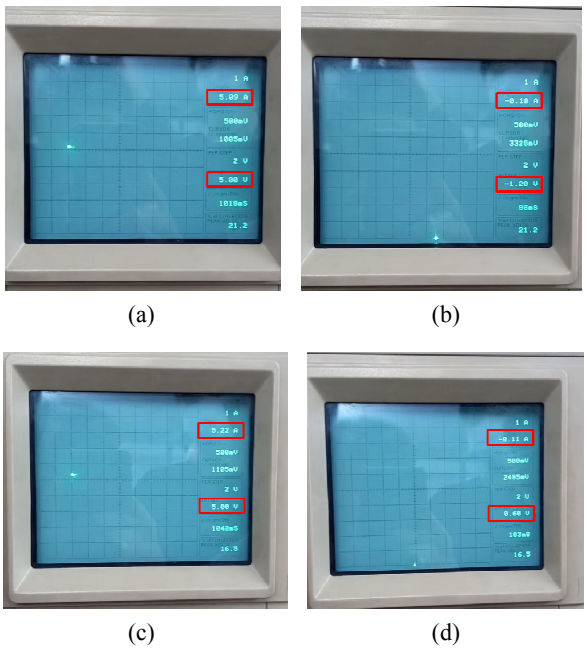
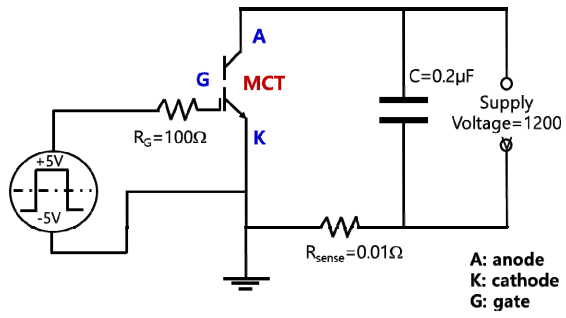


Fig. 14. Measured turn-on and -off characteristics of MCTs with varying a gate bias (a) on-state without V_{th} implantation, (b) off-state without V_{th} implantation, (c) on-state with V_{th} implantation, (d) off-state with V_{th} implantation.

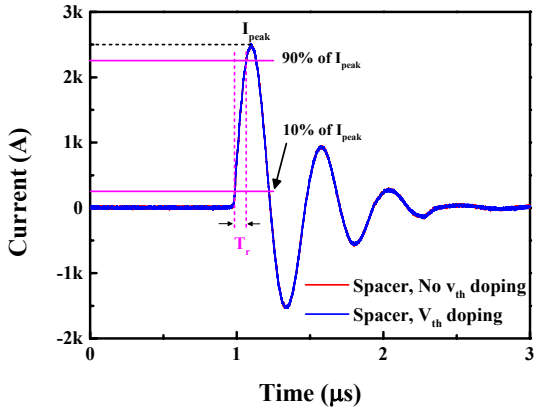
voltage goes down below the threshold voltage, the off-FET turns on and the regenerative action stops and this leads to the MCT turn off.

Fig. 14 shows the measurement result on packaged MCT using the test method described as Fig. 13. Fig. 14(a) and (b) show the measured turn-off characteristics of non-implanted MCTs. The MCT is on-state with 5 A of on current in Fig. 14(a). To turn off the MCT, the gate voltage has decreased from 5 V to -1.2 V as shown in Fig. 14(b). In the same way, the V_{th} implanted MCT turn on with 5A of anode current and turns off at gate voltage of 0.6 V as shown in Fig. 14(c) and (d), respectively. This matches the results as shown in Fig. 11 which means The MCT with spacer and counter doped off-FET channel shows better turn-off characteristics.

On the other hand, the peak anode current (I_{peak}) and *di/dt* characteristics are the key parameters of turn-on characteristics of MCT. Test circuit configuration for turn-on characteristics of packaged MCT devices is shown in Fig. 15(a). The circuit consists of a charging capacitor, gate resistor R_G, and a load for sensing current R_{sense}. The capacitor is charged with 1200 V by an external power supply and switching pulse with an amplitude of -5 V to 5 V is applied at the gate of MCT.



(a)



(b)

Fig. 15. (a) Circuit configuration of turn-on switching time measurement, (b) measured pulse waveform with or without V_{th} implantation.

The change in anode current is evaluated by reading the current value flowing in the current sensing resistor (R_{sense}). Fig. 15(b) shows the measured pulse waveform on the MCTs which has an active area of 4.84 ㎟ including the gate pad region. As shown in the figure, the MCTs with and without V_{th} doping perform the same *di/dt* around 35.7 kA/㎲, and I_{peak} near 2.69 kA (*di/dt* is measured from 10% to 50% I_{peak}). The rising time of MCTs is around 77 ns (measured from 10% of peak anode current to 90% of peak anode current). The *di/dt* characteristics are the most important factor for thyristor-based devices for pulse power applications. Thus, the V_{th} doping using self-align spacer formation and oxide recess does not disturb the turn-on switching characteristics. In addition, the *di/dt* performs over 35.79 kA/㎲ in both MCTs with little variation but this performance difference due to the mismatches on the packaging and wire bonding which is negligible.

V. CONCLUSIONS

An 1400V/5A-rated MCT was implemented with low V_{th} off-FET for pulsed power application. The uniform and short channel of off-FET with low threshold voltage were fabricated by self-aligned spacer and recess process. To obtain short and uniform channel length, the off-FET channel was defined by the spacer and recessed oxide. By implanting boron into the off-FET channel region, a low threshold voltage was achieved. The threshold voltage of off-FETs in non-doped and proposed MCT were -1.2 V and 0.6 V, respectively. Which results in improved current driving capability. While it is shown similar on-characteristics. The forward blocking voltage of both MCTs was similar to 1800V. The turn-on voltage of undoped and doped MCT was 0.2 V and 0.75 V, respectively. And both MCTs represent the same *di/dt* around 35.7 kA/㎲ and I_{peak} of 2.69 kA. Even though the proposed MCT showed a small snap-back effect, the forward voltage drops and turn-on switching speed, which are the most important factors for pulse power application, were similar between non-doped and proposed structure.

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