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Switching and Heat-dissipation Performance Analysis of an LTCC-based Leadless Surface Mount Package

Dong-Yun Jung[1,*], Hyun-Gyu Jang[1], Jong-Il Won[1], Doo-Hyung Cho[1], Sung-Kyu Kwon[1], Seong-Hyun Lee[1], Kun-Sik Park[1], Jong-Won Lim[1], and Yong-Ha Lee[2]

Abstract—**A leadless surface mount package was developed to enhance the switching and heat-dissipation properties of a power semiconductor. The package was implemented through a low-temperature co-fired ceramic (LTCC)-based multilayer circuit substrate that could form embedded cavities. A silicon carbide (SiC) Schottky barrier diode (SBD) bare die was attached to the cavity in the LTCC substrate. Chip interconnection was realized using a wide and thick copper (Cu) clip with a low parasitic inductance and electrical resistance compared to those of a conventional wire. Silver-filled multiple vias and wide metal planes were used to reduce the electrical parasitic effects and enhance the heat-dissipation of the package. The DC and dynamic characteristics of the 600 V/10 A-class SiC SBD package involving the proposed technologies were evaluated. The dynamic test results indicated that the reverse recovery charge (Q_{rr}) was 18.7% lower than that of a traditional TO-220 packaged product with the same bare die. Furthermore, two leadless commercial products and the proposed package prototype were applied to a power factor correction (PFC) converter, and the power loss and heat-dissipation performances were compared. The proposed package exhibited a lower loss and higher heat dissipation than those of the commercial products.**

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[1]DMC Convergence Research Department, Electronics and Telecommunications Research Institute (ETRI), 218 Gajeong-ro, Yuseong-gu, Daejeon 34129, Korea
[2]Y.TECH, 218 Gajeong-ro, Yuseong-gu, Daejeon 34129, Korea
E-mail : dyjung14@etri.re.kr

Index Terms—**Low-temperature co-fired ceramic, leadless surface mount package, switching, heat-dissipation, power factor correction converter**

I. INTRODUCTION

The power loss of a switching power converter primarily involves two components: switching semiconductors and passive components. The losses due to switching semiconductors correspond to switching losses and those related to the on-resistance. The parasitic inductance in semiconductor packaging affects the switching loss of semiconductors. Notably, the parasitic inductance is of significance in high-frequency operating systems as it can cause undesired high-frequency oscillations corresponding to the parasitic capacitance [1, 2]. Furthermore, the parasitic inductance can generate switching over-voltage in a system and, thus, this parameter influences the switching power loss and lifetime or reliability of the device [3, 4].

In the effort to improve switching characteristics, various studies have been conducted to reduce parasitic inductance. They include studies on the location of semiconductor bare dies and the metal layout of the substrates inside a semiconductor package [5-7] and studies on chip interconnection technologies through wide metal contacts such as flex foil, lead frame, and copper clip [3, 8, 9].

In addition, the heat-dissipation performance is a critical indicator in a semiconductor package because it considerably influences the overall heat-sink design and system fabrication [10, 11]. To solve heat dissipation issues in the field of power semiconductor packaging

applications, various studies have been performed. They include studies on bonding materials and structures [12, 13], on ceramic substrate materials such as aluminum nitride (AlN) and silicon nitride (Si_3N_4) [7, 8, 13], on substrate manufacturing and processing [8], on the base plate materials [7], and on the chip interconnection technologies (including the double-side cooling method) [3, 9, 14, 15].

We previously proposed a leadless silicon carbide (SiC) Schottky barrier diode (SBD) discrete surface-mount package to enhance the switching and heat-dissipation performance of the SBD [16]. In this paper, we discuss the implementation of the package using low-temperature co-fired ceramic (LTCC) multilayer substrates and the evaluation conducted of its DC and dynamic characteristics. Moreover, the performances of the proposed package compared to those of conventional commercial products, evaluated using a power factor correction (PFC) converter, are also elucidated.

II. Proposed Package

Fig. 1(a) shows the basic structure of the proposed leadless surface mount package. The package includes an LTCC-based multilayer circuit structure that exhibits a higher thermal conductivity compared to that of conventional epoxy molded packages and can form embedded cavities.

To reduce the parasitic inductance caused by bond wires, two approaches were adopted. First, the device was embedded in the cavity of the LTCC substrates to minimize the interconnection length [4, 16, 17]. The inductance of the bond wires was minimized by adjusting the top side of the device and height of the substrate equally. Second, a flat copper (Cu) clip was used to realize the chip interconnection [16]. Unlike aluminum (Al) wire [4, 17], the use of a wide and thick Cu clip helps to reduce the parasitic inductance and electrical resistance.

In previous work [4], the multiple vias, which serve as electrical and thermal paths, were vertically stacked within the structure, as shown in Fig. 1(b). Consequently, the outside of the package was irregularly formed owing to the stacking being based on filling metals. To rectify this embossing issue on the outside of the package, the stacking pattern of the embedded vias was changed to a zigzag pattern, as shown in Fig. 1(c).

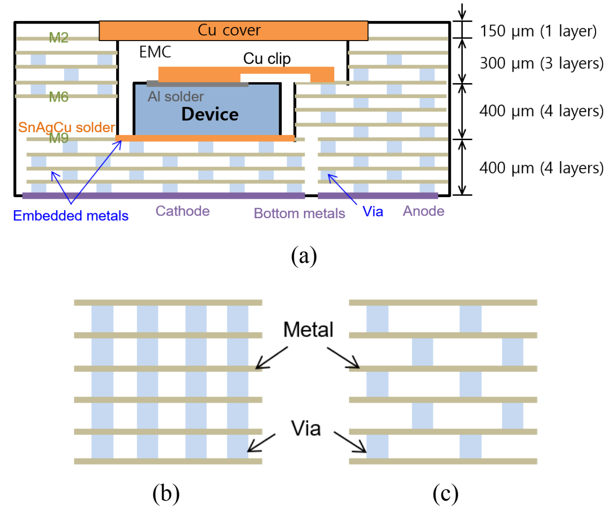


Fig. 1. (a) Basic structure of the proposed multilayer LTCC-based leadless surface mount package (not drawn to scale), (b) previous vertically stacked vias, (c) proposed zigzag via stacking pattern.

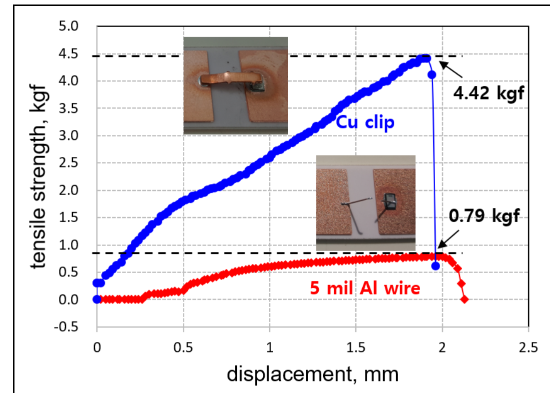


Fig. 2. Bond pull test results of frameworks with Cu clip and Al wire.

Fig. 2 shows the bond pull test results of the framework involving the Cu clip and Al wire interconnecting two Cu metal planes on an aluminum nitride (AlN) substrate. Although an Al solder paste was used to interconnect the Cu clip on the top metal of the device, the Al solder is not described herein. The Al wire was 5 mil thick, the same as that used in the proposed package. In the case of the Cu clip and Al wire, detachment occurred when they were pulled at tensile strengths of 4.42 kgf and 0.79 kgf, respectively. These results indicate that the Cu clip soldering has a higher tensile strength than that of the Al wire bonding. In addition, because a Cu clip is wider and thicker than an Al wire, it has a lower electrical resistance, lower

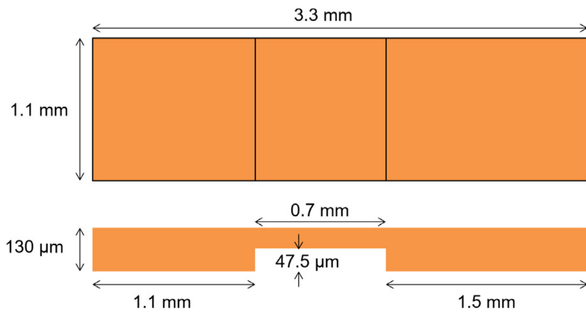


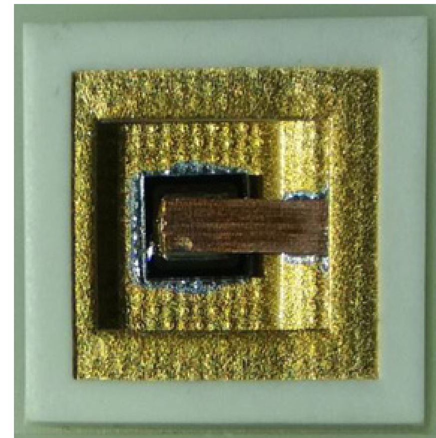
Fig. 3. Top view and cross-sectional view of the proposed Cu clip.

parasitic inductance, and superior heat transfer characteristics.

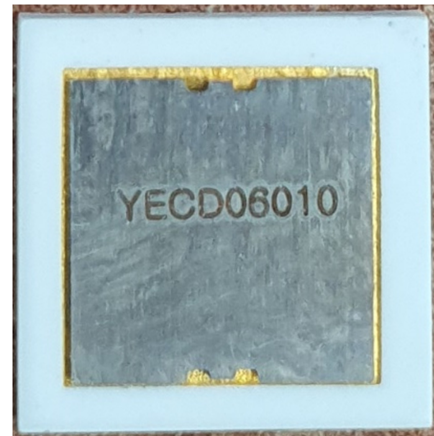
To verify the proposed methodologies, as shown in Fig. 1, we implemented an LTCC-based leadless surface mount device (SMD) package using a 600 V/10 A-class SiC SBD bare die manufactured by Global Power Technology Co., Ltd. [18]. The Cu clip was designed considering the anode window of the SiC SBD bare die and the gap between the bare die and anode metal patterns on the LTCC substrate. The width and thickness of the Cu clip were 1.1 mm and 130 μm, respectively. The pattern was etched to have a thickness of 47.5 μm to prevent the occurrence of any discharge between the clip and edge termination on the device, as shown in Fig. 3.

Fig. 4 shows images of the internal and external sides of the top and bottom surfaces of the fabricated leadless LTCC-based SiC SBD surface mount package [16]. The SiC SBD bare die was attached to the cathode metal region and interconnected to the anode metal pattern through the Cu clip in the cavity of the multilayer ceramic substrate. The cavity of the LTCC was filled with a liquid epoxy molding compound (EMC), and the Cu cover was soldered to the second metal (M2) on the LTCC. To prevent the current path from being exposed to the external environment, no metal was placed on the top of the LTCC. The package had dimensions of 8 mm × 8 mm, and the bottom plane of the package was exposed only to the terminals to connect the anode and cathode. The anode and cathode in the LTCC multilayers consisted of embedded silver metal planes and silver-filled vias.

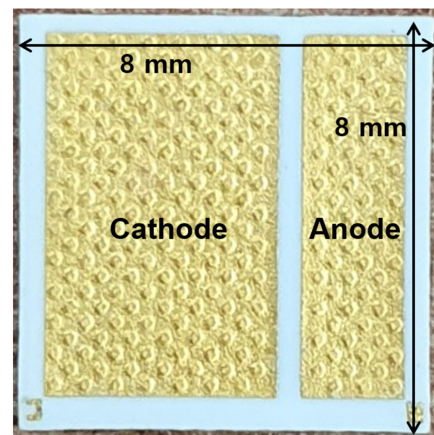
Fig. 5 shows the measured DC characteristics of the proposed discrete package shown in Fig. 4. The characteristics were measured using the IWATSU CS-5200 curve tracer. The forward current was 10.5 A at a forward voltage of 1.5 V, and the reverse leakage current was 4.16 μA at a reverse voltage of 600 V.



(a)



(b)



(c)

Fig. 4. Photographs of the (a) internal top, (b) external top, (c) bottom surfaces of the fabricated package prototype [16].

Fig. 6 shows the reverse recovery waveforms

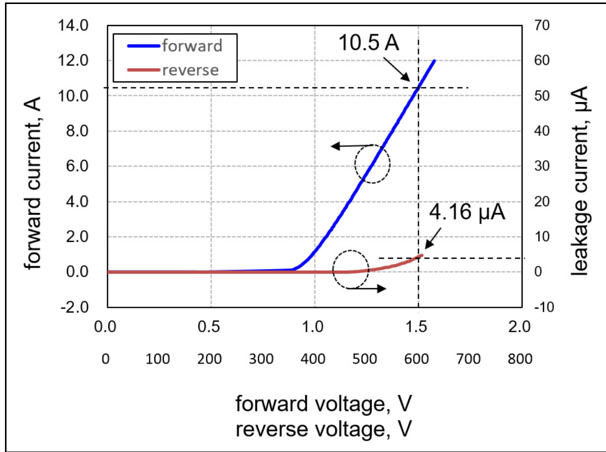


Fig. 5. Measured DC characteristics.

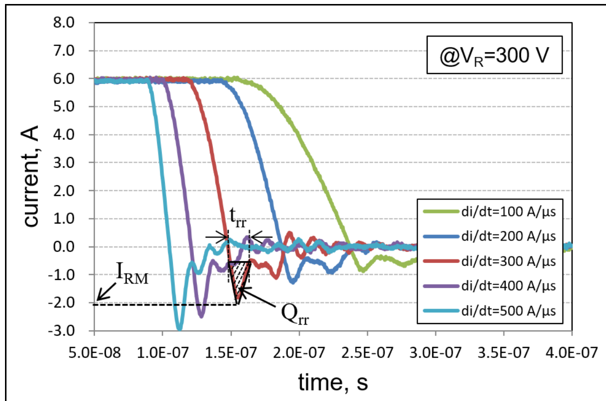


Fig. 6. Measured reverse recovery waveforms as a function of *di/dt* from 100 A/μs to 500 A/μs at a reverse voltage of 300 V [16].

Table 1. Measured switching performance as a function of *di/dt* from 100 A/μs to 500 A/μs at a reverse voltage of 300 V [16]

di/dt [A/μs]	I_{RM} [A]	T_{rr} [ns]	Q_{rr} [nC]
100	0.86	26.8	11.52
200	1.30	21.8	14.17
300	1.82	19.8	18.02
400	2.50	17.3	21.63
500	2.96	15.9	23.53

measured as a function of *di/dt* from 100 A/μs to 500 A/μs at a reverse voltage of 300 V, which is half of the rated voltage. The maximum reverse current (I_{RM}), reverse recovery time (T_{rr}), and reverse recovery charge (Q_{rr}) were 1.82 A, 19.8 ns, and 18.02 nC, respectively, at a reverse voltage of 300 V and *di/dt* of 300 A/μs. Table 1 summarizes the measured switching performance of the proposed package prototype under these conditions [16].

Fig. 7 shows the measured reverse recovery

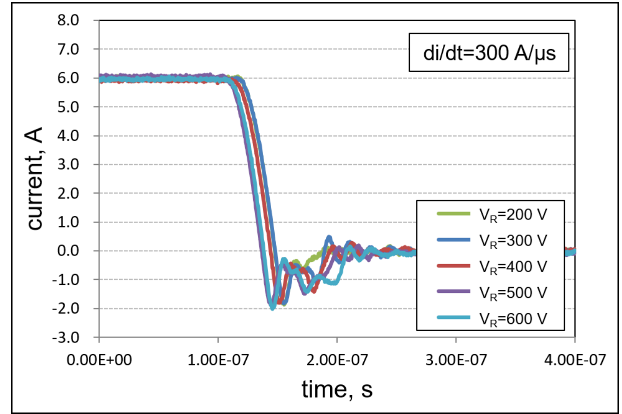


Fig. 7. Measured reverse recovery waveforms as a function of the reverse voltage from 200 V to 600 V at *di/dt* of 300 A/μs.

Table 2. Measured switching performance as a function of the reverse voltage from 200 V to 600 V at *di/dt* of 300 A/μs

V_R [V]	I_{RM} [A]	T_{rr} [ns]	Q_{rr} [nC]
200	1.82	19.9	18.11
300	1.82	19.8	18.02
400	1.80	19.9	17.91
500	1.86	19.5	18.14
600	1.95	18.7	18.23

waveforms as a function of the reverse voltage from 200 V to 600 V at a *di/dt* value of 300 A/μs. Table 2 summarizes the measured switching performance of the proposed package prototype under these conditions.

Table 3 compares the performance of the packaged 600 V/10 A-class SiC SBD devices using the same bare die [16]. The parasitic inductance of a 15-mil-thick Al wire with a length of approximately 7.1 mm, which is used in conventional TO-220 typed products, has been reported to be approximately 5.07 nH [19]. Moreover, in previous work [4], the parasitic inductance of three 5-mil-thick Al wires with a length of approximately 4.5 mm, which were used in the cavities of LTCC multilayers, was calculated to be approximately 2.55 nH [19]. In this work, the parasitic inductance of the flat Cu clip with length, width, and thickness of approximately 3.3 mm, 1.1 mm, and 82.5–130 μm was calculated to be approximately 1.49 nH based on [20]. These results demonstrate that the parasitic inductance of the proposed framework is lower than that of the conventional or existing frameworks. In addition, the dynamic performance is expected to be enhanced with the reduced parasitic inductance. Notably, the measured Q_{rr} of the

Table 3. Performance comparison of packaged SiC SBD devices using the same bare die [16]

		[4]	[4]	This Work
Package		TO-220 (Product)	SMD	SMD
Substrate on metal plate		-	LTCC w/ cavity	LTCC w/ cavity
Interconnection	Wire	15 mil Al (1 ea)	5 mil Al (3 ea)	[1)]Cu clip
	Length (mm)	7.1	4.5	3.3
	[2)]Inductance (nH)	5.07	2.55	1.49
Q_{rr} (nC) (@di/dt=300 A/μs, V_R=300 V)		22.17	19.92	18.02

[1)] Width: 1.1 mm, Thickness: 82.5-130 μm
[2)] Inductance calculated based on [19] and [20]

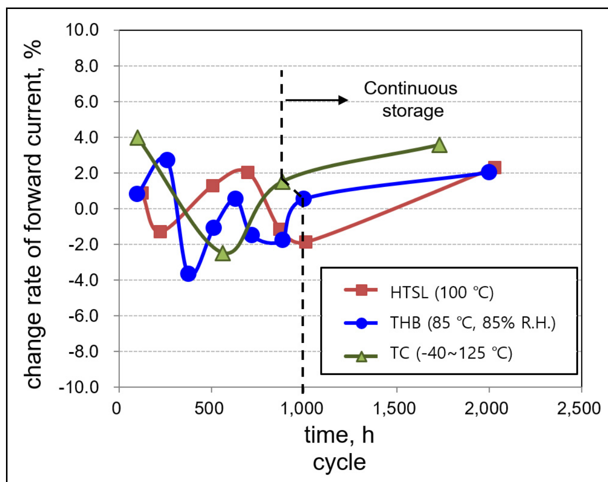


Fig. 8. Environmental reliability test results.

proposed package is 18.7% lower than that of the conventional TO-220 packaged product using the same SiC SBD bare die [16].

Fig. 8 shows the results of tests conducted to evaluate three types of environmental reliabilities: high-temperature storage life (HTSL), temperature humidity bias (THB), and temperature cycle (TC). In the HTSL test, the forward current characteristics corresponding to up to 1,000 h at 100 ℃ were measured during storage; subsequently, the forward current was measured after storage for 1,000 h. It was noted that the change rate of the forward current during storage for 2,000 h was within ±2%. The storage temperature and relative humidity of the chamber for the THB test were 85 ℃ and 85%, respectively. As in the case of the HTSL test, forward current characteristics were measured for up to 1,000 h during storage and, subsequently, the forward current

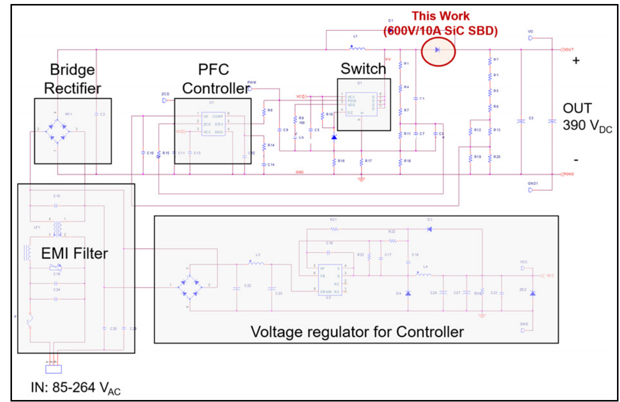


Fig. 9. Circuit diagram of the PFC converter including the proposed package.

was measured after storage for 1,000 h. The change rate of the forward current during storage for 2,000 h was within ±4%. The maximum and minimum temperature of the chamber for the TC test were –40 ℃ and 125 ℃, respectively. The forward current characteristics were measured for up to 850 cycles during storage, and the forward current was next measured after storage for 850 cycles. The change rate of the forward current during storage for 1,700 cycles was within ±4%. The results demonstrate that the proposed package exhibits excellent environmental reliability characteristics.

III. PFC Converter Including the Proposed Package

The proposed package is a SiC SBD device with a forward current of 10.5 A at a forward voltage of 1.5 V and a breakdown voltage of 600 V. It can primarily be used in the consumer electronics fields. In particular, it can be applied for power factor correction (PFC). To evaluate and demonstrate the proposed prototype, a PFC converter with the proposed package was designed and implemented. The PFC converter operated in the continuous conduction mode (CCM) and had a universal input voltage of 85–264 V_{rms} and output voltage of 390 VDC [16].

Considering the peak current flowing through the proposed SBD prototype and the inductor, the output power of the PFC converter was determined to be 150 W. The designed PFC converter consisted of an electromagnetic interference (EMI) filter, a bridge rectifier, a controller with a voltage regulator, a switch,

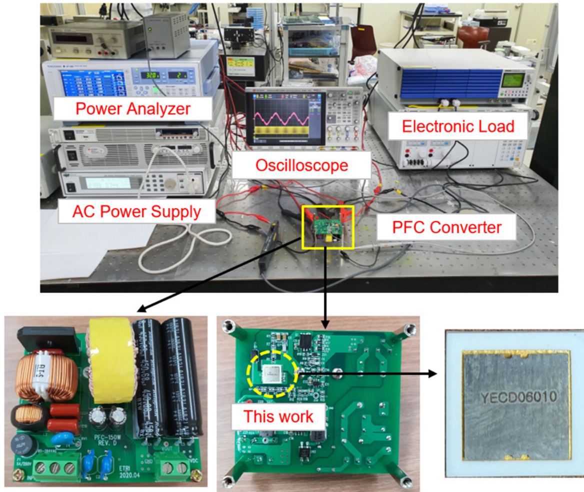


Fig. 10. Photographs of the PFC converter and test setup.

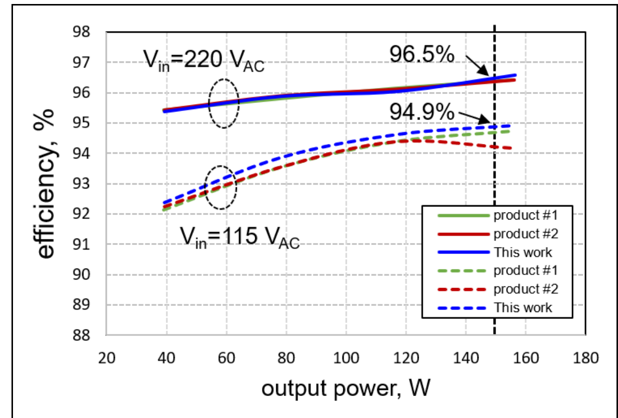


Fig. 11. Measured efficiency results of the PFC converter incorporated with the proposed package and other products of the SMD type.

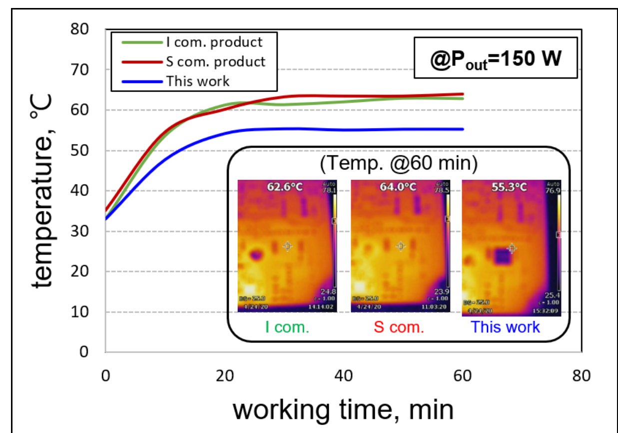


Fig. 12. Temperature variation in the three types of devices in the PFC converter as a function of the working time at an output power of 150 W [16].

many passive components (R/L/C/diode), and the proposed SBD prototype, as shown in Fig. 9.

Fig. 10 shows photographs of the top and bottom surfaces of the implemented PFC converter and the test setup environment consisting of an AC power supply as a power source, an electronic load, an oscilloscope, and a power analyzer.

Fig. 11 shows the efficiency of the PFC converter including the proposed package and commercial products. The rated voltage–current configuration of the proposed SBD and product 1 was 600 V/10 A-class SiC SBD, and that of product 2 was 600 V/8 A-class SiC SBD. The two commercial products corresponded to a conventional EMC-based surface mount package. When the proposed package was implemented, the efficiency of the converter was 96.5% at a 220 V_{AC} input and an output power of 150 W, comparable to that achieved when using other products [16]. However, when 115 V_{AC} input was applied, the efficiency of the converter was 94.9%, which was 0.2–0.8% higher than that achieved when using other products [16].

The reasons for the enhanced performance can be analyzed as follows. Under the 220 V_{AC} input conditions, the PFC converter is extremely efficient in the commercial products and the proposed prototype. In other words, under that condition, the loss of the PFC converter is small, which means that only a small amount of heat is generated, and eventually the converter efficiencies at this time are almost the same. However, under the 115 V_{AC} input condition, the efficiency of the PFC converter is relatively low. That is, because the loss of the converter is large, the heat generation is high. The switching loss of the SBD and power consumption by the current flowing through the SBD are converted into heat. This heat increases the operating temperature of the SBD, which eventually deteriorates its performance. In other words, the heat generated owing to the low efficiency of the converter deteriorates the device performance, and the difference in the performances of the devices affects the efficiency of the converter. Notably, the difference in the efficiency of the converter used in the commercial products and proposed prototype is larger under conditions involving a higher output power.

Fig. 12 shows the temperature variation in each device, which occurred while the converter was operated at an output power of 150 W for 60 min [16]. The

temperatures of the two commercial products and proposed package were measured at the top side of the EMC and ceramic on the top side, respectively. After 60 min, the temperature of the proposed package was 55.3 ℃, approximately 6.7 ℃ lower than that of other products.

V. CONCLUSIONS

A novel surface mount package structure composed of LTCC multilayer substrates for a SiC SBD power semiconductor was developed. Cavities in the LTCC multilayer substrates and a flat Cu clip bonding are used to reduce the parasitic inductance caused by chip interconnection. The proposed device achieved 18.7% lower Q_{rr} compared to that of the conventional TO-220 packaged product using the same bare die. The results of demonstration tests based on application to a PFC converter under the same conditions highlighted the superior efficiency and heat-dissipation performance of the proposed LTCC-based package over commercial SMD-type SiC SBD products.

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Dong Yun Jung received his BS degree in electronics and materials engineering (*First class honors*) from Kwangwoon University, Seoul, Rep. of Korea, in 2001, and his MS and PhD degrees *(excellence graduate)* in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea in 2003 and 2009, respectively. He studied broadband ICs for optical communications and low-power CMOS receiver circuits and 3-D modules using low-temperature co-fired ceramic (LTCC) technologies for millimeter-wave applications. He joined the ETRI, Rep. of Korea in 2003 as an engineering researcher. From 2009 to 2014, he worked with the R&D Center of Samsung Electronics as a senior engineer, where he contributed to the development of millimeter-wave ICs. Since 2014, he has worked with the ETRI as a principal researcher. His research interests include power electronics semiconductor devices and high-speed, high-efficiency power conversions for high power and energy applications. Dr. Jung received the Best Paper Award from KAIST in 2007 and 2008 and a Silver Award in the Samsung Best Paper Award competition in 2012.

Hyun Gyu Jang received his BS degree in electronics engineering from the Korea Polytechnic University, Siheung, Rep. of Korea, in 2013, and his MS in advanced device technology from the University of Science, UST, Rep. of Korea, in 2015. He mainly studied Gallium nitride power devices. In 2015, he joined the Electronics and Telecommunications Research Institute in Daejeon, Rep. of Korea, as a research engineer. His research interest includes power devices, power conversion applications, and pulsed power applications.

Jongil Won received his BS and MS in electronic engineering from Seokyeong University, Seoul, Rep. of Korea in 2008, 2010, respectively. He studied electrostatic discharge (ESD) protection devices. He has been a senior researcher at ETRI, Daejeon, Rep. of Korea since 2011. His research interests include TCAD simulation and the design, fabrication, and electrical evaluation of power semiconductor devices based on silicon and silicon carbide such as SBDs, MOSFETs, and IGBTs.

DooHyung Cho received his BS degree in electrical and electronics engineering from Dankook University in Seoul, Rep. of Korea, in 2011, and MS and PhD degrees in electronic engineering from Sogang University, Seoul, Rep. of Korea, in 2013 and 2018, respectively. He joined the ETRI, Rep. of Korea, in 2016 as a member of the engineering research team, where his research focused on power semiconductor devices.

Sungkyu Kwon received his BS, MS, and PhD degrees in electronics engineering from Chungnam National University, Daejeon, Rep. of Korea in 2011, 2013, and 2019, respectively. From 2017 to 2019, he was a research affiliate at the University of Texas in Austin, Texas, USA. He was involved with studies of 2D materials, such as TMDs and graphene, used for hetero-structure tunneling devices. In 2020, he joined ETRI, Daejeon, Rep. of Korea as a postdoctoral researcher. His research interests include implementing silicon power semiconductor devices and the reliability and low-frequency noise characteristics of nano-CMOS devices.

Seong Hyun Lee received his BS degree in electrical engineering from Pukyong National University, Pusan, Rep. of Korea, in 2009, and his integrated PhD degree *(President's Award)* in advanced device engineering from the University of Science and Technology, UST, Daejeon, Rep. of Korea, in 2015. He joined the Korea Research Institute of Standards and Science (KRISS), Daejeon, Rep. of Korea, in 2015 as a Post-Doc researcher and worked at ETRI since 2017 as a research engineer. His current research interests include the design, fabrication, and characterization of electronic devices based on Si semiconductors and next-generation electronic devices for AI applications such as neuromorphic devices and reconfigurable devices.

Kun Sik Park received his BS, MS, and PhD degrees at the Department of Material Science and Engineering at the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1991, 1996, and 2011, respectively. From 1996 to 2000, he worked for Hynix Semiconductor Inc., CheongJu, where he developed device technology for DRAM. Since 2000, he has been working at ETRI, where he is responsible for developing Si- and SiC-based devices, including power devices, CMOS, and detectors.

Jong-Won Lim received the BS, MS, and PhD degrees in physics from Chung-Ang University in Seoul, Korea, in 1988, 1990, and 1998, respectively. In 2000, he joined ETRI, Korea, as a senior research staff member, where he has been engaged in research on compound semiconductor MMIC developments for wireless telecommunications. Since 2019, he has worked as a managing director in the DMC (Defense Materials and Components) Convergence Research Department at ETRI. His current research interests include developing, fabrication, and characterizing the GaN-based HEMT devices and MMICs for millimeter-wave applications.

Yong Ha Lee received his BS degree Material Science Engineering from Ajou University, Suwon, Rep. of Korea, in 2001. He worked as a member of technical staff from 2002 to 2014 in RN2 Technologies. Since 2014, he has founded Y.TECH, an LTCC total provider company, where he currently has a CEO. (www.ytcera.co.kr)