X-band 8 × 8 phased-array 4-channel FMCW receiver in 65 nm CMOS technology

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Optimized two radar RFICs for an X-band 8 × 8 phased-array 4-channel frequency-modulated continuous-wave receiver is proposed using 65-nm CMOS technology and the beam steering operation of the receiver module is demonstrated. The 8 × 8 phased-array receiver module is constructed using 16 2 × 2 phased-array receivers and a 4-channel receiver for implementation of monopulse radar. The array size is scalable with the proposed two chips solution. The 2 × 2 phased-array receiver has novel vector-sum phase-shifter with 7-bit resolution in low supply voltage. The measured result of the phase shifter shows 7-bit phase states with a 0.37° RMS phase error and a 2.17 dB gain error over 360° sweep.

Introduction: These days, the need of small radar for the detection of unmanned aerial vehicle (UAV) or for UAV-mounted radar has been increasing. This kind of radar must have the capabilities of long range detection and fine angle detection in low power consumption. For the applications, the phased-array structure with RF phase shifting has advantages such as high antenna gain and a simpler design [1]. Also, to obtain fine angle detection resolution, monopulse radar is widely used [2].

We present two radar RFICs with which 8 × 8 phased-array frequency-modulated continuous-wave (FMCW) radar module with monopulse algorithm is realized. The integrated phase shifter (PS) has linearly controlled 7-bit phase resolution at 1.2 V low supply voltage.

Description of receiver chips: Figure 1 shows block diagrams of chips for 8 × 8 phased-array 4-channel FMCW receiver. One is 2 × 2 phased-array receiver and another one is 4-channel receiver. The 8 × 8 phased-array 4-channel receiver is composed of an 8 × 8 antenna array, which has four sectors of a 4 × 4 sub-array, 16 2 × 2 phased-array receiver chips, on-board Wilkinson power combiners, and a 4-channel receiver chip. Compared with the previous design in [3], phase resolution is increased in 2 × 2 phased-array receiver and baseband analogue blocks such as variable gain amplifier (VGA) and band-pass filter (BPF) are added in 4-channel receiver. The 2 × 2 phased-array receiver has four channels of a single-to-differential low-noise-amplifier (LNA) and phase shifter (PS), 4-channel combiner, and 50-ohm driver. The 4 channels are combined by a current summing method using a trans-conductor (Gm). The 4-channel receiver has 4 channels of a single-to-differential LNA, passive mixer, trans-impedance amplifier (TIA), BPF, VGA, and single-to-differential LO buffer. By attenuating low frequencies and passing high frequencies signals by the BPF, it is possible to correct the range based signal attenuation. Both of the chips have band-gap reference circuit and serial to parallel interface (SPI)

Figure 2 shows integrated low voltage vector-sum phase shifter circuit for high phase resolution. It is composed of the quadrature generator, vector adder, 6-bit digital-to-analogue converter (DAC), and current mirror. The quadrature generator is designed with a two-stage resistance-capacitance (RC) poly-phase filter for small area consumption and exact quadrature phase. The vector adder is constructed with two cascode variable gain amplifiers with the quadrant selection switches in the middle.

Implementation and measurement: Figure 3 shows microphotographs of chips for 8 × 8 phased-array 4-channel FMCW receiver. The chips are encapsulated in the quad-flat no-leads (QFN) packages. The sizes of the 2 × 2 phased-array receiver and 4-channel receiver are 2.43 mm × 1.78 mm and 2.42 mm × 2.72 mm, respectively. The measured performance summary of the two chips is shown in Table 1.

The measured phase response of the 2 × 2 phased-array receiver at 9.6 GHz excited by the 6-bit digital data inputs to the I/Q DACs and the

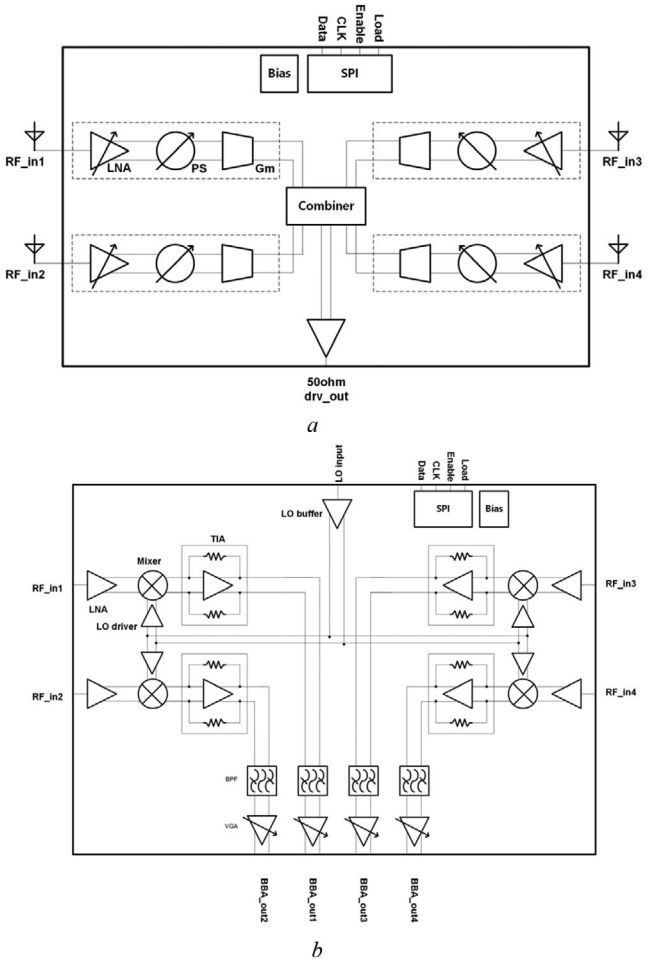

Fig 1 *Block diagrams of chips for 8 × 8 phased-array 4-channel FMCW receiver: (a) 2 × 2 phased-array receiver (RX_2 × 2), (b) 4-channel receiver (RX_4ch)*

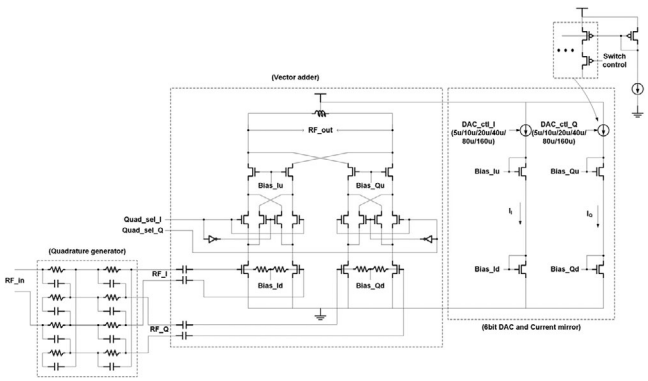

Fig 2 *Proposed low voltage vector-sum phase shifter circuit for high resolution*

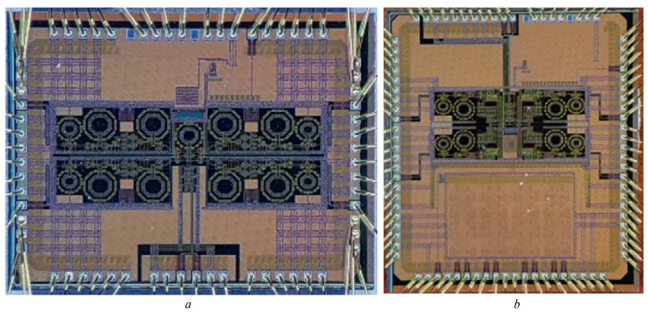

Fig 3 *Microphotographs of chips: (a) 2 × 2 phased-array receiver (RX_2 × 2), (b) 4-channel receiver (RX_4ch)*

Table 1. Measured performance summary of receiver chips

Design technology	
Technology	TSMC 65 nm GP CMOS 1P9M
Supply voltage (V)	1.2
Frequency band (GHz), 3 dB	8.6–9.8
2 × 2 phased-array receiver chip	
Number of integrated channels	2 × 2 = 4
LNA gain (dB)	20 (HG)/13 (MG)/5 (LG)
NF/single-channel (dB)	6.4
Input P1dB (dBm)	−27 (@HG)
Phase shifter resolution (bit)	7
DC current (mA)	100/4-channels
Area (mm^2), PADs included	2.43 × 1.78
4-channel receiver chip	
Number of integrated channels	2 × 2 = 4
Gain of RF front-end (dB)	15
Gain range by BBA control (dB)	13–70
LPF bandwidth (MHz)	6
DC current (mA)	130/4-channels
Area (mm^2), PADs included	2.42 × 2.72

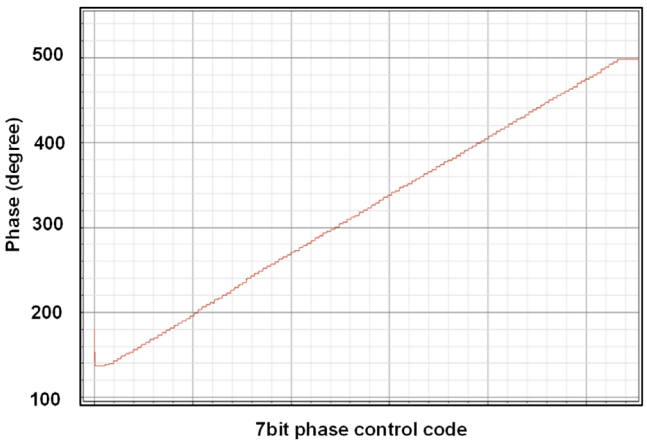

Fig 4 *Measured phase versus 7-bit control code @9.6 GHz of 2 × 2 phased-array receiver*

2-bit quadrature selection digital data input is shown in Figure 4. The measured phase data are achieved by sweeping the phase control codes using a software program from 0° to 360°. For the linearized 7-bit phase resolution, we have extracted 7-bit codes from the 8-bit control codes. The RMS phase error is approximately 0.37°, and the RMS gain error is approximately 2.17 dB over the sweep. The high phase resolution of the phase shifter is useful for the compensation of delay mismatches among many paths of phased array.

Figure 5 shows the implemented 8 × 8 phased-array 4-channel RX antenna module. The 8 × 8 rectangular patch antennas are on the front-side of the PCB module. The 16 2 × 2 phased-array chips, Wilkinson power combiners, and a 4-channel receiver chip are on the rear-side of the PCB module. The patch antennas and inputs of the 2 × 2 phased-array receiver chips are directly connected by via holes. The Rogers PCB is used in the receiver antenna module. Figure 6 shows the setup for near-field measurement of the 8 × 8 phased-array 4-channel RX antenna module. The outputs of 4-channel receiver are summed in 4-channel sum board and the summed output is converted to RF frequency by the up-converter. Figure 7 shows the measured beam steering results of the receiver module. The far-field results of the Figure 7 are converted from the near-field measurement results. The V_0, H_0 is the plot of bore-

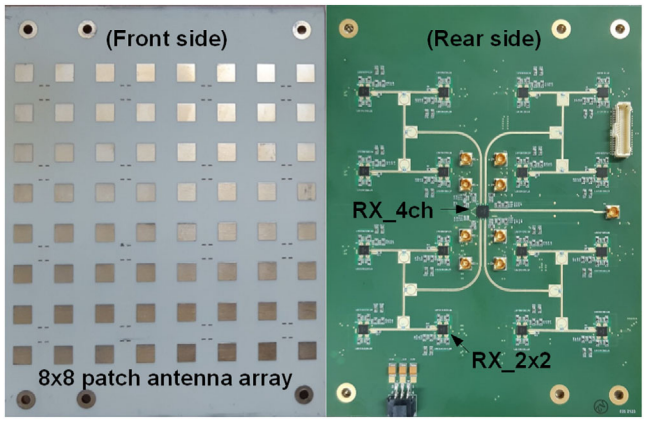

Fig 5 *Implemented 8 × 8 phased-array 4-channel RX antenna module*

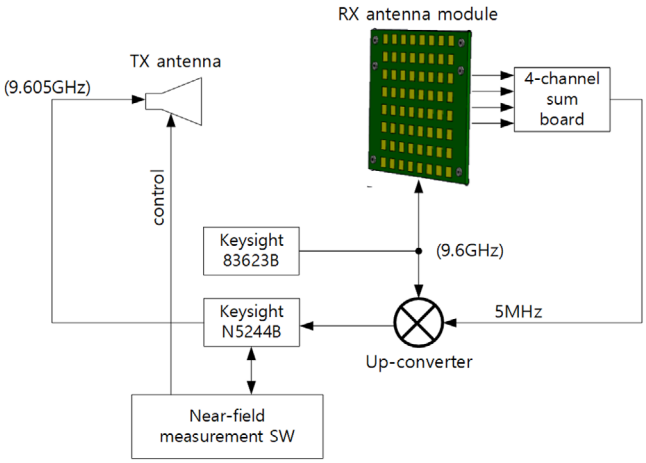

Fig 6 *Setup for near-field measurement of RX antenna module*

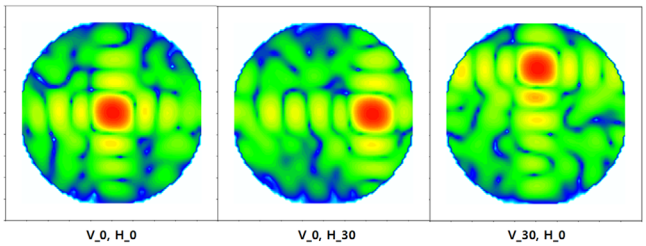

Fig 7 *Measured beam steering results of RX antenna module: far-field amplitude plot*

sight beam, the V_0, H_30 is the beam of vertical 0° and horizontal 30°, and the V_30, H_0 is the beam of vertical 30° and horizontal 0°. The beams are well controlled to exact angle according to control program. Due to H-tree array structure, well-matched PCB design of signal lines, and symmetric design among 4-channels of 2 × 2 phased-array receiver chip and 4-channel receiver chip, the measured results of the Figure 7 are achieved without phase mismatch compensation among 8 × 8 phased-array channels. The maximum side lobe levels of Figure 7 are under about -12 dB in average.

Conclusion: The two radar RFICs for 8 × 8 phased-array 4-channel FMCW receiver are designed in 65 nm CMOS technology. One is 2 × 2 phased-array receiver and another one is 4-channel receiver. The beam steering operation is successfully tested on phased-array module with 16 2 × 2 phased-array receivers and a 4-channel receiver. The phased-array structure is based on the RF phase shifting. The measurement of the 2 × 2 phased-array receiver with the proposed low voltage phase shifter circuits shows very low RMS phase and gain errors over 7-bit phase states.

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