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Analysis of issues in gate recess etching in the InAlAs/InGaAs HEMT manufacturing process

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Abstract

We have developed an InAlAs/InGaAs metamorphic high electron mobility transistor device fabrication process where the gate length can be tuned within the range of 0.13 μm–0.16 μm to suit the intended application. The core processes are a two-step electron-beam lithography process using a three-layer resist and gate recess etching process using citric acid. An electron-beam lithography process was developed to fabricate a T-shaped gate electrode with a fine gate foot and a relatively large gate head. This was realized through the use of three-layered resist and two-step electron beam exposure and development. Citric acid-based gate recess etching is a wet etching, so it is very important to secure etching uniformity and process reproducibility. The device layout was designed by considering the electrochemical reaction involved in recess etching, and a reproducible gate recess etching process was developed by finding optimized etching conditions. Using the developed gate electrode process technology, we were able to successfully manufacture various monolithic microwave integrated circuits, including low noise amplifiers that can be used in the 28 GHz to 94 GHz frequency range.

KEYWORDS
gate, HEMT, InAlAs/InGaAs, recess

1 | INTRODUCTION

Various semiconductor technologies that realize future information and communication are the most important industrial growth engines, not only now but also in the future. Interest in these applications has increased the importance of reliable semiconductor technologies that can reproducibly fabricate electronic devices with superior characteristics at higher frequencies. Among electronic devices, the high electron mobility transistor (HEMT) attracts attention as a key component operating in the millimeter wave or submillimeter wave band. These transistors have applications for devices used in radar, seekers, spectrometers, and future giga-level mobile communication technology, due their high gain, low noise, and excellent ultrahigh-frequency characteristics [1]. When a metamorphic buffer layer is applied to a GaAs substrate, an InP lattice-matched InAlAs/InGaAs epilayer can be grown to create a metamorphic HEMT (mHEMT) device. Results for monolithic microwave

integrated circuits (MMICs) using mHEMT devices have been reported [2, 3].

In the fabrication of field-effect transistor (FET)-based devices, the fine linewidth gate process, which is essential for improving high-frequency characteristics, is one of the most important process steps [4]. In this paper, we describe the key process that must be addressed in the manufacture of InAlAs/InGaAs mHEMT devices with gate lengths ranging from 0.13 µm to 0.16 µm. For good noise characteristics at the high frequency used, the cross-sectional area must be large to lower the resistance of the gate electrode while it is also necessary to minimize the Schottky contact length with the substrate. To this end, it is necessary to have a T-shaped gate cross-sectional structure; a process method for achieving this is presented in detail. In addition, process conditions to be considered in order to precisely etch the substrate under the gate electrode for high gain characteristics of the device are described. The recess process is usually performed by repeated etching until the desired drain current (I_{ds}) value is reached. For this, the resist used as an etching mask on the ohmic electrode must be opened to electrically contact the measuring probe.

When the ohmic electrode is exposed, abnormal etching behavior can occur because an electrochemical potential is established between two different materials in contact with the electrolyte. In gate recess etching, a chemical reaction by the etching solution and an electrochemical reaction occurs because the ohmic electrode contained in the electrolyte acts as an anode and the gate recess region acts as a cathode due to an electrochemical potential difference [5–7]. For example, an electrode reaction between a substrate and deionized water has been reported [8], as well as the occurrence of electrochemically induced etching nonuniformities, depending on the conductivity of the substrate [9, 10]. There are also reports that etching behavior differs depending on the surface material of the ohmic electrode and the size of the monitor opening [5, 11]. In the manufacture of compound semiconductor devices, Au is generally used as the uppermost metal electrode layer. We have reported how the size of the monitor opening and the exposed Au area affects gate recess etch characteristics [12].

Specifically, this paper can play a role in suggesting gate recess engineering factors that must be considered in determining the epitaxial structure, device design layout, gate etching method, and so on, in the manufacturing of InAlAs/InGaAs mHEMT devices.

2 | EXPERIMENTS

2.1 | Epitaxial structure

In order to fabricate the InAlAs/InGaAs mHEMT device, an epitaxial wafer (epi-wafer) having the layer structure described in Table 1 was used. InGaAs/InAlAs layers were formed after growing a metamorphic buffer layer on a 4-in. semi-insulating GaAs substrate using molecular beam epitaxy. In the basic structure with $In_{0.52}Al_{0.48}As$ as the Schottky layer and $In_{0.60}Ga_{0.40}As$ as the channel layer, there is a pulse doping layer doped with Si at 5.5×10^{12} cm^{-2} to form a two-dimensional electron gas (2-DEG). The top layer was grown with an $In_{0.53}Ga_{0.47}As$ ohmic contact layer to reduce ohmic resistance of the source and drain electrodes, doped with Si at 1×10^{19} cm^{-3} The epi-wafer of the above structure was manufactured by IntelliEPI Inc., and its characteristics included a 2-DEG charge density greater than 3.2×10^{12} cm^{-2} and a mobility greater than 9800 cm^2/Vs. The sheet resistance of the cap layer was 80 ± 5 Ω/sq.

2.2 | Device design layout

A basic device was designed to investigate gate recess characteristics. The source-drain spacing was 2 µm, and

TABLE 1 Epitaxial structure of InAlAs/InGaAs HEMT

Layer	Material	Thick. (nm)	Do-pant	Level (/cm^3)	Type
Cap	$In_{0.53}Ga_{0.47}As$	20	Si	1.0×10^{19}	N+
Schottky	$In_{0.52}Al_{0.48}As$	8	-	-	i
Pulse doping			Si	5.5×10^{12}	N
Upper spacer	$In_{0.52}Al_{0.48}As$	3	-	-	i
Channel	$In_{0.60}Ga_{0.40}As$	20	-	-	i
Buffer	$In_{0.52}Al_{0.48}As$	300	-	-	i
m-buffer	$GaAs–In_{0.52}Al_{0.48}As$	300	-	-	i
Substrate					

the unit gate width was 50 μm. The gate length was adjusted so that the contact length between the gate electrode and the InAlAs Schottky layer was 0.13 μm by controlling the lithography process conditions for forming the gate electrode. The gate electrode was T-shaped with a head size of 0.6 μm. One end of the gate electrode formed an anchor, and the other end formed a pad for connection with the other gate electrode. Basically, there were two gate electrode fingers. Figure 1 shows the layout of a device with a unit gate width of 50 μm and a total gate width of 100 μm, consisting of two gates.

As shown in Figure 1, recess monitor openings were placed on the source and drain electrodes to monitor the degree of etching by measuring the change in resistance and current between the source and drain as the gate recess etching proceeds. Two recess monitor openings were placed as close as possible to both source electrodes of the unit device, and one recess monitor opening was placed on the drain pad extended from the drain electrode.

2.3 | Device fabrication

Device fabrication began by forming an align-key on the epi-wafer for the stepper lithography process using a photomask based on the designed layout. At this time, a photoresist pattern for device isolation is also formed. The patterned photoresist was used as an etch mask for device isolation, and the substrate was etched to a depth of 200 nm for about 90 s using an etchant composed of phosphoric acid, hydrogen peroxide, and water with a ratio of 1:1:40, respectively.

Ohmic electrodes were formed by sequentially depositing Au/Ge/Ni/Ti/Au to a thickness of 34/17/11.5/11.5/120 nm, respectively. Metal deposition was performed using an electron-beam evaporator in a vacuum at less than 5×10^{-7} Torr. Formation of the ohmic electrode was completed by a lift-off method in which the deposited wafer was dipped in acetone to remove the metal film deposited on the photoresist.
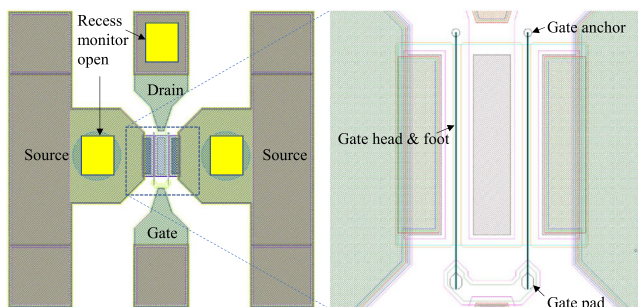
The ohmic electrode system, which achieves low contact resistance through diffusion into the substrate, generally requires rapid temperature annealing. However, in this experiment, excellent contact resistance properties were exhibited without the addition of an artificial heat treatment process. The improvement of contact resistance was not evident, even when heat treatment was carried out at 350°C for 30 s, but rather, a decrease in sheet resistance was observed due to the change in the properties of the InGaAs cap layer.

For the next part of the process, an electrode having a larger area for monitoring the gate recess was required. After patterning the photoresist using a stepper to form the so-called first metal, Ti/Au was deposited and lifted off. The first metal is required for electrical connection between devices, such as a transmission line for composing a MMIC, and Au is mainly used for low electrical resistance.

2.3.1 | Patterning for the T-shaped gate

In an InAlAs/InGaAs HEMT device used as a low noise amplifier, it is common to reduce the resistance of the gate electrode by increasing the cross-sectional area of the gate electrode to improve noise characteristics [13]. The gate foot, which represents the actual gate length, is made small, and the gate head is enlarged so that the cross-sectional shape is a T-shape. Electron-beam lithography is essential to make a gate electrode with a gate length of 0.13 μm. In addition, to form such a gate electrode, a lithography process using two or more different resists is required. In this study, an electron-beam resist system with a three-layer structure was used.

Figure 2 is a cross-sectional schematic diagram of the three-layered electron-beam resist system patterned by
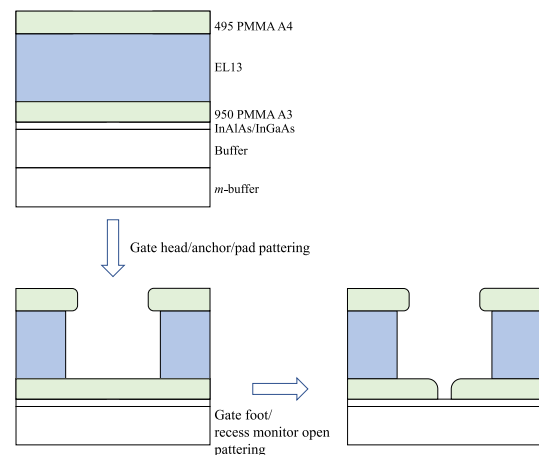

FIGURE 1 Position of recess monitor openings and the layout of a unit device with a two-finger gate

FIGURE 2 Three-layer resist system and processing steps using electron-beam lithography

electron-beam lithography. The bottom layer of resist, which determines the length and height of the gate foot, is coated with 950 PMMA A3 to a thickness of 120 nm. The middle layer and the upper layer, which determine the shape of the gate head, were coated with EL13 with a thickness of 900 nm and 495 PMMA A4 with a thickness of 140 nm, respectively.

In the lithography step for forming the so-called gate head, the gate head, gate anchor, and gate pad specified in Figure 1 were exposed to each optimized dose and beam step size. Then, MIBK:IPA (1:1) and MIBK:IPA (1:3) were used to develop upper PMMA and EL13, respectively. Due to the difference in sensitivity of the developing characteristics of each layer, the EL13 in the middle layer is undercut and the PMMA in the upper layer has an overhang structure. Therefore, the lift-off process becomes possible.

The next electron-beam exposure step was performed under optimized conditions, with higher doses for fine patterning to form the gate foot and with increased beam step size for fast processing time to form the recess monitor opening. Using the MIBK:IPA (1:3) developer, a pattern for a gate foot of <100 nm line width of the bottom resist was formed. In the case of the recess monitor opening, the development of the three-layer resist occurred at once due to the higher dose.

Figure 3 shows the results of critical dimension scanning electron microscopy (CD-SEM) observation of patterns formed by the two-step electron-beam lithography process. After the development is completed in the gate head/anchor/pad pattering stage, the three layers of electron-beam resist for the anchor and pad are all developed so that the substrate is exposed (bright area). The gate anchor and the gate pad have a sufficient contact area at both ends of the gate electrode to secure structural stability and electrical contact. It can be seen that the bottom resist (dark region) remains in the gate head region.
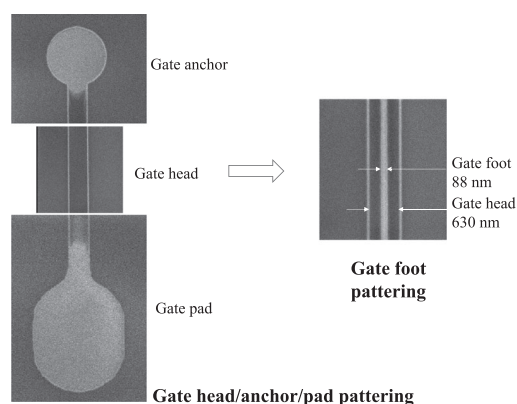
After the second step, the gate foot/recess monitor opening pattering, the line width of the gate foot pattern measured by CD-SEM was 88 nm. A descum was performed to remove any residual resist and then the width of the gate foot was increased to 110 nm.

2.3.2 | Gate recess etching

A recess etching process was performed to position the gate electrode at an appropriate depth in the InAlAs Schottky layer. An etchant comprising citric acid (10 g), hydrogen peroxide (1 ml), and water (430 ml) was used. The etch rates of the InGaAs cap layer and the InAlAs Schottky layer reacted very sensitively to the etchant composition and temperature. In this experiment, recess was performed in an etching solution maintained at a constant temperature of 32 °C. The total etching time was ~17 s, and the target resistance and current values were reproducibly reached.

Figure 4 shows the measured values of source-drain current and resistance in the recess etch steps of a device with a unit gate width of 50 μm patterned to a line width of 88 nm by electron-beam lithography. Etching was performed a total of four times until the final target current and resistance were reached. As the etching progressed, the resistance at a source-drain voltage (V_{SD}) of 0 V increased from 10.3 Ω to 18.7 Ω after the final etching was completed. The current value measured at 0.5 V decreased from 45.8 mA to 17.2 mA, and the current value measured at 1.0 V decreased from 80.6 mA to 31.3 mA. The current value measured at 1.5 V changed from an initial value greater than 100 mA to 39.4 mA.
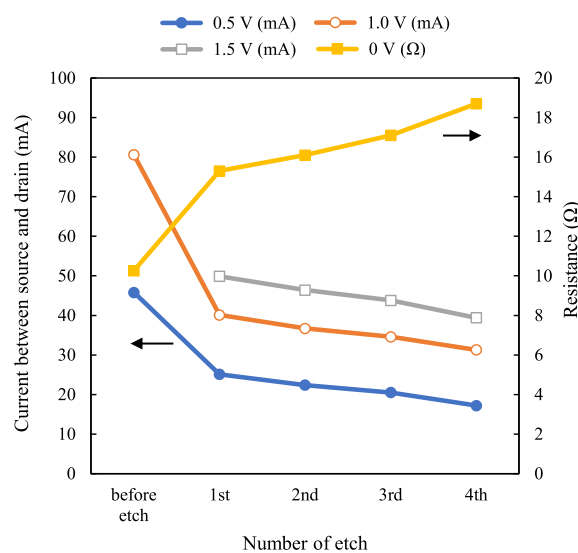

FIGURE 3 Critical dimension scanning electron microscopy (CD-SEM) analysis of two-step electron-beam lithography

FIGURE 4 Variation in source-drain current and resistance according to the number of etches

A gate metal was deposited with a thickness of 50/400 nm of Ti/Au on the etched substrate coated with electron-beam resists. Lift-off was easily achieved due to the three-layer resist structure having an overhang shape, as shown in Figure 2. The substrate was immersed in boiling acetone to minimize mechanical damage to the gate electrode during lift-off.

The wafer on which the gate electrode process was completed was passivated by depositing a 50 nm thick SiN film by plasma enhanced chemical vapor deposition. Subsequently, processes, such as via etching of the passivation film, secondary metal deposition for metal–insulator–metal capacitors, and air-bridge metal formation, were performed to complete the front-side process for MMIC fabrication [12]. Figure 5 is a SEM image of a unit device with a two-finger gate with a gate width of 50 μm. The image on the right shows the entire gate finger by magnifying the region enclosed by a dotted line in the left image in Figure 5.

3 | RESULTS AND DISCUSSION

3.1 | Cross-section analysis of devices

Figure 6 is a cross-sectional image of the gate region of the fabricated InAlAs/InGaAs HEMT device as observed by transmission electron microscopy (TEM). A thin specimen was processed using focused ion beam SEM (FIB-SEM) so that the cross-section of a specific part of the gate finger could be imaged. The thickness of the epitaxial layer was consistent with the fabrication specifications, and crystalline defects of the metamorphic buffer layer on the GaAs substrate were clearly visible. It can also be seen via TEM that the crystal defects disappeared from the InAlAs buffer layer. Source and drain ohmic electrodes composed of Au/Ge/Ni/Ti/Au were formed on

the InGaAs cap layer at a distance of 2 μm. The gate electrode is located closer to the source electrode than the drain electrode, and the gate foot was placed on the recessed epitaxial layer. The gate head shape had two peaks. It can be seen that the Ti/Au gate electrode, the source/drain ohmic electrode, and the InGaAs cap layer are covered by the SiN passivation film.

Figure 7 shows magnified TEM and scanning TEM (STEM, inset) images of the gate foot region. The thicknesses of the InGaAs cap layer, InAlAs Schottky layer, and InGaAs channel layer were measured, and the thicknesses of 20, 11, and 20 nm, respectively, were consistent with the fabrication specifications. The bottom of the gate foot (Ti) was located in the InAlAs Schottky layer and was 3.88 nm away from the top of the InGaAs channel layer. That is, the etch depth in the vertical direction of the substrate during the gate recess etching was 27 nm. The length of the contact surface between the gate foot
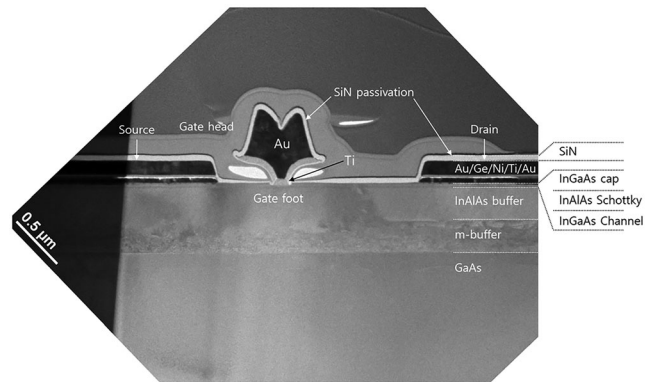

FIGURE 6 Cross-sectional transmission electron microscopy (TEM) image of source/drain and gate electrodes
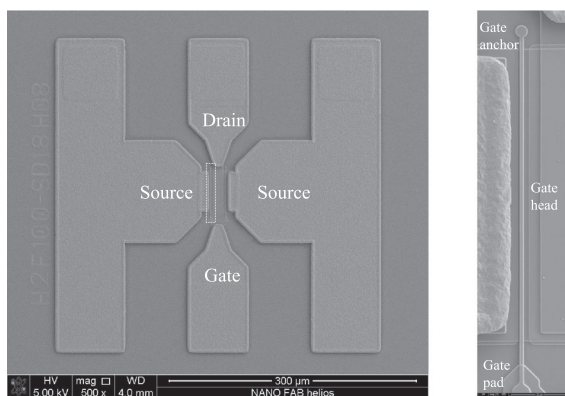

FIGURE 5 SEM image of a fabricated unit device and an enlarged image of a gate finger
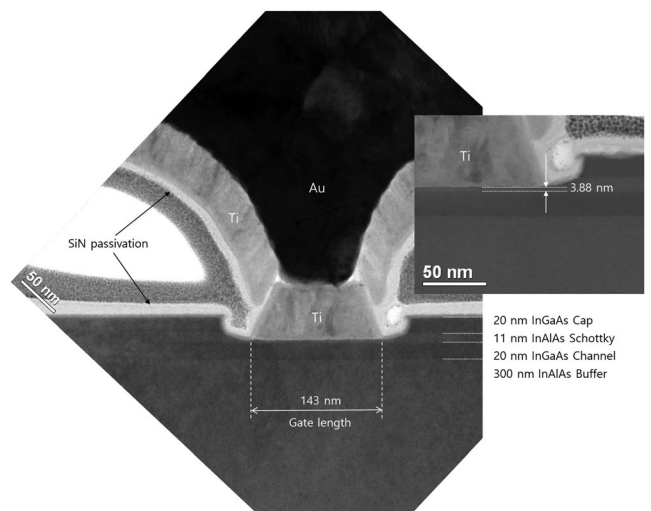

FIGURE 7 Magnified cross-sectional transmission electron microscopy (TEM) and scanning TEM (STEM) (inset) images and dimensions at the gate foot region

(Ti) and the substrate, which is called the gate length, was measured to be 143 nm. Meanwhile, during gate recess etching, the horizontal undercut etching of the substrate under the resist was measured to be 31 nm from the edge of the Ti. Since the interface between the Ti and InAlAs Schottky layers is very uniformly located at a constant height, the recess etching was very uniform. Even when the interface was microscopically enlarged through high resolution TEM, an abrupt junction interface was confirmed.

3.2 | Relationship between gate line width and etch depth

In our previous paper, we discussed that the size of the recess monitor opening affects the etching rate [12]. At this time, we intend to discuss the relationship between the etch depth and the line width changed by electron-beam lithography conditions for a two-finger gate unit device with the same recess monitor opening size. The gate line width can be changed through the dimension of the device design layout, but it can also be changed depending on the electron-beam lithography process conditions. Under the premise of electron-beam resists of the same type and thickness, electron-beam dose, beam step size, and development time are experimental variables that can change the gate line width. In this study, we focused on the change of the recess etch depth under the same recess etch conditions for several devices with artificially or intentionally changed line widths. Figure 8 shows the change in the depth of the gate recess etch with the gate length as a variable, which is directly related to the line width patterned by electron-beam lithography.
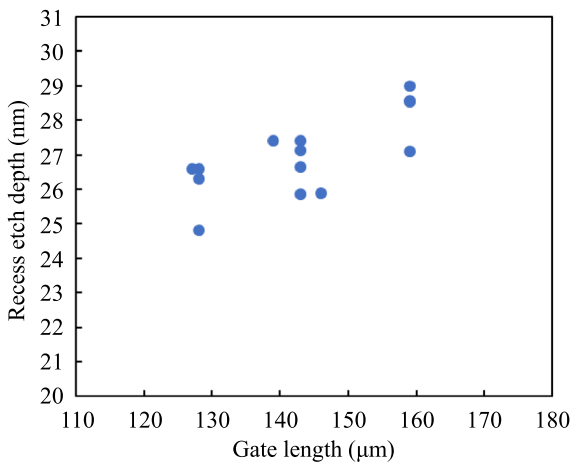
Measurement of gate length and recess etch depth from TEM images require consideration of some error. In particular, measurement methods with nanometer-scale precision are not easily accessible. Nevertheless, for devices with gate lengths of approximately 130 nm, 145 nm, and 160 nm, the recess etch depth tends to increase as the gate length increases. These results contradict the report that the recess etch rate decreases as the gate line width increases when Ni is exposed to the recess monitor opening [9, 10]. On the other hand, when Pt is exposed, there it has been reported that the etch rate increases as the gate length increases [5]. In the case of Ni, electrochemical etching characteristics are dominant. In the
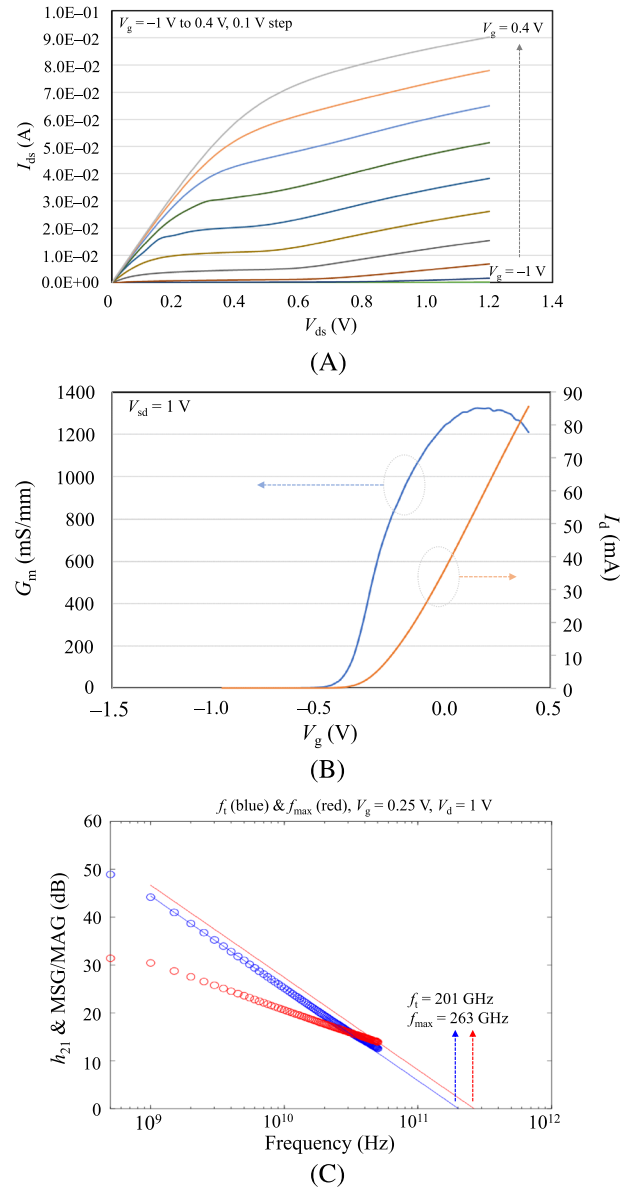

(A)

(B)

(C)

FIGURE 9 Characteristics of an InAlAs/InGaAs mHEMT with a two-finger gate: (A) current–voltage curve, (B) transconductance curve, and (C) RF performance

FIGURE 8 Variations of gate recess etch depth according to gate length

case of Pt, typical chemical etching characteristics are shown. As in this study, when Au is exposed by the recess monitor opening, it can be predicted that chemical and electrochemical etching properties coexist with reference to the aforementioned report [12].

3.3 | Electrical characteristics

The direct current (DC) characteristics of a device with a total gate width of 100 μm showed good pinch-off characteristics. Figure 9A shows the drain current (I_{ds}) curves obtained when the drain voltage (V_{ds}) was changed from 0 V to 1.2 V, and the gate voltage (V_g) was changed from −1 V to 0.4 V with 0.1 V steps. Figure 9B presents the drain current and transconductance characteristics according to the change in V_g. When the gate voltage was −1 V, the leakage current was 23.0 μA; when the gate voltage was 0.4 V, the maximum drain current was 86.5 mA. The threshold voltage (V_{th}) was −0.40 V. The maximum transconductance was 1325 mS/mm at $V_{ds} = 1.0$ V and $V_g = 0.25$ V.

The S-parameter was measured at frequencies of 0.5–50 GHz, and the bias conditions were $V_{ds} = 1.0$ V and $V_g = 0.25$ V. Figure 9C shows the RF characteristics of the current gain ($h21$) and the MSG/MAG determined from the measured S-parameter values. The current gain cutoff frequency (f_T) and the maximum resonant frequency (f_{max}) obtained by extrapolating the curves with a linear relation (slope = −20 dB/decade) were 201 and 263 GHz, respectively.

4 | CONCLUSIONS

The key process to consider for the manufacture of an InAlAs/InGaAs mHEMT device with a gate length ranging from 0.13 μm to 0.16 μm was described in detail. A specific lithography process for fabricating a device having a cross-sectional structure with a small gate resistance, in order to exhibit suitable characteristics at high frequencies, was introduced. Through a two-step electron-beam lithography process for three layers of resist, a T-shaped gate electrode with a large gate head was realized. In order to obtain gain and high-frequency characteristics, etching conditions that must be considered for the gate recess process were presented. Since the electrochemical etching reaction is involved, a device design layout that reflects this phenomenon should be made. That is, a window, such as a recess monitor opening, should be located on the source and drain electrodes to achieve uniform recess etching in all devices. As a result, using optimized InAlAs/InGaAs mHEMT process

conditions, a uniform device could be reproducibly fabricated. By fabricating a device with a gate length suitable for each frequency of use, such as 28 GHz, 38 GHz, 77 GHz, and 94 GHz, it was possible to successfully manufacture MMICs such as a low noise amplifier, mixer, and multiplier.

CONFLICTS OF INTEREST
The authors declare that there are no conflicts of interest.

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