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Four-channel GaAs multifunction chips with bottom RF interface for Ka-band SATCOM antennas

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Abstract

Receiver and transmitter monolithic microwave integrated circuit (MMIC) multifunction chips (MFCs) for active phased-array antennas for Ka-band satellite communication (SATCOM) terminals have been designed and fabricated using a 0.15-μm GaAs pseudomorphic high-electron mobility transistor (pHEMT) process. The MFCs consist of four-channel radio frequency (RF) paths and a 4:1 combiner. Each channel provides several functions such as signal amplification, 6-bit phase shifting, and 5-bit attenuation with a 44-bit serial-to-parallel converter (SPC). RF pads are implemented on the bottom side of the chip to remove the parasitic inductance induced by wire bonding. The area of the fabricated chips is 5.2 mm × 4.2 mm. The receiver chip exhibits a gain of 18 dB and a noise figure of 2.0 dB over a frequency range from 17 GHz to 21 GHz with a low direct current (DC) power of 0.36 W. The transmitter chip provides a gain of 20 dB and a 1-dB gain compression point (P1dB) of 18.4 dBm over a frequency range from 28 GHz to 31 GHz with a low DC power of 0.85 W. The P1dB can be increased to 20.6 dBm at a higher bias of +4.5 V.

KEYWORDS
active phased-array antenna, GaAs, Ka-band, MMIC, multichannel, multifunction chip, SATCOM

1 | INTRODUCTION

Active phased-array antennas are increasingly popular for satellite communication (SATCOM) terminals owing to their electronic steering ability and high signal-to-noise ratio [1]. Multifunction chips (MFCs) are essential components of phased-array antennas and perform several functions such as phase control, gain-level control, and amplification. Reducing the cost of SATCOM antennas is very important for commercial competition, and the cost of MFCs accounts for a large portion of the cost of these antennas. To reduce the cost of MFCs, it is necessary to reduce the cost per channel via chip multichannelization.

As commercial MFCs for SATCOM antennas, a complementary metal–oxide–semiconductor (CMOS)-based four-channel receiver chip [2] and a transmitter chip [3] released by Anokiwave provide remarkable performance with regard to the noise figure and 1-dB gain compression point (P1dB), respectively. The SiGe bipolar CMOS (BiCMOS)-based four-channel transceiver chip proposed by Hao [4] provides P1dB performance that is competitive with that of GaAs chips.

GaAs chips have remained competitive for antennas with up to hundreds of antenna elements or a high output power per element [5]. Because the entire bottom surface is a ground plane, GaAs chips are expected to have a lower thermal resistance and better radio frequency (RF) stability, which removes unwanted oscillation compared with CMOS chips. Ka-band chips have not been reported for GaAs-based multichannel MFCs, but multichannel MFCs operating at lower frequency bands, such as two-channel X-band chips [6] and four-channel Ku-band chips [7], have been reported. For Ka-band GaAs MFCs, which are all single-channel chips, a commercial OMMIC MFC [8] that consists of passive components without amplifiers and a receiver MFC with a wide operating frequency band [9] has been reported.

The wire bonding technique conventionally used for the interconnections between the chip and an external printed circuit board (PCB) introduces a parasitic inductance, which degrades the RF performance of the chip. In CMOS chips, the adverse effects of wire bonding can be eliminated through the flip chip assembly; however, this increases the thermal resistance owing to the reduced contact area with the PCB.

In the present study, GaAs-based four-channel monolithic microwave integrated circuit (MMIC) MFCs used for the phased-array antennas of Ka-band SATCOM terminals are implemented. The four-channel receiver chip and transmitter chip provide a low noise figure and high P1dB performance, respectively, at a low power consumption that is competitive with that of CMOS chips. In our design, RF pads are implemented on the bottom side of the chip to remove the adverse effects of wire bonding, keeping the ground plane at the bottom to reduce the thermal resistance. These chips are designed using WIN Semiconductors' commercial 0.15-μm pseudomorphic high-electron mobility transistor (pHEMT) (PE15-0P) process, which provides a hot-via process that enables bottom pad implementation [10].

2 | MULTIFUNCTION CHIP DESIGN

An MMIC receiver MFC that operates over a frequency range from 17 GHz to 21 GHz and a transmitter MFC that operates over a frequency range from 28 GHz to 31 GHz were designed for a Ka-band SATCOM antenna. The functional block diagrams of the receiver and transmitter chips are shown in Figure 1A, B, respectively. The receiver chip contains four-channel RF paths and includes a 4:1 combiner to combine these four channel outputs into one output. Each channel consists of two low-noise amplifiers (LNAs) to improve the noise figure,

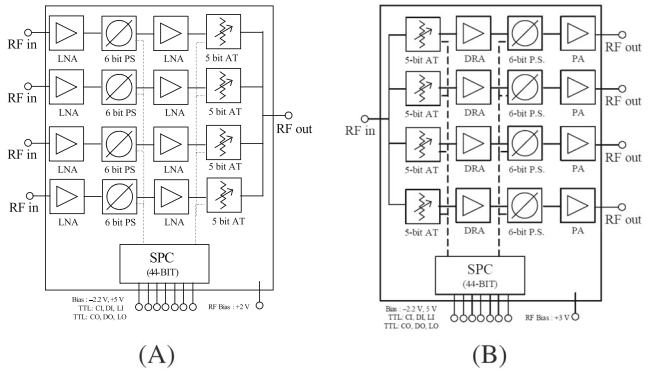


FIGURE 1 Functional block diagrams of the (A) receiver and (B) transmitter multifunction chips (MFCs).

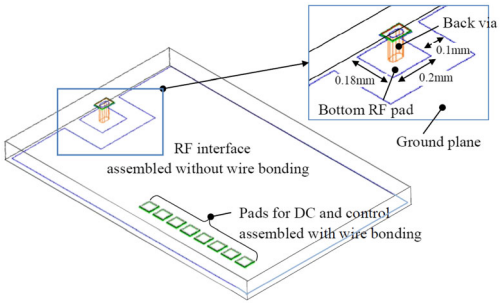


FIGURE 2 Interfacial configuration of the chip. The bottom radio frequency (RF) pads and direct current (DC)/control pads are on the upper side of the chip.

6-bit phase shifters for phase control, and 5-bit attenuators for gain-level control. A digital serial-to-parallel converter (SPC) provides 44-bit control signals to the 6-bit phase shifters and 5-bit attenuators in each of the four channels. Three biases are required: −2.2 V for the SPC circuit, +5 V for the transistor–transistor logic (TTL) outputs, and +2 V for the amplifiers integrated in the chip.

The transmitter chip has a structure similar to that of the receiver chip, including four-channel RF paths and a 4:1 divider. One RF input was divided into four inputs for each of the four channels. Each channel includes 6-bit phase shifters, 5-bit attenuators, amplifiers, and an SPC. In contrast to the receiver chip, two types of amplifiers are present in the transmitter chip—namely, a driving amplifier (DRA) and power amplifier (PA), which required a bias of +3 V.

Figure 2 shows the pad configurations of the RF, direct current (DC), and control interfaces in the chip. The RF pads were implemented on the bottom side of the chip to remove the parasitic inductance induced by wire bonding. The bottom pad was connected to the RF interface on the chip using a back via. To configure the RF pad on the bottom, it needed to be isolated from the ground plane on the bottom surface, and space between

the pad and ground plane was required. Because of this space, the configuration on the bottom of the RF pad required a relatively large area. To reduce the area of the chip, a large number of DC and control interface pads that were not affected by the parasitic inductance were placed on the upper side of the chip for conventional wire bonding. In the RF pad design, the larger size of the pad and the space between the pad and the ground plane provide easier assembly. However, this increases the parasitic capacitance of the pad and causes the microstrip mode in the matching circuit to be missing, which degrades the RF performance of the chip. The area of the RF pad and space were designed to be 0.2 mm × 0.18 mm and 0.1 mm, respectively, which are the minimum sizes for safe assembly.

The SPC circuit is composed of 3 TTL-to-direct coupled field-effect transistor logic (DCFL) converters, 44 shift registers, 3 DCFL-to-TTL converters, and 44 output drivers, as shown in the functional block diagram in Figure 3 and described in Jeong and others [11]. The TTL-to-DCFL converter converts the control voltage level from a TTL level of +5 V/0 V to a DCFL level of 0 V/−1.2 V for the main block of the SPC that operated at the DCFL level. The DCFL-to-TTL converter converts the DCFL signal level to the TTL level for the clock output (CO), data output (DO), and load output (LO).

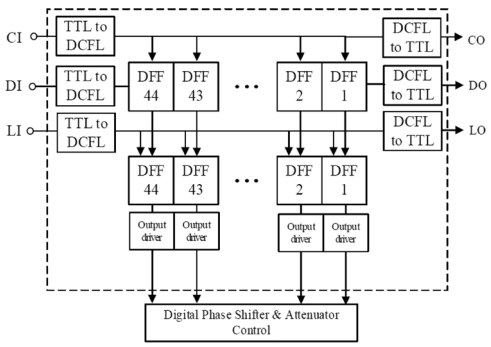


FIGURE 3 Functional diagram of the serial-to-parallel converter (SPC).

When the three TTL outputs—namely, the CO, DO, and LO—are connected to the clock input (CI), data input (DI), and load input (LI) in an adjacent MFC, the serial data enable multiple MFC controls. The shift register is the core block of the SPC and consists of two D-flip flops (DFFs). The first DFF stores data in binary form and is used to move the stored data to the next shift register once every CI cycle. Meanwhile, the second DFF is used to load the arranged data in each register into the output driver using the LI signal.

Figure 4 shows circuit diagrams of the amplifiers used in the MFCs. The sizes of the HEMTs and the values of the components are indicated. The receiver MFC requires a good noise figure and high gain to improve the gain-to-noise temperature ratio of the receiving antenna. Therefore, two LNAs are placed in the first and third blocks of the chip. Figure 4A shows the circuit diagram of the LNA. The designed LNA has a two-stage amplification structure that uses an enhanced-mode (E-mode) device and a four-finger and 25-μm unit-gate-width (4f25) high-electron mobility transistor (HEMT) with good noise performance. The input matching of the first stage was designed using noise matching to improve the noise performance, whereas the interstage and output stage were designed using interstage matching and gain matching, respectively, to improve the gain performance. Improvements in the RF stability and wideband performance were achieved using series feedback with inductors connected to the sources of the HEMTs. The inductors for series feedback were realized using microstrip lines with a narrow width and long length.

The transmitter MFC required a high output power to improve the equivalent isotropic radiated power of the transmitting antenna. Thus, a PA was placed at the output stage of the transmitter MFC. Figure 4B shows the circuit diagram of the PA. The designed PA has a three-stage amplification structure in which an E-mode 4f75 HEMT is placed at the output stage for high power output, while 4f25 HEMTs are used in the first and second stages. These two small HEMTs are expected to provide the chip with lower power consumption. Input and

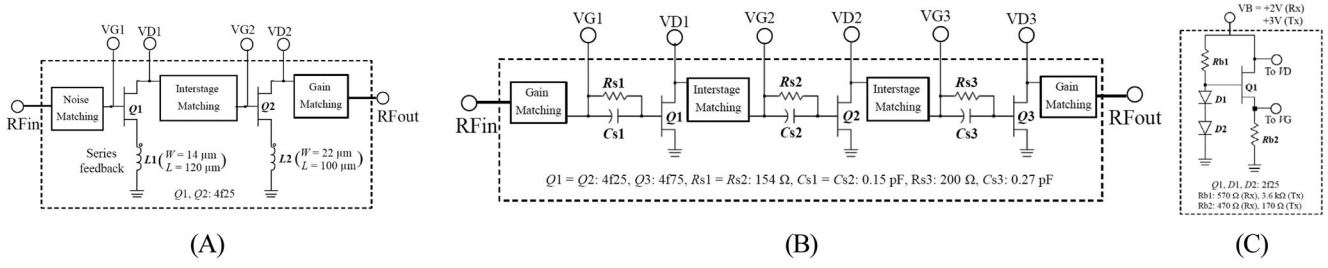


FIGURE 4 Circuit diagram of the amplifiers. (A) Low-noise amplifier (LNA) for the receiver multifunction chip (MFC). (B) Power amplifier (PA) for the transmitter MFC. (C) Active bias circuit.

output matching were performed using gain matching to improve the return loss. The resistors and capacitors connected in parallel at the gates of the HEMTs can improve the stability of the chip. The DRA shown in the chip block diagram in Figure 1B was designed using the first two stages of the PA circuits, as shown in Figure 4B. To reduce the power consumption of the chip, the small 4f25 HEMT devices were used in both stages.

All amplifiers in the MFCs operated at a single bias, which was enabled by the active bias circuit in the circuit diagram shown in Figure 4C. In addition to providing a simple interface to the chips, the active bias circuit compensates for the current variation over the temperature and threshold variations during fabrication [11]. Through the circuit, a single drain bias of +2 V was converted to a suitable gate bias of +0.4 V for the receiver MFC.

Individual 6-bit phase shifters of 5.6°, 11.2°, 22.5°, 45°, 90°, and 180° were designed using a passive-switch field-effect transistor (FET) model with three basic structures, as shown in Figure 5A–C [7]. The 5.6°, 11.2°, and 22.5° phase shifters have a switch filter structure to produce relatively small phase shifts. This structure is known to provide advantages in terms of a small chip area and small insertion loss (Figure 5A) [12]. The 45° phase shifter has a bridged-T structure that can effectively determine the phase shift using the parallel resonance between the equivalent capacitor and the inductor in the off state of the FET (Figure 5B) [13]. Phase shifters with large values of 90° and 180° were designed using a high-pass/loss-pass structure (Figure 5C) [14]. Because this structure consists of two single-pole–double-throw switches and a filter structure, it suffers from an increased chip size and insertion loss while exhibiting better wideband performance. Table 1 lists the sizes of the HEMTs used in the 6-bit phase shifters and the capacitor and inductor values. The inductors were used as microstrip lines, and their optimal inductance values were determined by adjusting their widths and lengths.

Individual 5-bit attenuators of 0.5 dB, 1 dB, 2 dB, 4 dB, and 8 dB were designed using the passive-switch FET model with two basic structures, as shown in Figure 5D,E [7]. Attenuators with relatively small attenuation values of 0.5 dB and 1 dB were designed using a switch structure consisting of only one FET and a resistor (Figure 5D) [15]. The 2-dB, 4-dB, and 8-dB attenuators were designed using a switch-T structure (Figure 5E) [15]. Because the switch and switch-T attenuators are composed of a small number of elements, they result in a small chip size and good insertion loss. Table 2 lists the sizes of the HEMTs and resistance values used in the 5-bit attenuators.

A 4:1 combiner was designed by connecting the two stages of a 2:1 Wilkinson combiner. The 2:1 combiner was designed using lumped elements instead of distributed elements to reduce the chip size.

3 | CHIP MEASUREMENT

The designed MMIC receiver and transmitter MFCs were fabricated using the commercially available PE15-0P GaAs pHEMT process provided by WIN Semiconductors with a gate length of 0.15 μm [10]. Figure 6 shows photomicrographs of the fabricated receiver and transmitter chips with an area of 5.2 mm × 4.2 mm. Both chips have four channels, and a combiner and divider are included in the receiver and transmitter chips, respectively. Four RF input interfaces—namely, RF in(1)–RF in(4)—are located on the left side, whereas one RF-out interface is located on the right side of the receiver chip, as shown in the photomicrograph of the receiver MFC (Figure 6A). One RF input interface is located on the left side,

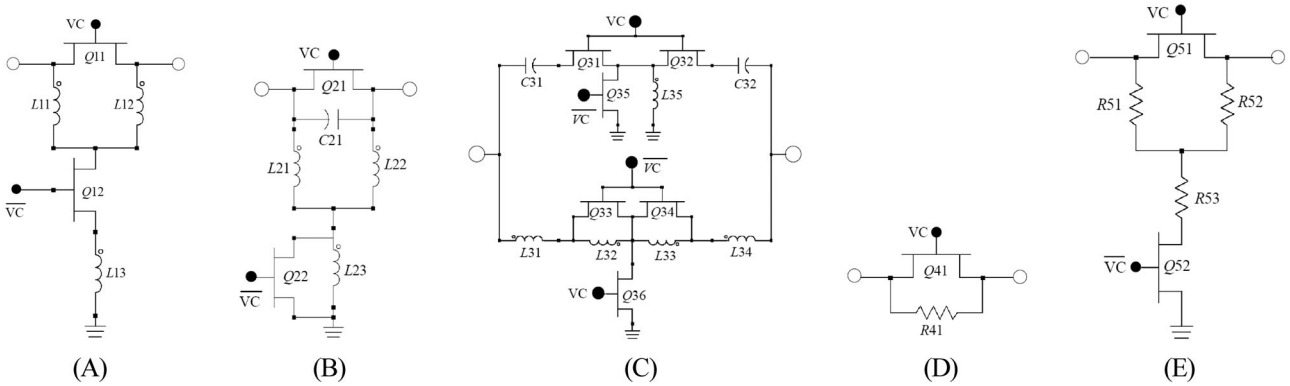


FIGURE 5 Circuit diagram of the phase shifter and attenuator. (A) Switched filter type for the 5.6°, 11.2°, and 22.5° phase shifters. (B) Bridged-T type for the 45° phase shifter. (C) High-pass/low-pass type for the 90° and 180° phase shifters. (D) Switch type for the 0.5- and 1-dB attenuators. (E) Switch-T type for the 2-, 4-, and 8-dB attenuators.

TABLE 1 Sizes of the switching HEMTs, capacitances, and inductances of the phase shifters of the receiver and transmitter MFCs.

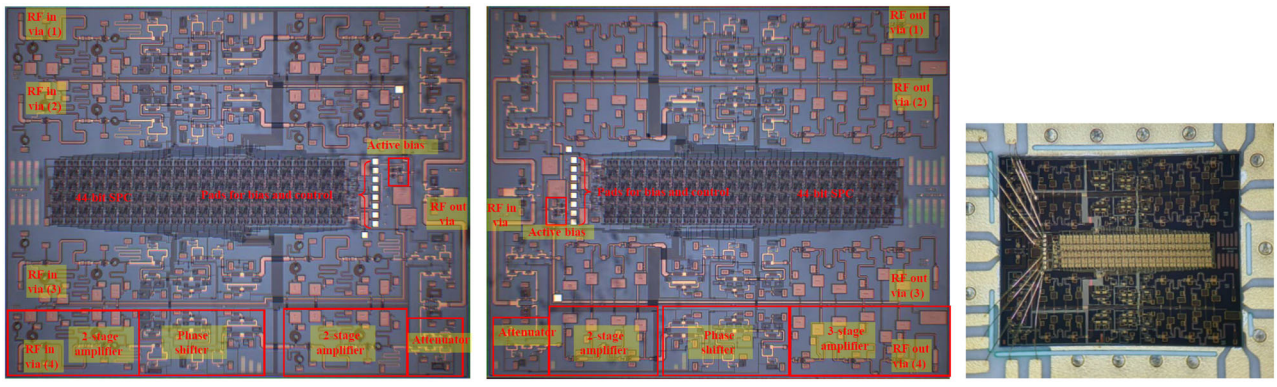
Phase shifter (°)	5.6	11.25	22.5	45	90	180
HEMT size, Rx	*Q*11/*Q*12: 4f25/2f25	*Q*11/*Q*12: 6f30/2f25	*Q*11/*Q*12: 6f25/2f25	*Q*21/*Q*22: 4f60/2f35	*Q*31 = *Q*32/ *Q*33 = *Q*34/ *Q*35/*Q*36: 6f70/4f70/2f25/ 4f40	*Q*31 = *Q*32/ *Q*33 = *Q*34/ *Q*35/*Q*36: 6f70/4f70/2f25/ 4f40
HEMT size, Tx	*Q*11/*Q*12: 4f25/2f25	*Q*11/*Q*12: 6f30/2f25	*Q*11/*Q*12: 6f25/2f25	*Q*21/*Q*22: 4f60/2f35	*Q*31 = *Q*32/ *Q*33 = *Q*34/ *Q*35/*Q*36: 6f70/4f30/2f25/ 4f40	*Q*31 = *Q*32/ *Q*33 = *Q*34/ *Q*35/*Q*36: 6f70/4f70/2f25/ 4f40
Capacitor, Rx (pF)	-	-	-	*C*21: 0.14	*C*31 = *C*32: 0.18	*C*31 = *C*32: 0.29
Capacitor, Tx (pF)	-	-	-	*C*21: 0.08	*C*31 = *C*32: 0.14	*C*31 = *C*32: 0.25
Inductor, Rx *W*/*L* (μm)	*L*11 = *L*12, *L*13: 20/120, 4/1000	*L*11 = *L*12, *L*13: 20/170, 4/1040	*L*11 = *L*12, *L*13: 20/300, 4/1060	*L*21 = *L*22, *L*23: 4/1020, 4/1600	*L*31 = *L*34, *L*32 = *L*33: 4/620, 20/160	*L*31 = *L*34, *L*32 = *L*33: 4/470, 4/390
Inductor, Tx *W*/*L* (μm)	*L*11 = *L*12, *L*13: 20/100, 4/710	*L*11 = *L*12, *L*13: 20/140, 4/720	*L*11 = *L*12, *L*13: 20/150, 4/640	*L*21 = *L*22, *L*23: 4/650, 4/700	*L*31 = *L*34, *L*32 = *L*33: 4/420, 40/160	*L*31 = *L*34, *L*32 = *L*33: 4/360, 4/340

Abbreviations: HEMT, high-electron mobility transistor; MFC, multifunction chip.

TABLE 2 Sizes of the switching HEMTs and resistances of the attenuators of the receiver and transmitter MFCs.

Attenuator (dB)	0.5	1	2	4	8
HEMT size, Rx = Tx	*Q*41: 2f25	*Q*41: 2f25	*Q*51/*Q*52: 2f25/2f25	*Q*51/*Q*52: 4f25/2f25	*Q*51/*Q*52: 4f25/2f25
Resistor, Rx = Tx (Ω)	*R*41: 14.8	*R*41: 28	*R*51 = *R*52/*R*53: 12.5/170	*R*51 = *R*52/*R*53: 18.4/103	*R*51 = *R*52/*R*53: 24.8/23

Abbreviations: HEMT, high-electron mobility transistor; MFC, multifunction chip.



(A) (B) (C)

FIGURE 6 Photomicrographs of the fabricated multifunction chips (MFCs) with an area of 5.2 × 4.2 mm^2 and a photograph of the MFC assembled on a printed circuit board (PCB). (A) Receiver MFC. (B) Transmitter MFC. (C) MFC assembled on a PCB.

whereas the four RF outputs of RF out(1)–RF out(4) are on the right side, as shown in the photomicrograph of the transmit MFC (Figure 6B). Each of the four channels contains the same RF circuits for the amplifiers, phase shifters, and attenuators, as shown in the chip photomicrograph. A small active bias circuit and 44-bit SPC are

installed at the center of the chip. Five RF pads in each chip are implemented on the bottom side of the chip to remove the parasitic inductance induced by wire bonding. To reduce the chip size, a large number of DC and control interface pads, which are not affected by the parasitic inductance, are placed on the upper surface of the chip for conventional wire bonding.

Figure 6C shows a photograph of the chip assembled on a PCB. The RF interfaces are directly attached to the PCB without wire bonding, whereas the other interfaces such as the DC and control pads are connected to the PCB using conventional wire bonding. An active bias circuit for the amplifier provides biases of +2 V and +3 V to the receiver and transmitter MFCs, respectively. The currents for the amplifiers were measured to be 127 and 248 mA in the receiver and transmitter chips, respectively. Three TTL inputs (DI, CI, and LI) and a −2.2 V bias are required for the SPC input, whereas three TTL outputs (DO, CO, and LO) and a +5 V bias are needed for the SPC output. For both chips, currents of 44 mA at −2.2 V and 1.5 mA at +5 V were measured.

Figure 7 shows the measured performance of the receiver MFC. Figure 7A shows the measured gain and input/output return losses at a drain bias of +2 V for the receiver MFC, which are compared with the design results. The measured results for the four channels are overlaid, and the gain levels of each channel are almost the same. The measured gain levels are lower than the designed levels, which we believe to be due to the additional losses induced by the combiner that were not considered in the design. The RF performance parameters such as the gain level, noise figure, and power consumption at the applied drain biases exhibit different values. The measured gain levels and noise figures at the applied biases for the receiver MFC are shown in Figure 7B,C, respectively. Table 3 summarizes the RF performance and power consumption measured at the applied drain biases for the receiver MFC. The optimal drain bias can be determined on the basis of the required gain level, noise figure, and power consumption. The optimal drain bias of the receiver chip was determined to be +2 V at a measured current of 127 mA, and the power

TABLE 3 Performance of the receiver MFC at various applied drain biases.

VD	1.5 V	1.75 V	2 V	2.25 V	2.5 V
DC power (W)	0.18	0.25	0.36	0.50	0.95
Gain (dB)	13.0	16.0	18.0	19.0	19.5
NF (dB)	2.60	2.20	2.00	1.90	1.80

Abbreviations: DC; direct current; MFC, multifunction chip.

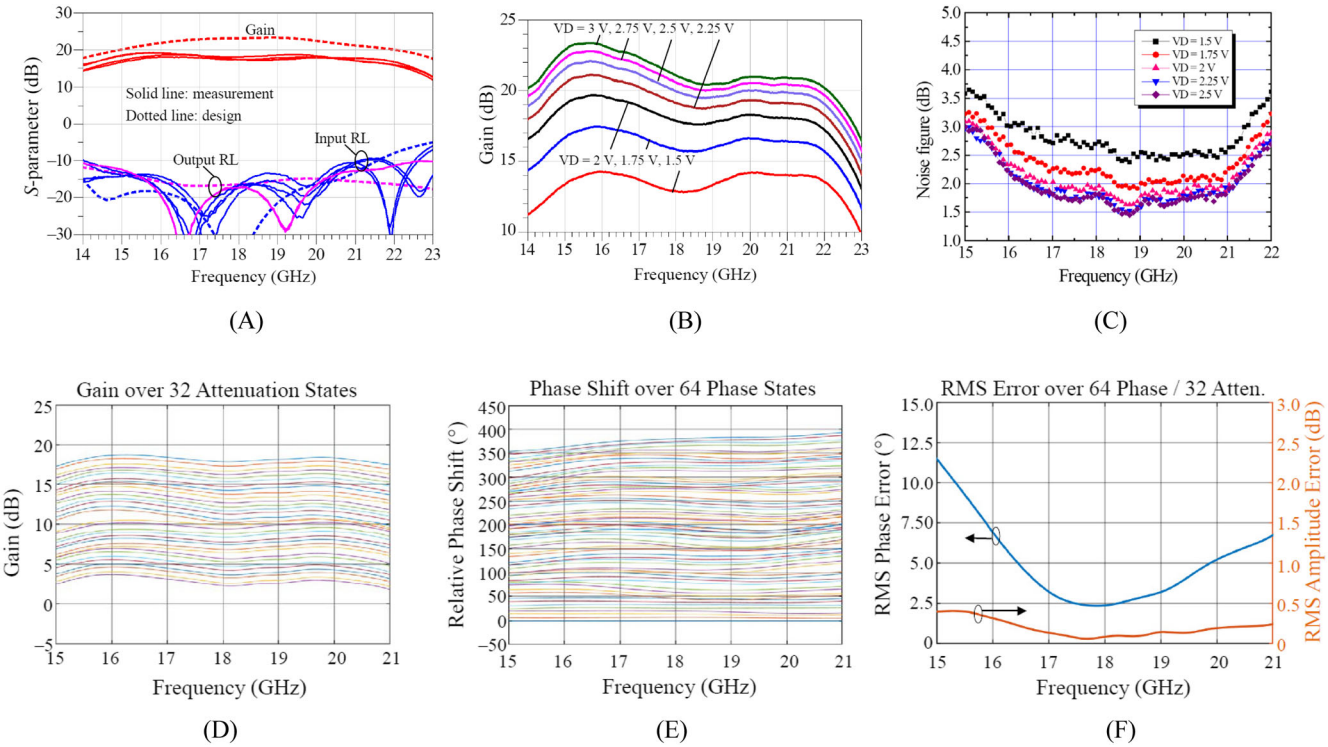


FIGURE 7 Measured results of the receiver multifunction chip (MFC). (A) Gain and return loss of each channel. (B) Gain levels for the drain bias. (C) Noise figure for the drain bias. (D) Gain level for attenuation control. (E) Relative phase shift for phase control. (F) Root-mean-square (RMS) phase and amplitude errors for phase and attenuation control, respectively.

consumption including the SPC power was calculated to be 0.36 W. Under bias conditions, the gain and noise figure were measured to be 18 dB and 2 dB, respectively, over a frequency range from 17 GHz to 21 GHz. The noise figure could be improved by 1.8 dB at a higher drain bias of +2.5 V. Figure 7D shows the gain levels for attenuation control in 32 states of the five bits for the receiver MFC, while Figure 7E shows the relative phase shift for the phase control in 64 states of the six bits for the receiver MFC. The root-mean-square (RMS) errors of the phase and attenuation controls for the receiver MFC are shown in Figure 7F. The receiver MFC exhibits slightly poor phase performance, which is mainly attributed to the frequency performance of the 90° and 180° phase shifters.

Figure 8 shows the measured performance of the transmitter MFC. Figure 8A shows the measured gain and input/output return losses at a drain bias of +3 V for the transmitter MFC, which are compared with the design results. Similar to the receiver chip, the gain levels of each channel are almost the same, and the measurement gain levels are lower than the designed levels owing to additional divider losses. The measured gain levels and P1dB for the transmitter MFC at various applied biases are shown in Figure 8B,C, respectively.

Table 4 summarizes the RF performance and power consumption measured at various applied drain biases for the transmitter MFC. The optimal drain bias of the transmitter chip was determined to be +3 V at a measured current of 248 mA, and the power consumption including the SPC part was calculated to be 0.85 W. Figure 8D shows the gain levels for attenuation control in 32 states of the 5 bits for the transmitter MFC. Figure 8E shows the relative phase shift for the phase control in 64 states of the 6 bits for the transmitter MFC. The RMS errors of the phase and attenuation controls are shown in Figure 8F for the transmitter MFC. The transmitter MFC exhibits poor attenuation performance, which may be caused by the effect of the frequency performance of the 8-dB attenuator.

Table 5 summarizes of the performance of our two MFCs and compares it with results previously reported for multichannel MFCs. Our chips have lower noise figures and higher P1dBs for the receiver and transmitter MFCs, respectively, at lower power consumption. Our

TABLE 4 Performance of the transmit MFC at various applied drain biases.

VD	2.5 V	3.0 V	3.5 V	4.0 V	4.5 V
DC power (W)	0.52	0.85	1.16	1.55	2.10
Gain (dB)	17.0	20.0	21.0	21.5	22.0
P1dB (dBm)	16.8	18.4	19.2	20.3	20.6

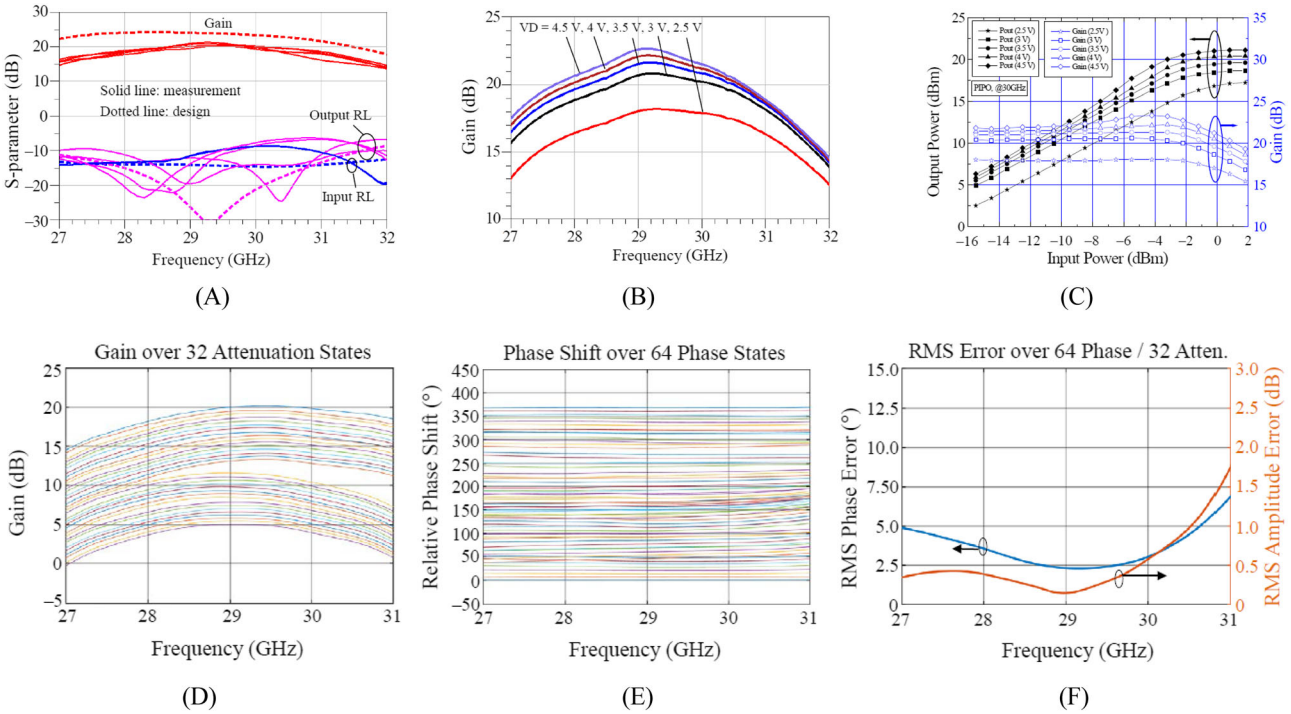


FIGURE 8 Measured results of the transmitter multifunction chip (MFC). (A) Gain and return loss of each channel. (B) Gain levels for the drain bias. (C) P1dB for the drain bias. (D) Gain level for attenuation control. (E) Relative phase shift for phase control. (F) Root-mean-square (RMS) phase and amplitude errors for phase and attenuation control, respectively.

TABLE 5 Performance summary and comparison with other studies on multichannel MFCs.

	This work Rx MFC	This work Tx MFC	Anokiwave [2]	Anokiwave [3]	Hao and Chuanchuan [4]	Zhou et al. [6]	Jeong et al. [7]	Jeong et al. [7]
Process	0.15-μm pHEMT	0.15-μm pHEMT	- CMOS	- CMOS	0.13-μm BiCMOS	0.5-μm pHEMT	0.25-μm pHEMT	0.25-μm pHEMT
Frequency (GHz)	17–21	28–31	17.7–20.2	27.5–30	8–12	7.5–9	10.7–12.75	13.75–14.5
No. of channels	4	4	4	4	4	2	4	4
Gain (dB)	18	20	26	20	13	−13	28	15
NF (dB)	2	-	2	-	11.5	-	1.6	-
P1dB (dBm)	3	18.4	-	8	13	-	-	15
Phase control (°) Range/step/bit	360/5.6/6	360/5.6/6	360/5.6/6	360/5.6/6	360/22.25/5	360/5.6/6	360/5.6/6	360/5.6/6
RMS phase error (°)	3	3	4	4	3	2	3	2.5
Amplitude control (dB) Range/step/bit	15.5/0.5/5	15.5/0.5/5	15.5/0.5/5	15.5/0.5/5	31.5/0.5/6	31.5/0.5/6	15.5/0.5/5	15.5/0.5/5
RMS amplitude error (dB)	0.2	0.4	1	0.5	0.5	0.45	0.3	0.2
DC consumption (W)	0.36	0.85	0.36	0.58	-	-	0.74	1.27
Chip size (mm^2)	5.2 × 4.2	5.2 × 4.2	-	-	9 × 6	3.5 × 4.5	5.2 × 5.2	5.2 × 5.2

Abbreviations: CMOS, complementary metal–oxide–semiconductor; DC, direct current; pHEMT, pseudomorphic high-electron mobility transistor; MFC, multifunction chip; RMS, root-mean-square.

two MFCs provide a 2-dB noise figure and 18.4-dBm P1dB at low power consumptions of 0.36 W and 0.85 W for the K-band receiver and Ka-band transmitter chips, respectively. The receiver chip [2] based on CMOS technology has a competitive noise figure, but the transmitter chip [3] has a P1dB that is 10 dB lower compared with those of our chips. Even the BiCMOS chip [4] with improved power performance still has a P1dB that is 5 dB lower. The Ku-band MFCs [7] based on 0.25-μm GaAs technology provide a competitive noise figure and P1dB but have a large DC power consumption.

4 | CONCLUSION

In this study, receiver and transmitter MMIC four-channel MFCs that can be used in active phased-array antennas for Ka-band SATCOM terminals were developed using a GaAs process. RF pads were implemented on the bottom side of the chip to remove the parasitic inductance induced by wire bonding. The chips with a 6-bit phase shifter and a 5-bit attenuator in each channel provided a 2-dB noise figure and 18.4-dBm P1dB for the receiver and transmitter chips, respectively, at a low power consumption. The P1dB could be increased to 20.6 dBm at a higher bias of +4.5 V for the transmitter MFC. The developed MMIC receiver and transmitter MFCs are expected to be applicable to SATCOM terminals implemented with planar active-phase antennas.

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CONFLICT OF INTEREST STATEMENT

The authors declare that there are no conflicts of interest.

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