Optimized recess etching criteria for T-gate fabrication achieving f_t = 290 GHz at L_g = 124 nm in metamorphic high electron mobility transistor with $In_{0.7}Ga_{0.3}As$ channel

Jong Yul Park,✉ Byoung-Gue Min, Jong-Min Lee, Woojin Chang, Dong Min Kang, E-San Jang, Junhyung Kim, and Jeong-Gil Kim

Terrestrial and Non-Terrestrial Integrated Telecommunications Research Laboratory/Electronics and Telecommunications Research Institute, Yuseong-gu, Daejeon, Republic of Korea

✉Email: jongyulpark@etri.re.kr

The authors propose criteria for recess etching to fabricate T-gate used in InGaAs high electron mobility transistors (HEMTs). By patterning additional rectangular pads on the source and drain metals in the e-beam lithography step, it is possible to measure the drain-to-source resistance (R_{ds}) and current (I_{ds}). The ratio (Γ) of before and after etching for each R_{ds} and I_{ds} can be used as criteria to determine the point in time to stop etching. By performing recess etching with Γ= 1.97 for R_{ds} and Γ= 0.38 for I_{ds} on an epiwafer having cap doping concentration of 2×10^{19} cm^{-3} and channel indium content of 0.7, the authors have fabricated InGaAs metamorphic high electron mobility transistor (mHEMT) device showing $g_{m,max}$= 1603 mS/mm and f_t= 290 GHz at L_g= 124 nm. The criteria presented can be applied to InGaAs HEMTs with various epitaxial structures.

Introduction: Metamorphic high electron mobility transistor (mHEMT) with InGaAs channel material based on GaAs substrate can be applied to monolithic microwave integrated circuit (MMIC) with high frequency [1]. Compared to the competing InP-based InGaAs HEMT, the mHEMT exhibits relatively lower performance but is more cost-effective due to cheaper substrate price, the ability to fabricate on larger wafers, and ease of handling [2]. Both InP-based HEMT and GaAs-based mHEMT can have various epitaxial structures, mainly differentiated by the presence or absence of an InP layer between the cap and barrier layers. Here, the InP layer acts as an etch stop layer during the recess etching process. After removing the cap layer through wet etching, it is possible to deposit Ti as the first layer of the gate metal stack on InP. However, it has been reported that higher gate current (I_g) flows compared to Ti/InAlAs Schottky contact [3]. Even if it is feasible to selectively remove InP with dry etching [4], this approach results in damage to InAlAs barrier so that it is crucial to find the condition to minimize the damage. Also, although wet etching methods for selective removing InP have been reported [5], it is difficult to control lateral etching due to high etch rate. An alternative method involves depositing Pt/Ti/Pt/Au on InP and performing Pt sinking [6]. However, it is important to optimize the parameters such as thickness of bottom Pt layer, and the temperature and time for Pt sinking On the other hand, not using an InP etch stop layer can avoid such issues, but there is a risk of etching into the channel during the recess etching process. To solve this problem, it is necessary to measure the drain-to-source resistance (R_{ds}) and current (I_{ds}) before and after etching to find proper time to stop the etching process. It can be done by developing additional recess pads on source and drain metals, which are coated by e-beam resists. In our previous works, we dealt with the uneven recess etch rate between fingers in multi-finger mHEMT [7] and the etching depth variation according to the foot width of the T-gate [8]. In this paper, we present criteria of performing citric acid-based electrochemical recess etching before T-gate metal evaporation to fabricate high-performance InGaAs HEMTs. We describe the fabrication process from mesa isolation to e-beam lithography for T-gate pattern formation, followed by the recess etching process. Based on the measurement results of transconductance (g_m) and cut-off frequency (f_t), we emphasize the importance of the ratios (Γ) of before and after etching for R_{ds} and I_{ds}, which are criteria for optimization of recess etching.

Fabrication process before recess etching: To fabricate InGaAs HEMT device, we used 4-inch GaAs substrate and molecular beam epitaxy (MBE) to grow epitaxial structures as shown in Table 1. First, metamorphic buffer layer, which was used to offset the lattice mismatch between GaAs and $In_{0.52}Al_{0.48}As$ buffer layer, was grown on the semi-insulating GaAs substrate by changing its In content (x) from $x = 0$ to 0.52. Then, $In_{0.7}Ga_{0.3}As$ of 10 nm was formed to be used as a channel on $In_{0.52}Al_{0.48}As$ buffer layer of 300 nm. The carrier density and channel mobility (μ_{ch}) were 2.9×10^{12} cm^2 and 10,710 $cm^2/V \cdot s$, respectively. Next, Si δ-doping of 6×10^{12} cm^{-2} was applied to supply electrons to the channel upon $In_{0.52}Al_{0.48}As$ spacer of 3 nm. Another Si δ-doping of 5.5×10^{12} cm^{-2} was applied in $In_{0.52}Al_{0.48}As$ barrier to enhance conductivity. Finally, the $In_{0.53}Ga_{0.47}As$ cap layer of 20 nm doped with Si of 2×10^{19} cm^{-3} was formed on the $In_{0.52}Al_{0.48}As$ barrier to fabricate Ohmic contacts of source and drain electrodes. The epitaxial structure designed by our research group was produced by IntelliEPI Inc. and its sheet resistance was 77.8 Ω/sq. By using this 4-inch epiwafer, mesa isolation was firstly conducted. Each HEMT device was separated by mesa having a thickness of 200 nm, which were etched by the solution of H_3PO_4:H_2O_2:H_2O= 1:1:40. As a result of transmission line measurement (TLM) with a gap of 5 μm between 100 × 100 μm mesa pads, 61 GΩ was measured, and 65 pA was flowed at 2 V, which confirms that mesa-to-mesa isolation was properly achieved. To fabricate Ohmic contact serving as a source and drain, Mo/Ti/Pt/Au was deposited by using e-beam evaporator. The source-to-drain distance of the device was designed to be 2 μm. Also, the device was designed as a two-finger T-gate with a total gate width of 100 μm. To measure the resistance of Ohmic contact, patterns with interval of 5/10/20/40/80 μm were made. As a result of TLM measurement, a contact resistance (R_c) of 0.078 Ω·mm was measured. After coating PMMA-based tri-layer to make T-gate patterns, e-beam lithography using Raith EBPG 5000 was performed . In addition, 'anchor' and 'gate pad' were added to the end of each T-gate pattern to ensure structural stability, as shown in Figure 1a.

Table 1. Epitaxial structure of InGaAs HEMT.

Layer	Material	THK	Level	Type
Cap	$In_{0.53}Ga_{0.47}As$	20 nm	$2.0 \times 10^{19}/cm^3$	N+
Barrier	$In_{0.52}Al_{0.48}As$	2 nm	–	i
First δ-doping	Si	–	$5.5 \times 10^{12}/cm^2$	N
Barrier	$In_{0.52}Al_{0.48}As$	6 nm	–	i
Second δ-doping	Si	–	$6.0 \times 10^{12}/cm^2$	N
Spacer	$In_{0.52}Al_{0.48}As$	3 nm	–	i
Channel	$In_{0.7}Ga_{0.3}As$	10 nm	–	i
Buffer	$In_{0.52}Al_{0.48}As$	300 nm	–	i
m-buffer	GaAs -$In_{0.52}Al_{0.48}As$	300 nm	–	i

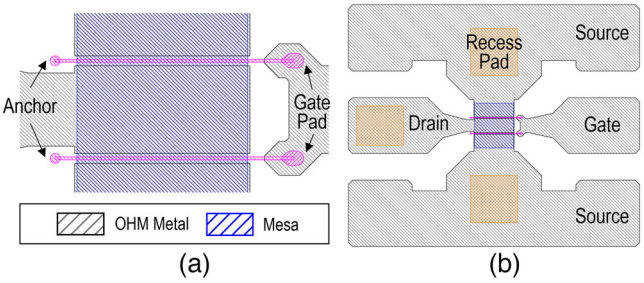

Fig. 1 *Top views of design for HEMT device. (a) Anchor and gate pad added to the end of two-finger T-gate. (b) Recess pads for monitoring* R_{ds} *and* I_{ds} *during recess etch process. HEMT, high electron mobility transistor.*

Gate recess etching: Before evaporating T-gate metal stacks, recess etching for InGaAs and InAlAs makes it possible to improve gate controllability so that higher g_m is secured. As shown in Figure 1b, rectangular pads were additionally exposed on the source and drain metals in the e-beam lithography step [7, 8]. These 'recess pads' should have a size enough to contact probe tips. In this paper, recess pads were designed to be 60 × 60 μm and 50 × 60 μm on each source and drain electrode,

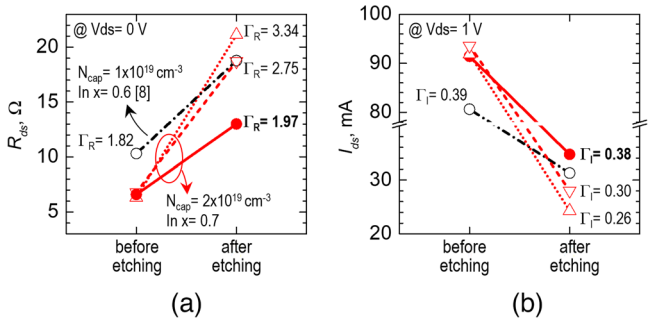

Fig. 2 *Measurement results of* R_{ds} *and* I_{ds} *for mHEMTs before and after recess etching process. (a)* R_{ds} *when biasing* V_{ds}*= 0 V. (b)* I_{ds} *when biasing* V_{ds}*= 1 V. mHEMT, metamorphic high electron mobility transistor.*

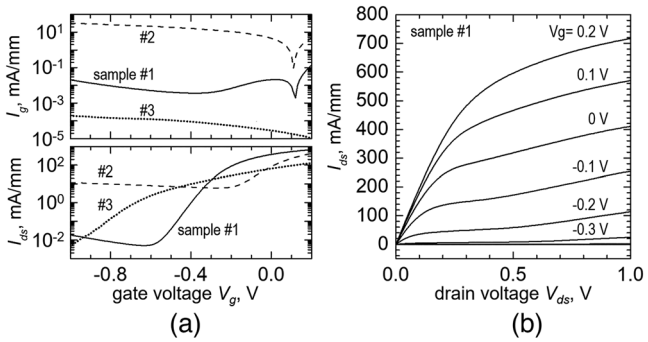

Fig. 3 *Electrical characteristics of mHEMT after T-gate fabrication. (a) Measured* V_g–I_g *plot and* V_g–I_{ds} *plot when biasing* V_{ds} *= 0.8 V. (b) Measured* V_{ds}–I_{ds} *plot for sample #1. mHEMT, metamorphic high electron mobility transistor.*

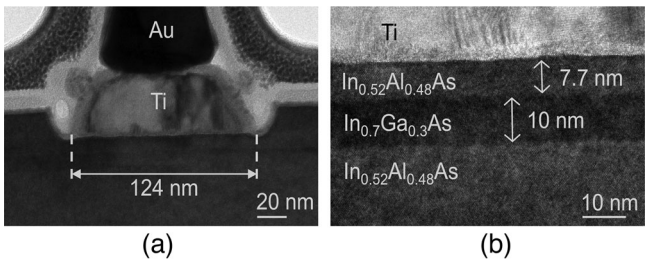

Fig. 4 *Cross-sectional TEM images of sample #1. (a) T-gate foot deposited on recessed* $In_{0.52}Al_{0.48}As$ *layer. (b) Magnified TEM image showing epitaxial structures below T-gate foot. TEM, transmission electron microscopy.*

respectively. Because etching depth varies depending on the size of the recess pad [7], it is important to design the pads to have similar sizes. By using developed recess pads, it is possible to monitor R_{ds} and I_{ds} for biased drain voltage (V_{ds}). Accordingly, it is feasible to find optimal point in time to stop etch and keep from etching of second Si δ-doping layer on the $In_{0.52}Al_{0.48}As$ spacer. Also, by using citric acid-based etchant, the InGaAs/InAlAs layers can be electrochemically etched because potential difference occurs between InGaAs/InAlAs layer opened by foot pattern and Ohmic metal opened by recess pad. In the same way as our previous paper [8], an etchant comprising citric acid (10 g), hydrogen peroxide (1 mL), and water (430 mL) was used and maintained its temperature at 32°C. To find an appropriate point in time to stop etching, we compared the experimental results for two different epitaxial structures, which have the same thickness of $In_{0.53}Ga_{0.47}As$ cap and $In_{0.52}Al_{0.48}As$ barrier/spacer, but differ in cap doping concentration (N_{cap}), the number of Si δ-doping layers, and In content of channel. Figure 2 shows the R_{ds} at V_{ds}=0 V and the I_{ds} at V_{ds}=1 V for these two epitaxial structures. Comparing R_{ds} and I_{ds} before etching for N_{cap}=1 × 10^{19} cm^{-3} (dash-dotted line [8]) and N_{cap}=2 × 10^{19} cm^{-3} (solid line, this work), high N_{cap} reduces R_{ds} and increases I_{ds}. In the pre-etching epitaxial structure, the current flows more through the cap layer, which has a lower resistance compared to the channel layer. The R_{ds} gradually increases as the thickness of the cap layer decreases by recess etching so that I_{ds} decreases. Even if the cap layer is completely etched and the InAlAs barrier is revealed, R_{ds} does not change abruptly and keep gradually increasing because Si δ-doping layers supply electrons to the channel layer and form current path. At this stage, assuming the same etching depth for both epi-structures, higher N_{cap} and dual Si δ-doping layers result in a lower series resistance. Additionally, the increased mobility due to higher channel In x content leads to an increase in I_{ds}. Finally, when the Si δ-doping layer on the spacer is etched, the resistance sharply increases and the current abruptly decreases.In the previous work, we stopped to etch when R_{ds}= 18.7 Ω and I_{ds}= 31.3 mA were measured, and the resultant device showed good performance [8]. Here, the ratios (Γ) of before and after etching for each R_{ds} and I_{ds} can be defined in equations as follows:

$$\Gamma_R = \frac{R_{ds,i=0}}{R_{ds,i=n}}, \quad \Gamma_I = \frac{I_{ds,i=0}}{I_{ds,i=n}}, \tag{1}$$

where i = 0,1,2…,n is integer and n means the number of times etching has been performed. In the case of previous work, Γ_R= 1.82 and Γ_I= 0.39. Referring to these ratios, in this work, etching was stopped when R_{ds}=13 Ω and I_{ds}=34.7 mA (sample #1, solid line) so that Γ_R=1.97 and Γ_I=0.38. Additionally, for other wafers (sample#2 and #3) with the same epi-structure of #1, more etching was carried out. In the case of sample #2 (dashed line), etching was stopped when R_{ds}= 18.7 Ω and I_{ds}= 28 mA, yielding Γ_R=2.75 and Γ_I=0.3. Lastly, for sample #3 (dotted line), additional etching was performed compared to #2, resulting in R_{ds}= 21.1 Ω and I_{ds}=24.3 mA so that Γ_R=3.34 and Γ_I=0.26. Following the etching process, the gate stack of Ti/Au=40/400 nm were evaporated on patterns of T-gate and recess pads.

Electrical characteristics: Figure 3 illustrates the device performances by measuring with Keysight HP4142 and Cascade on-wafer probe station. The measurement results of sample #1 after recess etching with V_{ds}= 0.8 V show acceptable on/off current ratio of 4 × 10^4 with I_{ds}= 1.8 × 10^{-2} mA/mm at V_g= −1 V and I_{ds}= 678 mA/mm at V_g= 0.2 V (see Figure 3a). Also, by measuring sample #1 within the voltage range of V_g= −1 to 0.2 V and V_{ds}= 0 to 1 V, we confirmed its good pinch-off performance (see Figure 3b). In the case of overetched sample #2, it exhibited a poor on/off ratio of 40 with I_{ds}= 12 mA/mm at V_g= −1 V and I_{ds}= 432 mA/mm at V_g= 0.2 V. This can be attributed to the overetching that excessively approached the Si delta doping layer on the spacer, leading to the occurrence of a high I_g (see Figure 3a). Lastly, considering the more extensively etched sample #3, the I_g decreased to 1.9 × 10^{-4} mA/mm, and the on current decreased to 128 mA/mm at V_g= 0.2 V. This suggests that even the Si δ-doping layer, which supplies electrons, has been etched. Figure 4 shows the results of transmission electron microscopy (TEM) using Tecnai F30 S-Twin after completing T-gate fabrication for sample #1. The final gate length (i.e. gate foot width) is evaluated as about 124 nm (see Figure 4a). By magnifying TEM to make the epitaxial structures more visible, it can be observed that $In_{0.7}Ga_{0.3}As$ channel on $In_{0.52}Al_{0.48}As$ buffer has a thickness of 10 nm, as designed (see Figure 4b). Above the channel, it is noticeable that the thickness of $In_{0.52}Al_{0.48}As$ remaining after recess etching is about 7.7 nm. This means that the T-gate was deposited on 4.7 nm from the second Si δ-doping layer, so it can be evaluated that the recess etching was properly performed to suppress the gate leakage. Also, as the vertical etching depth increases, the lateral etching width also widens. This characteristic of isotropic etching is consistent with the TEM images from our previous works [7, 8], indicating good controllability and reproducibility.

From the measurement results of sample #1, the threshold voltage (V_{th}) and maximum transconductance ($g_{m,max}$) of −0.47 V and 1603 mS/mm were extracted, respectively (see Figure 5a). Subsequently, the S-parameter for the frequency range of 0.5 to 50 GHz was measured using a Keysight N5245A microwave network analyzer while V_g= 0 V and V_d= 0.8 V were applied to the same device. The radio frequency characteristics of current gain (h_{21}) and MSG/MAG are shown in Figure 5b. By extrapolating with a line of −20 dB/decade, f_t = 290 GHz and f_{max} = 227 GHz were extracted.

Figure 6 describes comparison between these results (f_t and $g_{m,\,max}$) and the other values reported by various research groups. All references dealt with mHEMTs for channel In x range from 0.6 to 0.8. Firstly, we obtained a higher cut-off frequency of 290 GHz at longer gate length

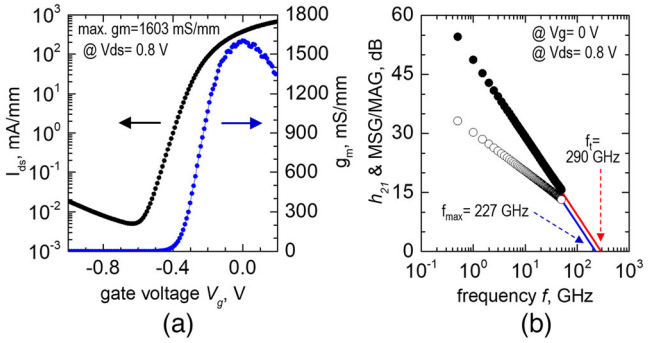

Fig. 5 *Electrical characteristics of mHEMT (sample #1). (a) Measured* V_g–I_{ds} *plot and extracted* g_m *curve at* $V_d = 0.8$ *V. (b) Calculated* h_{21} *and extrapolated line to find* f_t. *mHEMT, metamorphic high electron mobility transistor.*

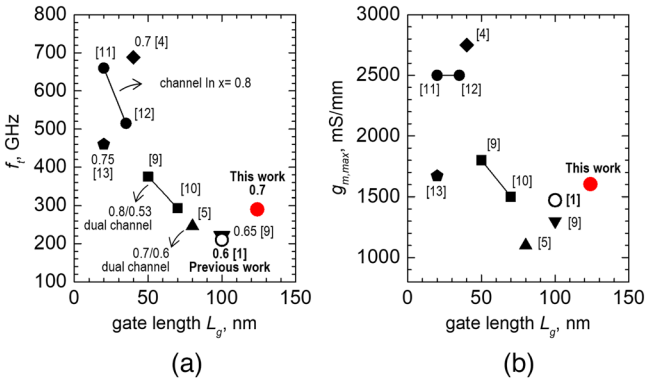

Fig. 6 *Comparison of our results with other reported values for mHEMTs. (a)* L_g–f_t *plot for results comparison. (b)* L_g–$g_{m,max}$ *plot for results comparison. mHEMT, metamorphic high electron mobility transistor.*

of 124 nm compared to the results of our previous work (f_t= 210 GHz at L_g= 100 nm [1]). Considering that recess etching was carried out properly for both devices, one of the main reasons for the difference in performance is epitaxial structure changed its channel in content from 0.6 to 0.7 and N_{cap} from $N_{cap}= 1\times10^{19}$ cm^{-3} to $N_{cap}= 2\times10^{19}$ cm^{-3}.

Next, in comparison with the results from other research groups, the f_t= 290 GHz obtained in this paper is higher than that of devices with L_g= 100 nm [9] and L_g= 80 nm [5], which have f_t values of 220 GHz and 246 GHz, respectively. Also, the f_t performance in this paper is comparable to the device reporting f_t= 293 GHz at L_g= 70 nm [10]. To analyse the reasons, it is necessary to perform a detailed analysis for each case because different epitaxial structures or device designs were used by each research group. However, a simple overview of all cases reveals that, as shown in Figure 6b, our result shows relatively high $g_{m,max}$ = 1603 mS/mm, which leads to the high f_t value according to the equation of $f_t = g_m/2\pi(C_{gs}+C_{gd})$. Hence, it can be evaluated that the optimal recess etching performed in this study led to a sufficient g_m potentially achievable by the device design and epitaxial structure.

Conclusion: We have demonstrated the recess etching technique for T-gate fabrication in InGaAs mHEMTs. By opening additional recess pads on the source and drain metals, it is possible to find the optimal point in time to stop etching by measuring R_{ds} and I_{ds}. Specifically, by referring the criteria of Γ_R= 1.82 and Γ_I= 0.39 for epiwafer having $N_{cap}= 1\times10^{19}$ cm^{-3} and channel In x = 0.6, we have adjusted the criteria and performed recess etching to be Γ_R= 1.97 and Γ_I= 0.38 for epiwafer having $N_{cap}= 2\times10^{19}$ cm^{-3} and channel In x = 0.7. As a result, we have fabricated mHEMT device showing $g_{m,max}$= 1603 mS/mm and f_t = 290 GHz at L_g = 124 nm.

Author contributions: Jong Yul Park: Conceptualization; Data curation; Formal analysis; Investigation; Methodology; Visualization; Writing – original draft; Writing – review & editing. Byoung-Gue Min: Conceptualization; Formal analysis. Jong-Min Lee: Conceptualization; Formal analysis. Woojin Chang: Conceptualization; Methodology. Dong Min Kang: Project administration; Resources; Funding acquisition; Supervision. E-San Jang: Data curation; Investigation. Junhyung Kim: Data curation; Investigation. Jeong-Gil Kim: Formal analysis.

Acknowledgements: This research was financially supported by the Institute of Civil Military Technology Cooperation funded by the Defence Acquisition Program Administration and Ministry of Trade, Industry and Energy of Korean government under grant No. 22-CM-TN-15.

Conflict of interest statement: The authors declare no conflict of interest.

Data availability statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: *14 April 2023* Accepted: *7 July 2023*
doi: 10.1049/ell2.12886

References

1 Lee, J.-M., et al.: W-band MMIC chipset in 0.1-μm mHEMT technology. *Electron. Telecomunm. Res. Inst. J.* **42**(4), 549–561 (2020)
2 Ng, G.I. et al.: Are we there yet? – a metamorphic HEMT and HBT perspective. In: *European Gallium Arsenide and Other Semiconductor Application Symposium, GAAS*, Paris, France, pp. 13–19 (2005)
3 Enoki, T., et al.: 0.1-μm InAlAs/InGaAs HEMTs with an InP-recess-etch stopper grown by MOCVD, *Microw. Opt. Technol. Lett.* **11**(3), 135–139 (1996)
4 Kim, D.-H., et al.: f_T = 688 GHz and f_{max} = 800 GHz in L_g = 40nm $In_{0.7}Ga_{0.3}As$ MHEMTs with g_{m_max}>2.7 mS/um. In: *IEEE International Electron Devices Meeting*, Washington, DC, USA, pp.13.6.1–13.6.4 (2011)
5 Ji, X., et al.: Fabrication of 80-nm T-gate high indium $In_{0.7}Ga_{0.3}As/In_{0.6}Ga_{0.4}As$ composite channels mHEMT on GaAs substrate with simple technological process. *J. Semicond.* **37**(2), 024006 (2016)
6 Shin, S.H., et al.: Buried-Pt gate $InP/In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ pseudomorphic HEMTs. *Solid State Electron.* **62**(1), 106–109 (2011)
7 Min, B.-G. et al.: A study on the behavior of gate recess etch by photoresist openings on Ohmic electrode in InAlAs/InGaAs mHEMT devices. *J. Korean Phys. Soc.* **77**(2), 122–126 (2020)
8 Min, B.-G., et al.: Analysis of issues in gate recess etching in the InAlAs/InGaAs HEMT manufacturing process. *Electron. Telecomunm. Res. Inst. J.* **45**(1), 171–179 (2023)
9 Leuther, A. et al.: 50 nm MHEMT technology for G- and H- band MMICs. In: International Conference on Indium Phosphide and Related Materials, Matsue, Japan, pp.24–27 (2007)
10 Leuther, A., et al.: 70 nm low-noise metamorphic HEMT technology on 4 inch GaAs wafers. In: International Conference on Indium Phosphide and Related Materials, Santa Babara, USA, pp. 215–218 (2003)
11 Leuther, A., et al.: 20 nm metamorphic HEMT with 660 GHz f_t. In: International Conference on Indium Phosphide and Related Materials, Berlin, Germany, pp.1–4 (2011)
12 Leuther, A. et al.: 35 nm metamorphic HEMT MMIC technology. In: International Conference on Indium Phosphide and Related Materials, Versailles, France, pp. 1–4 (2008)
13 Kim, J., et al.: SiO_2/Si_3N_4 bilayer sloped etching for 20nm InAlAs/InGaAs metamorphic HEMTs. In: IEEE International Conference on Nanotechnology, Ilsan, Korea, pp. 246–249 (2010)