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RESEARCH ARTICLE

A Self-Body-Biasing Network of Vector Sum Phase Shifter for Reduction of Output Capacitance Variation and Supply Current Variation

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ABSTRACT This paper presents the self-body-biasing effects of a vector-sum phase shifter(VSPS) in 0.13-μm CMOS technology. The self-body-biasing network is simply implemented by connecting the drain and body terminals of a vector-sum MOSFET amplifier through a single resistor. The proposed network reduces the output capacitance variations of the MOSFET amplifier and the total current variation of the phase shifter. The phase and amplitude of the phase shifter output signal are strongly influenced by these variations. The phase shifter covers full 360° by 6-bit digital control and its return loss is less than 7 dB for 64 states at 5-6 GHz. The RMS phase error is less than 3.1°, and the RMS amplitude error is less than 0.48 dB. The total current consumption is 6 mA from 1.2 V supply voltage.

INDEX TERMS Body biasing, CMOS, output capacitances, phase shifter, vector-sum.

I. INTRODUCTION

Recently, the use of wireless communications has been increasing very rapidly. Thus, 5th-generation communication is being widely studied which has more than Gbps data rate. The channel bandwidths for Gbps communications are achieved by increasing the carrier frequency. Millimeter wave and under 6 GHz bands are very strong candidates for carrier frequencies. Since the high frequency has a chance of small antenna arrays, beam forming technology is being actively pursued in 5G communication system. It also helps to have high data rates and high RF efficiencies. In a beam-forming system, a phase shifter is a key circuit that determines the direction and width of a beam. Thus, accurate and efficient phase shifters are required.

There are many types of phase shifters [1], [2], [3], among which the vector summation-type phase shifter (VSPS) has many advantages over others [3], [4], [5], [6], [7]. It has a small chip size which does not increase much with an increased number of control bits. Also, gain control functions can be integrated into the phase shifter. Thus, it has been widely used, especially in one-chip beam formers.

This work presents a self-body-biasing network to reduce the RMS phase and the RMS amplitude errors of a phase shifter. It reduces the output capacitance variation of a vector-sum amplifier by adjusting the body voltage adaptively according to the drain current.

In addition, it reduces the supply current variation by keeping a tail current source in the saturation region.

In this work, the effects of the self-body-biasing network on a 6-bit vector-sum phase shifter (VSPS) at 5 GHz were investigated. The phase shifter was implemented using a 1P8M 0.13-μm CMOS process.

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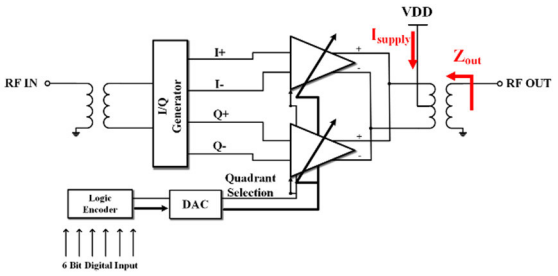


FIGURE 1. Block Diagram of the 6-bit phase shifter.

II. PROPOSED VSPS WITH SELF-BODY-BIASING NETWORK

The block diagram of the proposed 6-bit vector-sum phase shifter is shown in Fig. 1. The proposed Self-Body-Biasing network is implemented by inserting 5 kΩ resistor between body and drain of the summing transistors (M1-M8). The resistance has at least 1kΩ for saturation of the transistor. It is necessary to couple only DC voltage and block the RF signals. The I/Q generator was chosen to be an RC-CR ladder type for wideband I and Q characteristics [4].

The quadrature signals are summed up at vector-sum amplifiers to make a certain phase shift, which is selected by the DAC. Fig. 2 shows the schematic of the vector-sum amplifiers with a self-body-biasing network and the DAC. The DACs make different current ratios between the I and Q paths, which are controlled by external 6-bit digital signals. The current ratios make phase shift θ, which can be calculated as follows:

$$I_{Ipath} : I_{Qpath} = 1 : \tan^2(\theta) \tag{1}$$

where I_{Ipath} and I_{Qpath} are the bias currents that flow through the vector-sum amplifiers [3]. At first, 16 current ratios to cover one quadrant by a 5.625 ° step are obtained by (1). To express 16 different current ratios, the multiple current paths of the DAC in Fig. 2(b) are composed of six transistors which all have different sizes. It remains the total current and only steers the directions of currents to I or Q. After that, the transistor sizes are optimized by simulation to get more accurate phases. The optimized size ratio of the six transistors for each bias current is 2 / 5 / 9 / 15 / 22 / 52.

Despite of the optimization, however, the phase and amplitude errors are still significant because of the output impedance variations of the vector-sum amplifiers. As seen in Fig. 2(a), we introduced a self-body-bias network to reduce the errors by simply connecting the drain and body terminals with a single resistor.

A. OUTPUT CAPACITANCES VARIATIONS

A vector-sum phase shifter provides phase shifts by adding the outputs of I and Q vector-sum MOSFET amplifiers, which the output phase should keep the same to make an accurate phase. However, the MOSFET amplifiers experience several operation regions, which causes inevitable output capacitance changes.

Note that a simple self-body-biasing network of the vector-sum amplifier can reduce this variation. Fig. 3 shows the simulated output capacitances with respect to the drain current with three different body terminations. One is the self-body-biasing, and another is a conventional body-source tied case, and the other is giving fixed biases to the body terminal, where the biases are from 1.2 V to 1.12 V.

Since the drain current changes from 0 to 2.8 mA in vector-sum operation, there must be transitions of the amplifier between the cut-off and saturation regions. This causes a large variation of the output capacitance. However, the self-body-biasing network makes it smaller by more than three times compared to the typical body-source tied case. This is because the body biases of M1-M8 are changed adaptively as follows.

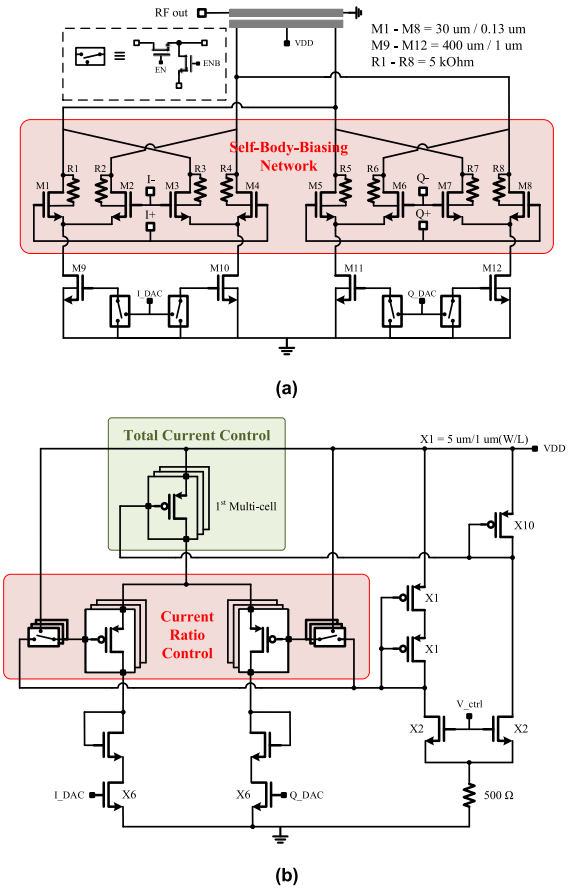


FIGURE 2. Schematics of (a) the proposed VSPS and (b) DAC.

When the drain current increases, the voltage drop from the drain to the body also increases. This causes the body voltage to decrease. As a result, the threshold voltage of the MOSFET amplifier increases slowly as shown in Eq.(2).

$$V_{TH} = V_{T0} + \gamma \left(\sqrt{|V_{SB} + 2\phi_F|} \right) - \sqrt{\phi_F} \tag{2}$$

where V_{TH} is the threshold voltage, V_{T0} is the threshold voltage for zero body voltage, γ is the body effect parameter, V_{SB} is the source-to-body voltage, and $2\phi_F$ is the surface potential.

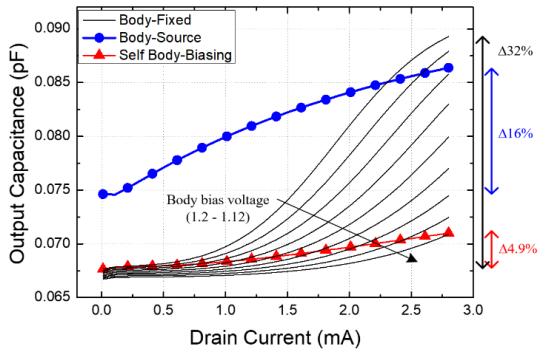


FIGURE 3. Simulated output capacitance variations of a MOSFET amplifier respect to drain current.

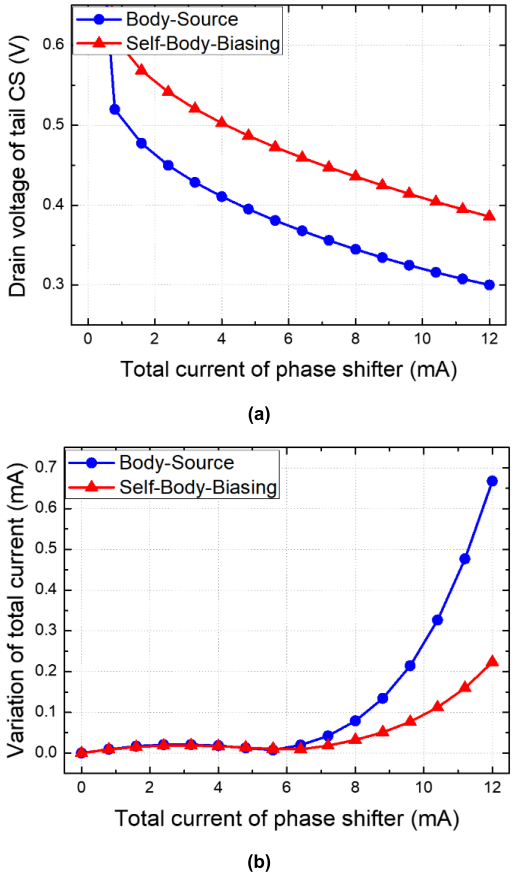


FIGURE 4. Simulated (a) the minimum drain voltage of the tail current source and (b) total current variations of phase shifter.

As seen in Fig. 3, when the body terminal is 1.2 V, its threshold voltage is the lowest, and the transition region of the output capacitance appears at a low drain current. The decrease in the body voltage makes the transition region appear at a higher current, so the output capacitance of the self-body-biased amplifier shows a flat curve. This allows the amplifier to maintain the same output phase with drain current variations for vector-sum operations.

B. TOTAL SUPPLY CURRENT VARIATIONS

The vector-sum amplifier of the phase shifter is designed to have small variations of not only the output capacitance but also the output impedance. If the output impedance of the phase shifter changes, the output phase obtained by summing the I and Q path signals can be altered. To keep the output impedance unchanged, the total current through the vector-sum amplifiers should be kept the same during the entire operation range.

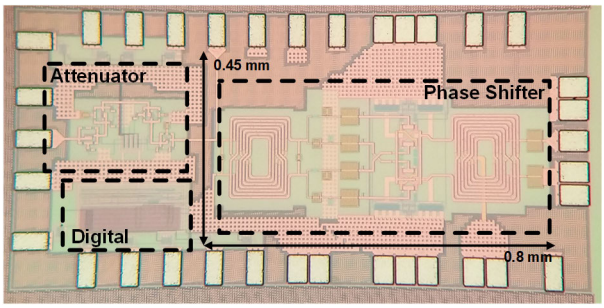


FIGURE 5. Microphotograph of the fabricated phase shifter chip.

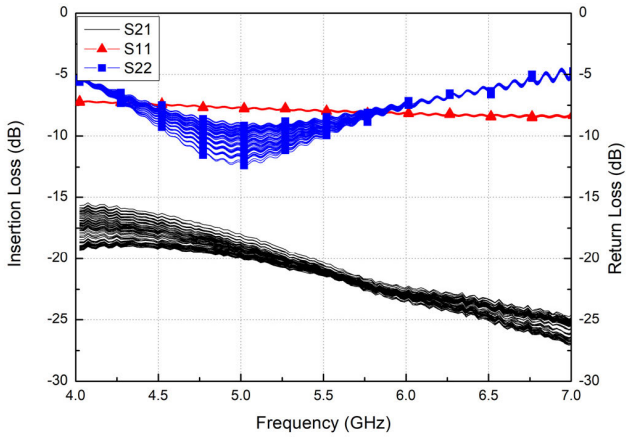
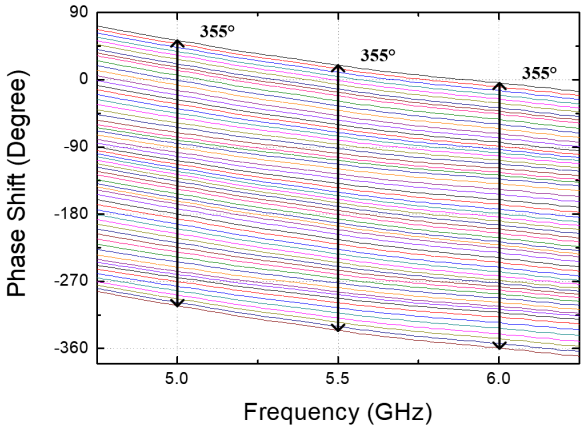
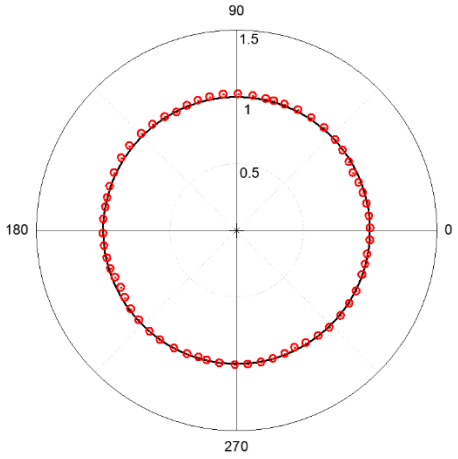


FIGURE 6. Measured insertion loss and return loss.

The total current variation is due to the tail current variation. The tail current source copies the currents from the DAC, which must operate in the saturation region not to be affected by the drain voltage. As seen in Fig. 4(a), the drain voltage of the tail current source with the self-body-biased vector-sum amplifier is about 0.1 V higher than that of the conventional body-source tied case. Since the threshold voltage of the vector-sum amplifier becomes lower, its gate to source voltage naturally decreases. Therefore, the drain voltage of the tail current source is kept high, which makes it remain in the saturation region. The variation of the total current is shown in Fig. 4(b). Since the phase shifter has been designed to have a total current of around 6 mA, the total current variations are not very different in the two cases. If the total current is increased to have more power, this effect becomes very serious.



(a)



(b)

FIGURE 7. Measured 64 states of (a) phase shifts at 5 – 6 GHz and (b) phase shifts with normalized amplitude at 5.5 GHz.

III. IMPLEMENTATION AND MEASUREMENT

A microphotograph of the proposed 6-bit vector-sum phase shifter with the self-body-biasing network is shown in Fig. 5, which was fabricated with a 1P8M 0.13-μm CMOS technology. The phase shifter core area is 0.8 × 0.45 mm^2 excluding pads, and the DAC with logic encoder area is 0.26 × 0.12 mm^2. The attenuator is just included on the reference state which will be reported elsewhere. The phase shifter consumes around 6 mA from a 1.2 V supply voltage, including the DAC. The insertion loss and return loss are shown in Fig. 6. Return losses (S11, S22) are under −5 dB from 4 to 7 GHz. And insertion loss has −17 dB at 5 GHz, which includes −12 dB insertion loss of attenuator at reference state. As seen in Fig. 7, from 5 to 6 GHz, all the 64 phase states are equally spaced. Also, the amplitude maintains the unit circle. The return loss is higher than 7 dB. At the center frequency, the RMS phase error is 1.78 °, and the RMS amplitude error is 0.2 dB.

Table 1 compares the performance of reported vector-sum phase shifters of 5 GHz-bands. The proposed phase shifter with the self-body-biasing network achieves the lowest RMS phase and amplitude errors.

TABLE 1. Performance Comparison of VSPS.

Reference	[3]	[5]	[6]	**This Work**
Technology (μm)	CMOS (0.13)	CMOS (0.13)	BiCMOS (0.25)	**CMOS (0.13)**
Frequency (GHz)	6 - 18	4.9 – 5.9	8 - 12	**5 - 6**
RMS phase error (°)	< 10	< 9.7	< 6.4	**< 3.1**
RMS amplitude error (dB)	< 1.7	< 0.7	< 2	**< 0.49**
Phase resolution (°/°)	22.5 / 360	5.625 / 360	5.625 / 360	**5.625 / 360**
Power consumption (mW)	8.7	28	110	**7.2**
Size (mm^2)	0.45	0.303*	1.65*	**0.36***

* core size

IV. CONCLUSION

A self-body-biased VSPS was implemented using 0.13-μm CMOS technology. It shows very low RMS phase and amplitude errors by reducing the variations of the output capacitance and the total current. The proposed body bias network of the vector-sum amplifiers is very size effective and easily implemented.

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