

Received 11 October 2024, accepted 10 November 2024, date of publication 13 November 2024,  
date of current version 21 November 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3497010

## RESEARCH ARTICLE

# A 120 GHz Hybrid Low Noise Amplifier in 40 nm CMOS

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This work was supported in part by the ICT Research and Development Program of MSIT/IITP, Development of Ultra-Precision Low-Cost Sub-THz Pulse-Based Radar Chip Technology, under Grant 1711193460; and in part by the Ministry of the Trade, Industry and Energy (MOTIE) and Korea Institute for Advancement of Technology (KIAT) through the International Collaborative Research and Development Program under Project P0019789.

**ABSTRACT** In this paper, we present a 6-stage 120 GHz hybrid low noise amplifier (LNA) for sub-THz radar systems. To enhance the noise figure (NF) and gain performance of the LNA, we propose a hybrid architecture that utilizes a combination of 2-stage single-ended and 4-stage differential common-source amplifiers. The first 2-stage single-ended common-source amplifier provides low-loss and low-noise characteristics, while the 4-stage differential common-source amplifier provides high gain, resulting in low noise and high gain performance. Implemented in a 40 nm CMOS process, the LNA occupies a chip area of 0.099 mm<sup>2</sup> excluding the pads. The measurement results show that the proposed LNA achieves a low NF of 5.5 dB, a high gain of 27.5 dB, and an input 1-dB compression point of -29.5 dBm at 122.5 GHz with a power consumption of 27.4 mW.

**INDEX TERMS** 120 GHz, common-source, CMOS, D-band, hybrid LNA, low-noise amplifier, millimeter-wave, noise figure, sub-terahertz.

## I. INTRODUCTION

Recently, sub-terahertz (sub-THz) and millimeter-wave (mm-wave) bands have emerged in response to growing interest in various applications such as high data-rate communications, radar, security imaging, and sensors [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. Sub-THz and mm-wave bands use large signal bandwidths and provide ultrahigh data rate, small displacement detection, and high range resolution under small form factor.

With recent advances in silicon-based technology, CMOS is widely used due to its small footprint, low cost, and low power consumption, along with an on-chip antenna and high-level integration. However, CMOS-based mm-wave and sub-THz systems suffer from lower power gain and higher noise figure (NF) as operation frequencies approach the maximum oscillation frequency ( $f_{\max}$ ), which degrades performance in terms of power dissipation, signal-to-noise ratio

(SNR), and chip area. Furthermore, passive elements limit these performances.

One of the most important building blocks in a receiver is the low-noise amplifier (LNA). As a key component of the receiver, the LNA determines the NF of the receiver. Additionally, the gain of the LNA is important to prevent NF degradation due to subsequent stages, including mixer and baseband amplifiers. Inductively degenerated common source (CS) amplifiers are popular for simultaneous noise and gain matching at the cost of gain reduction [13], [14]; however, inductive degeneration is avoided in the sub-THz band due to gain limitations. Various CMOS-based sub-THz LNAs have been reported to improve performance [15], [16], [17], [18], [19], [20], [21]. Differential CS with cross-coupled capacitive neutralization technique is widely employed due to better gain and stability in the sub-THz band [15], [16], [17]. However, the loss of the input transformer (TF) balun and the difficulty in simultaneous noise and gain matching degrade the NF. Single-ended CS LNAs with a staggered tuning multistage design have been proposed [18], [19]. These LNAs

The associate editor coordinating the review of this manuscript and approving it for publication was Jagadheswaran Rajendran<sup>1</sup>.

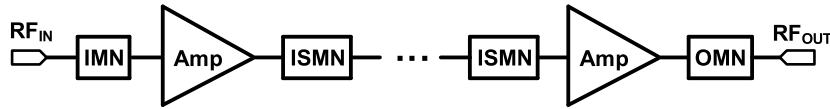


FIGURE 1. Block diagram of LNA with matching networks.

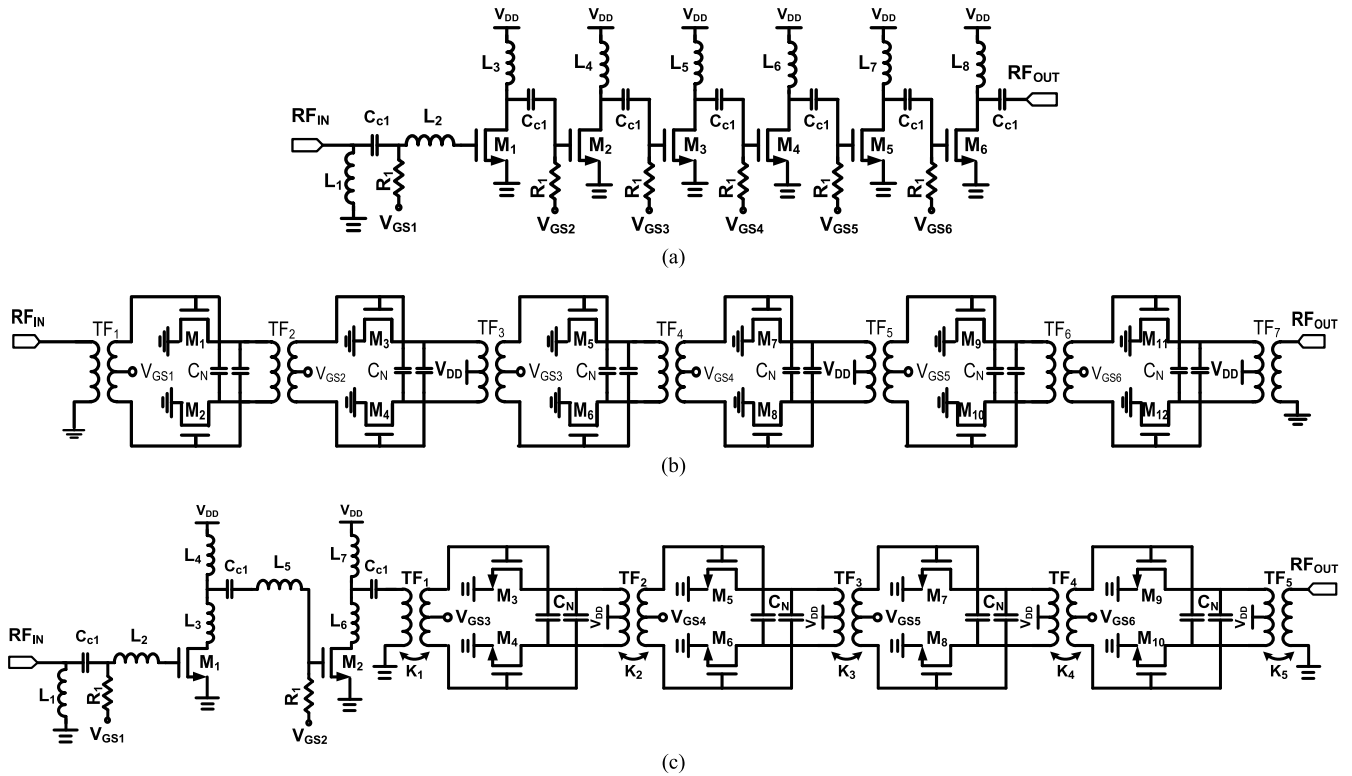


FIGURE 2. Schematics of (a) 6-stage single-ended CS LNA, (b) 6-stage differential CS LNA, and (c) proposed 6-stage hybrid CS LNA.

provide wideband performance, but their gain and NF are still limited.  $G_{\max}$ -core LNA with transmission line feedback shows high gain and low NF [20], [21]. However, the  $G_{\max}$ -core LNA shows a huge mismatch between measurement and simulation due to its sensitive  $G_{\max}$ -core and imperfect modeling.

In this paper, we present a 6-stage hybrid LNA for 120 GHz radar applications with a bandwidth of 5 GHz (120–125 GHz) and an input power level for the LNA of less than  $-40$  dBm. As a result, the LNA design focuses on achieving low noise and high gain with low power consumption, rather than prioritizing wide bandwidth and high linearity. The proposed LNA utilizes a hybrid combination of a 2-stage single-ended CS amplifier and a 4-stage differential CS amplifier for lower NF and higher gain. The first 2-stage single-ended CS amplifier provides low impedance matching loss and low-noise characteristics, while the 4-stage differential CS amplifier provides high gain, resulting in both low noise and high gain performance.

Section II describes the circuit design of the proposed 120 GHz hybrid LNA. In Section III, the measurement results

of the designed LNA are described. Finally, conclusions are presented in Section IV.

## II. CIRCUIT DESIGN

In the frequency band below 10 GHz, the NF of the receiver is mainly determined by the first single-stage of the LNA. However, the low gain of the single-stage contributes to NF degradation in the sub-THz band. Also, the loss of the matching network (MN) at the first and second stages of the LNA further degrades NF. Therefore, NF, gain, and impedance matching loss should be carefully considered for the sub-THz band.

### A. ANALYSIS OF GAIN AND NOISE FIGURE

Fig. 1 shows the block diagram of a general LNA. The LNA consists of an input MN (IMN), inter-stage MNs (ISMNs), an output MN (OMN), and single-stage amplifiers. The MN can be implemented with transmission lines, inductors, capacitors, and TFs. In the sub-THz band, the NF is dominated by the NF and gain of the first two or three stages due to low-gain characteristics, and single-ended or differential

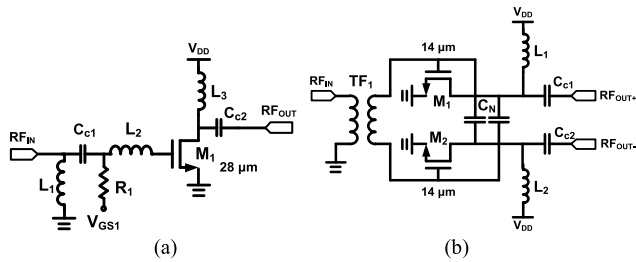


FIGURE 3. Schematics of single-stage CS amplifiers: (a) Single-ended and (b) differential.

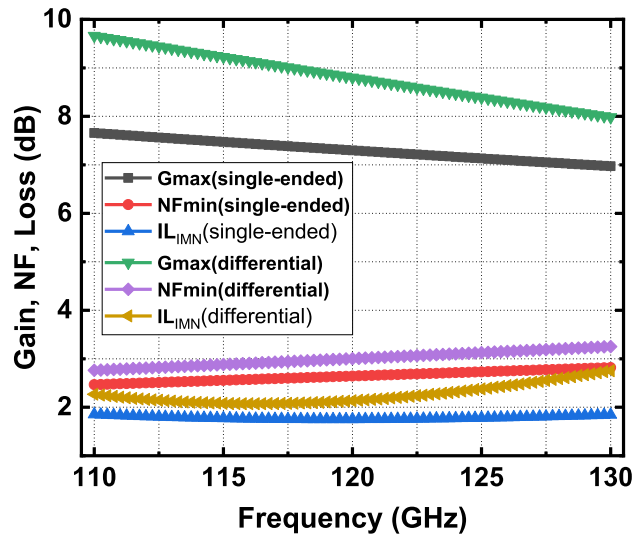


FIGURE 4. Maximum available gain, minimum NF, and insertion loss of input matching network for single-ended and differential single-stage CS amplifier.

CS amplifiers are widely used for better gain and noise performances [15], [16], [17], [18], [19], [20], [21]. Fig. 2 presents single-ended, differential, and hybrid architectures of the CS LNAs. Fig. 2(a) shows the 6-stage single-ended CS LNA. The IMN adopts an L-section of a series inductor and a shunt line inductor. The shunt line inductor  $L_1$  is also used for electrostatic discharge (ESD) protection. The ISMN uses a single shunt line inductor for conjugate matching, which contributes to low loss and small chip area. Fig. 2(b) depicts the 6-stage differential CS LNA. The single-stage single-ended and differential LNAs in Fig. 2 consume the same DC power under the same bias point. Also, all transistors in Fig. 2 use a unit finger width of  $1 \mu\text{m}$  for optimal NF and gain performance, and the total width in each stage is  $28 \mu\text{m}$  to ensure a fair comparison between the structures. The 6-stage differential CS LNA uses TFs for the IMN, ISMNs, and OMN and neutralization capacitors to cancel out Miller capacitances and enhance gain and stability performances. TFs are optimized to achieve low impedance matching loss and a compact design. The single-ended LNAs in Fig. 2 use the simultaneous noise and input matching (SNIM) technique for optimum NF [13].

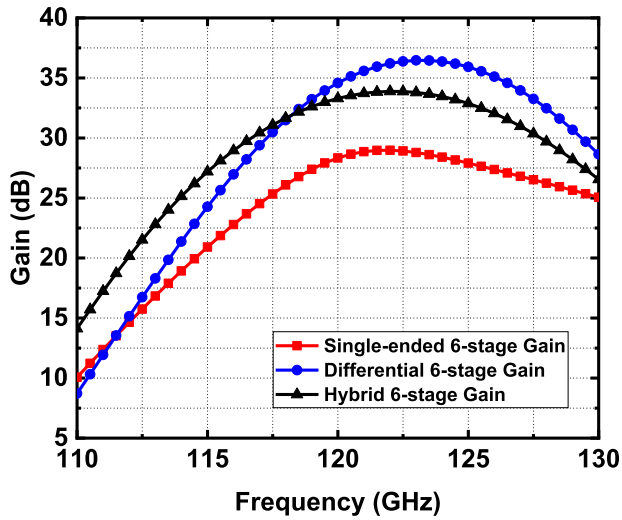
TABLE 1. Performance comparison of three types of 6-stage LNAs matching at 122.5 GHz.

Topology	Single-ended LNA	Differential LNA	Hybrid LNA
IL <sub>IMN</sub>	1.76 dB	2.24 dB	1.76 dB
$G_{max, Amp}$	7.2 dB	8.5 dB	7.2/8.5 dB
$NF_{min, Amp}$	2.69 dB	3.05 dB	2.69/3.05 dB
$NF^{\#}$	5.30 dB	6.15 dB	5.41 dB
Gain <sup>#</sup>	28.9 dB	36.4 dB	33.9 dB

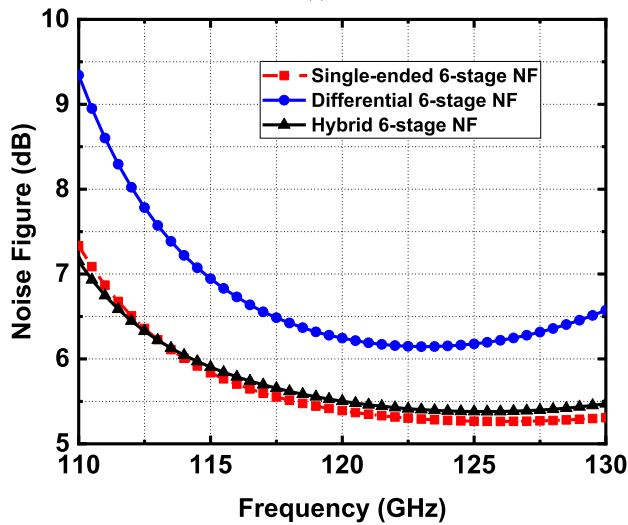
<sup>#</sup>Simulation result that all IMNs, ISMNs, and OMNs are matched at a single frequency of 122.5 GHz.

Fig. 3 illustrates the schematics of the single-ended and differential single-stage CS amplifiers. Fig. 4 shows the maximum available gain ( $G_{MAX}$ ), minimum NF ( $NF_{MIN}$ ), and insertion loss (IL) of the IMN for single-ended and differential single-stage CS amplifiers. The simulation results for  $G_{max}$  and  $NF_{min}$  were obtained without including the IMNs,  $L_1$  and  $L_2$  and  $TF_1$ . The insertion loss (IL) was obtained by simulating the IMN alone, without the transistors. Table 1 presents a performance comparison of the three types of 6-stage LNAs under the same power consumption, in which all IMNs, ISMNs, and OMNs are matched at a single frequency of 122.5 GHz.

The differential CS amplifier with neutralization capacitors provides better stability and a 1.3 dB higher gain, while  $NF_{MIN}$  and  $IL_{IMN}$  (IL of IMN) are 0.36 dB and 0.48 dB higher than those of the single-ended CS amplifier, respectively. The higher  $IL_{IMN}$  of the differential CS amplifier is mainly due to the high impedance transformation ratio of the TF, which requires a 1:2 turn ratio or offset between the primary and secondary inductors, resulting in a lower maximum available gain and consequently higher IL. This issue can be solved by using a much larger transistor size; however, the LNA with a huge transistor size suffers from high DC power dissipation. Assuming that all IMNs, ISMNs, and OMNs are matched with an ISMN loss of 1.5 dB and an OMN loss of 2.5 dB at a single frequency of 122.5 GHz, single-ended and differential CS LNAs can achieve gains of 28.9 dB and 36.4 dB and NFs of 5.30 dB and 6.15 dB, respectively. These results are achieved with impedance matching at a single frequency; therefore, the gain and NF can be degraded up to 10 dB and 1 dB, respectively, to widen the bandwidth. Fig. 2(c) shows the proposed 6-stage hybrid LNA. To simultaneously achieve lower NF and higher gain, the proposed LNA introduces a hybrid combination of 2-stage single-ended and 4-stage differential CS amplifiers. The first 2-stage single-ended CS amplifier provides low-noise characteristics, while the 4-stage differential CS amplifier provides high gain, resulting in low noise and high gain performance. As shown in Table 1, the proposed 6-stage hybrid CS LNA can achieve a gain of 35.9 dB and an NF of 5.35 dB for single-frequency impedance match. In the comparison in Table 1, NF of the hybrid LNA is 0.74 dB lower than that of the differential LNA and 0.11 dB higher than that of the single-ended LNA. Gain of the hybrid



(a)



(b)

FIGURE 5. Simulation result for 3-types of 6-stage LNAs matching at 122.5GHz (a)  $G_{MAX}$  and, gain, and (b)  $NF_{MIN}$  and NF.

TABLE 2. Parameter value for line inductors of single-ended 2-stage CS amplifier.

Topology	W/L# ( $\mu\text{m}$ )	Inductance (pH)	Q-factor <sup>#</sup>
L <sub>1</sub>	1.8/89.1	38.6	13.3
L <sub>2</sub>	1.8/28.2	11.0	5.7
L <sub>3</sub>	1.8/16.3	5.9	5.4
L <sub>4</sub>	1.8/52.9	21.6	17.6
L <sub>5</sub>	1.8/25.4	9.9	5.5
L <sub>6</sub>	1.8/16.3	5.9	5.7
L <sub>7</sub>	1.8/76.9	32.8	17.5

<sup>#</sup>W: width, L: length; <sup>†</sup>Q-factor: quality factor.

LNA is 5.0 dB higher than the single-ended LNA and 2.5 dB lower than the differential LNA.

The proposed 6-stage hybrid LNA in Fig. 2(c) is designed at a center frequency of 122.5 GHz. The unit finger width

TABLE 3. Parameter value for transformer of differential 4-stage CS amplifier.

Topology	L <sub>p</sub> (pH)	L <sub>s</sub> (pH)	Q <sub>p</sub>	Q <sub>s</sub>	Coupling factor
TF <sub>1</sub>	35.9	40.5	28.1	26.8	0.68
TF <sub>2</sub>	62.7	78.7	29.9	25.6	0.70
TF <sub>3</sub>	65.7	82.1	29.7	25.3	0.71
TF <sub>4</sub>	60.1	74.1	30.1	25.9	0.68
TF <sub>5</sub>	124.3	40.6	19.1	26.8	0.57

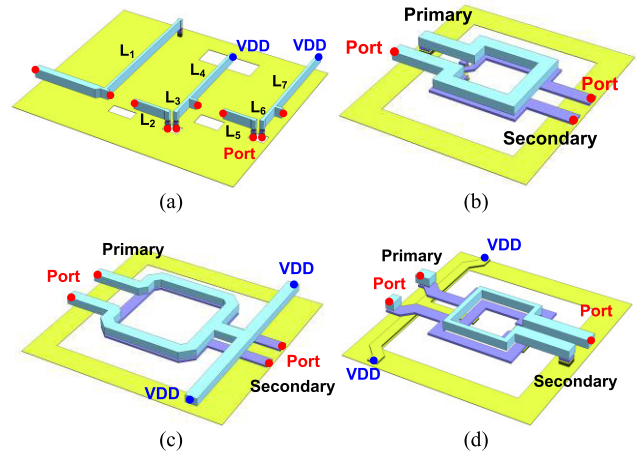


FIGURE 6. Layout of (a) line inductors, (b) input balun (TF<sub>1</sub>), (c) inter-stage transformer (TF<sub>2</sub>), and (d) output balun (TF<sub>3</sub>).

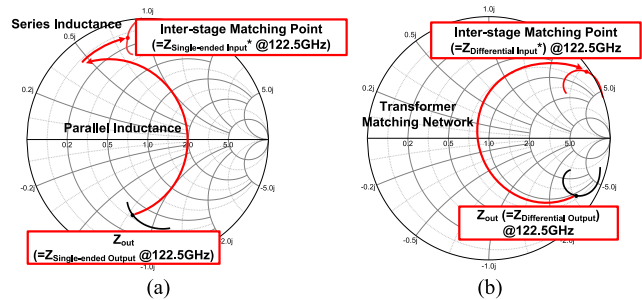


FIGURE 7. Inter-stage matching method of (a) single-ended 2-stage CS amplifier, and (b) differential 4-stage CS amplifier.

of M1–M10 is chosen as 1  $\mu\text{m}$  for optimum NF and gain performances. The number of fingers larger than 30 for a single transistor starts to saturate gain, NF, and 1-dB compression point (P1dB) performances while DC power dissipation is larger; therefore, the numbers of fingers are chosen to 28 for M1–M2 and 14 for M3–M10 for the optimum NF, gain and P1dB. All the transistors of the proposed LNA have a minimum gate length of 40 nm. The gate bias voltage of all transistors is set to 0.5 V to achieve a low NF and optimum gain under low DC power consumption while a gate bias voltage of 0.55 V gives the minimum NF with higher gain at the cost of much larger DC power dissipation.



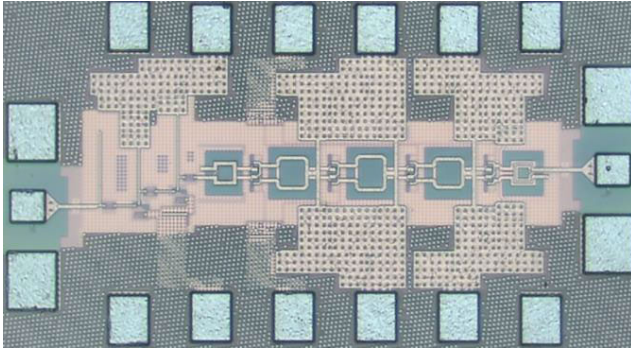


FIGURE 8. Chip microphotograph of the proposed LNA.

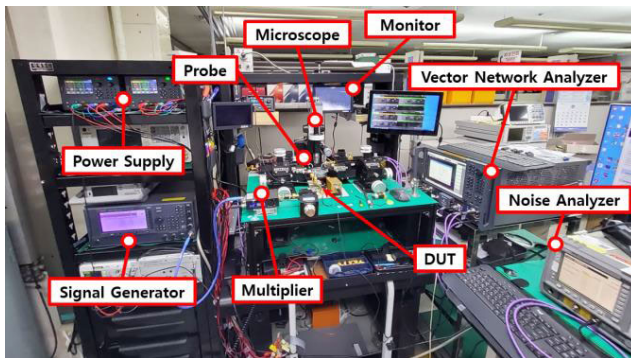


FIGURE 9. Measurement set-up for the proposed LNA.

### B. DESIGN OF THE PROPOSED HYBRID LNA

The LNA employs micro-strip line inductors in the first two stages and TFs at the last four stages for low loss and compact design. The layout of the line inductors and transformers is shown in Fig. 6. The micro-strip line inductors use an ultra-thick top metal with a line width of  $1.8 \mu\text{m}$  for low loss and compact design. The design parameters of line inductors and transformers in Fig. 2(c) are specified in Table 2 and Table 3. In Fig. 2(c), the TF1 with a physical primary-to-secondary winding turn ratio of 1:2 used for single-to-differential conversion and impedance transformation. The TF2, TF3 and TF4 use a turn ratio of 1:1 for inter-stage matching. The TF5 uses a turn ratio of 2:1 for impedance transformation and single-ended output. All the TFs consist of the top two metals with a magnetic coupling.

Fig. 7 (a) and (b) illustrate the inter-stage matching methods for single-ended and differential CS amplifiers, respectively. In the single-ended CS amplifier, as shown in Fig. 7 (a), the impedance of the inter-stage matching network is adjusted to the conjugate of the input impedance of the second stage using a parallel inductor and a series inductor. In the differential CS amplifier, the impedance is similarly shifted to the conjugate point by selecting the primary and secondary inductances, as well as the coupling coefficient of the transformer.

All the inductors, TFs, and interconnections are designed and optimized with electromagnetic simulation, and neutralization capacitors are designed with custom-designed metal-oxide-metal capacitors [22].

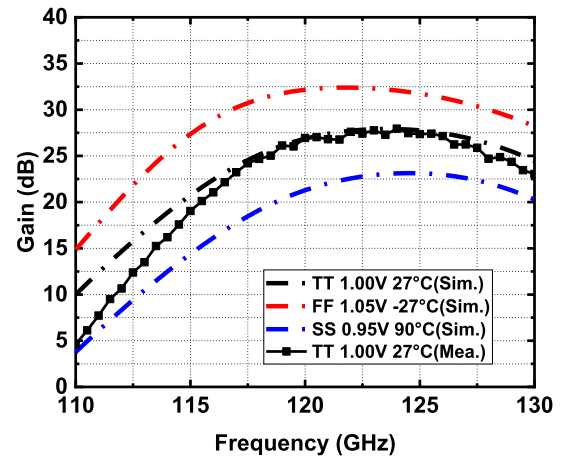


FIGURE 10. Simulated and measured gain of the proposed LNA.

To widen the bandwidth with low gain and NF degradations, the proposed LNA uses the stagger tuning technique [18] at two different frequencies, resulting in 8.1 dB lower gain and 0.35 dB higher NF than the hybrid LNA with impedance matching at a single frequency as shown in Table 1. The simulation results show that the proposed LNA has a power gain of 27.8 dB with a 3-dB bandwidth of 12.5 GHz and an NF of 5.7 dB.

### III. EXPERIMENTAL RESULTS

The proposed LNA was designed and fabricated using standard 1P10M 40-nm CMOS technology. Fig. 8 shows a microphotograph of the proposed LNA. The core area of the LNA, excluding the pads, is  $0.099 \text{ mm}^2$ . The LNA consumes 27.4 mW from a supply voltage of 1 V. Fig. 9 illustrates measurement set-ups for the S-parameter, P1dB and, NF. The S-parameters, P1dB, and NF were measured on-wafer using ground-signal-ground probes. For the S-parameter measurement, the Keysight N5222B vector network analyzer connected with frequency extension modules was used. To measure power handling capability, a signal generator was connected with a frequency multiplier, which feeds the input signal to the LNA through the step attenuator, and output power was measured through the power sensor and power meter. The on-wafer NF measurements were conducted with a Keysight N8973A NF analyzer, ELVA-1 D-band noise source with an isolator, sub-harmonic mixer, and signal generator. In the measurement results, all cable and probe losses were de-embedded.

Fig. 10, Fig. 11, and Fig. 12 depict the simulated and measured S-parameters of the LNA. The measured gain was 27.5 dB at 122.5 GHz, and the measured 3-dB bandwidth was 118–129 GHz. The measured 3-dB bandwidth is narrowed down by 2 GHz. This discrepancy between the measurement and simulation is mainly due to the imperfect modeling of the passive and active components. The measured input and output return losses were better than 10 dB for 111.5–132 GHz and 115.5–129 GHz, respectively.

TABLE 4. Performance comparison of the state-of-the-art F-/D-Band CMOS LNAs.

	[15]	[16]	[17]	[18]	[19]	[20]	This Work
Process	40-nm	40-nm	40-nm	40-nm	22-nm	40-nm	40-nm
Topology <sup>#</sup>	5 Diff. CG	5 Diff. CS	8 Diff. CS	8 SE CS	3 Cascode	2 SE CS	2 SE CS + 4 Diff. CS
Frequency (GHz)	153	127.7	153	120	92	152.2	120
Gain (dB)	20.9	19.7	20.9	20.6	18.2	17.9	27.5
3-dB BW (GHz)	31	24	31	6	31	11	11
NF <sub>MIN</sub> (dB)	6.2	7.9	13*	5.5	5.8	4.7	4.7
IP1dB (dBm)	-19.7	-24.8	-	-22.7	-22.8	-23.8	-29.5
OP1dB (dBm)	0.2	-6.1	-	-3.1	-5.6	-6.9	-3.0
P <sub>DC</sub> (mW)	49	17.8	94	45	16	13.7	27.4
Area (mm <sup>2</sup> )	0.082	0.070	0.27	0.075	0.148	0.193	0.099
FoM <sub>1</sub>	3.21	1.15	-	0.43	1.62	0.55	1.31
FoM <sub>2</sub>	8.49	3.36	-	5.38	7.73	9.62	11.80

<sup>#</sup> SE: single-ended, Diff.: differential; \*: simulation

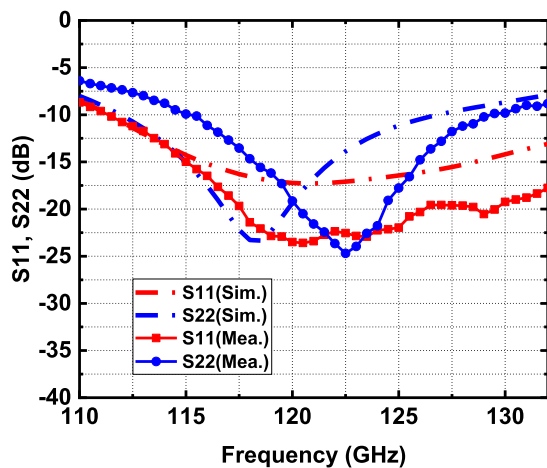


FIGURE 11. Simulated and measured return loss of the proposed LNA.

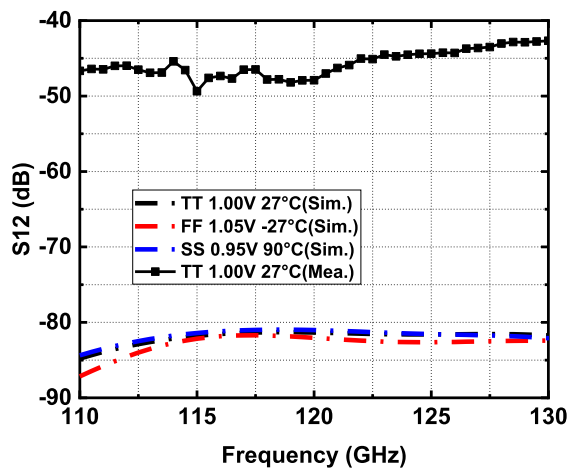


FIGURE 12. Simulated and measured S12 of the proposed LNA.

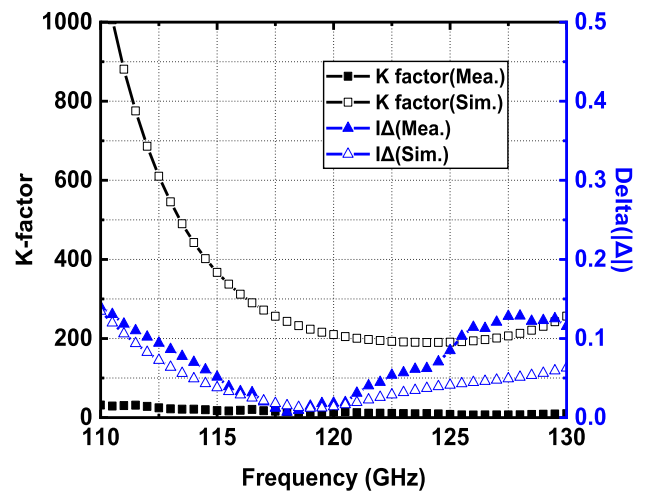


FIGURE 13. Simulated and measured K-factor and  $|\Delta|$  of the proposed LNA.

smaller than 0.2, respectively, indicating that the proposed LNA is unconditionally stable over the entire measured frequency range. This discrepancy between the measurement and simulation results of K-factor and  $|\Delta|$  is mainly due to higher measured S12 from substrate coupling. The measured minimum K-factor is 6.4 at 126 GHz.

Fig. 14 depicts the simulated and measured NF of the LNA. The measured NF was 5.5 dB at 122.5 GHz, and the measured minimum NF was 4.7 dB at 129 GHz. The NF discrepancy between the measurement and simulation is mainly due to imperfect modeling of the passive and active components. The simulated and measured output power versus input power at 120–127.5 GHz is shown in Fig. 15. The measured IP1dB was -29.5 dBm at 122.5 GHz. The simulated input third order intercept point was -22 dBm at 120 GHz.

Table 4 shows the performance comparison of several state-of-the-art F-/D-band CMOS LNAs. To compare the overall performance of the LNAs in Table 4, figure of merits

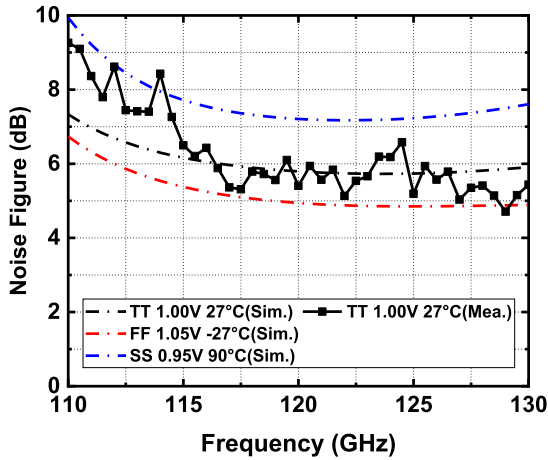


FIGURE 14. Simulated and measured NF of the proposed LNA.

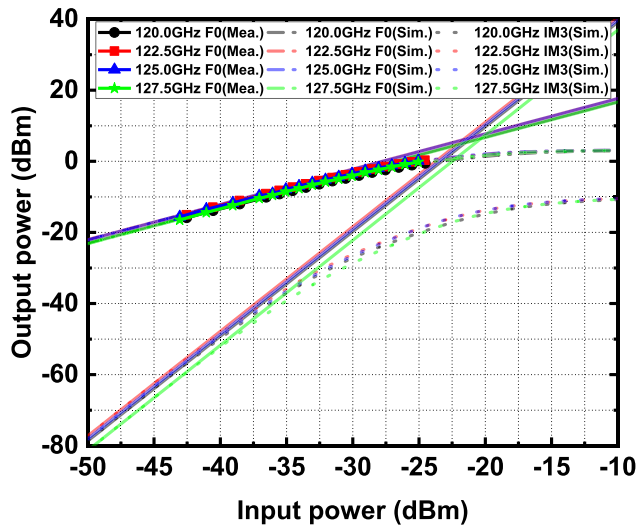


FIGURE 15. Simulated and measured IP1dB and simulated input third order intercept point of the proposed LNA.

(FoM<sub>1</sub>, FoM<sub>2</sub>) defined as

$$FoM_1 = \frac{Gain(linear) \cdot BW(GHz) \cdot IP1\ dB(linear)}{(NFmin(linear) - 1) \cdot P_{DC}(mW) \cdot area\ (mm^2)} \quad (1)$$

$$FoM_2 = \frac{Gain(linear) \cdot IP1\ dB(linear)}{(NFmin(linear) - 1) \cdot P_{DC}(mW)} * 10^3 \quad (2)$$

was employed.

The proposed LNA achieved a higher gain of 27.5 dB and a lower NF<sub>MIN</sub> of 4.7 dB than other works due to the hybrid combination of 2-stage single-ended and 4-stage differential CS amplifiers. A 3-dB bandwidth of 11 GHz is relatively smaller than in other works. However, a wider bandwidth can easily be achieved by using the stagger tuning technique [18].

The hybrid architecture of the proposed LNA provides a lower NF and higher gain with reasonable DC power consumption and P1dB. As a result, the proposed LNA achieved

a high FoM<sub>2</sub> compared with other works in Table 4, making it suitable for sub-THz radar systems.

#### IV. CONCLUSION

In this paper, we present a 6-stage 120 GHz hybrid LNA that was designed and fabricated using a 40 nm CMOS process. The proposed LNA utilizes a hybrid combination of 2-stage single-ended and 4-stage differential CS amplifiers to enhance the NF and gain performances. With this architecture, the proposed LNA achieves a low NF<sub>MIN</sub> of 4.7 dB and a high gain of 27.5 dB under a DC power consumption of 27.4 mW. These results contribute to a high FoM compared to other LNAs fabricated using a CMOS process.

#### ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

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