

우주망원경 이미지 센서를 위한 에너지 가변형 비교기 기반 11비트 극저온 SAR ADC

An 11-bit Cryo-CMOS SAR ADC Using Energy-Scalable Comparator for Image Sensors in Space Telescope

박창주*, 이재혁**, 이창엽**, 장동필*, 양민규***, 김정명***, 문성모*/**

(Changjoo Park, Jaehyuk Lee, Changyub Lee, Dongpil Chang, Minkyu Yang, Jeongmyeong Kim, and
Seong-Mo Moon[©])

요 약

본 논문은 우주 망원경의 이미지 센서를 위한 극저온 에너지 가변형 비교기를 제안한다. 제안하는 비교기는 기존 부동 인버터 증폭기의 고속 비교속도, 높은 전류 효율 (g_m/I_D), 그리고 공통모드제거 기능을 가지면서 동시에 전압제어발진기 기반 비교기의 에너지 가변성을 지닌다. 제안하는 비교기는 65 nm 공정으로 11-bit 극저온-CMOS SAR ADC에 구현되었으며, 해당 ADC는 5 MS/s의 샘플링 속도에서 65.2 dB의 SNDR과 174 dB의 Schreier FoM (FoM_S)을 지닌다.

Abstract

This paper presents a cryogenic energy-scalable comparator designed for image sensors in space telescopes. The proposed comparator maintains the fast comparison speed, high current efficiency (g_m/I_D), and intrinsic common-mode rejection ability of conventional floating inverter amplifier (FIA), while incorporating the energy scalability of voltage-controlled oscillator (VCO)-based comparators. The proposed comparator is implemented in an 11-bit cryo-CMOS SAR ADC, which is designed in 65 nm CMOS, and it achieves an SNDR of 65.2 dB and a Schreier FoM (FoM_S) of 174 dB at a sampling rate of 5 MS/s.

Keywords: ADC, Comparator, Cryo-CMOS, Energy-Scalability, Floating Inverter-Amplifier

※ Acknowledgment

* 비회원, 한국전자통신연구원 (ETRI) 위성탑재체 연구실 (Satellite Payload Research Section, ETRI)

** 비회원, UST 정보통신공학과 (Information and Communication Engineering, UST)

*** 비회원, KAIST 전기전자공학부 (Electrical and Electronic Engineering, KAIST)

© Corresponding Author (E-mail: smmoon@etri.re.kr)

※This work was supported by a grant from the Institute of Information Communications Technology Planning Evaluation (IITP), funded by the Korean government (MSIT) (No. 2018-0-00190, Development of Core Technology for Satellite Payload).

I. Introduction

Over the past decades, human beings have actively explored regions beyond the Earth, seeking to understand the broader structure and evolution of the universe. To support such endeavors, space telescopes (Fig. 1), such as the Hubble or the James Webb Space Telescope, have been deployed into the cryogenic and vacuum conditions of space, and they have provided invaluable data on galactic structures, cosmic expansion, and other fundamental astrophysical phenomena [1], [2].

CMOS image sensors employed in space telescopes contains 10–12 bit SAR ADCs with sampling rates ranging from tens of kS/s to a few MS/s [2]–[5]. There are two primary challenges in designing the SAR ADCs for space telescopes: first, ensuring sufficient speed under cryogenic conditions [6], where the device threshold voltage significantly increases; and second, achieving high energy efficiency, since the only energy source for the ASIC is solar energy.

A comparator is one of the most critical analog blocks for high-resolution SAR ADCs, since it requires low thermal noise. Comparator assisted with a floating inverter amplifier (FIA) [7], as shown in Fig. 2, uses the current-reuse property of inverter amplifiers, enabling theoretically up to 2.5 times better noise-energy efficiency than conventional

comparators using common-source amplifiers [7]. Additionally, by utilizing a floating reservoir capacitor, the FIA can establish an isolated power domain during amplification, which allows stable common-mode behavior without requiring a dedicated common-mode feedback (CMFB) circuit. This helps stabilize the offset, noise, and speed performance of the following latch stage. Despite these advantages, the FIA-based comparator consumes nearly constant energy regardless of the input difference. In applications such as SAR ADCs, where the input differences of the comparator vary widely, this leads to redundant energy consumption under large input conditions, thereby limiting the energy efficiency of the ADC.

To address the lack of energy scalability in FIA-based comparators, voltage-controlled oscillator (VCO)-based comparators, as shown in Fig. 2, have been widely adopted [8]. The VCO-based comparators convert the input voltage into the phase domain and then perform comparison based on the input phase difference. A large input difference results in a large phase difference, allowing for rapid comparison speed and an exponential reduction in both oscillation cycles and energy consumption.

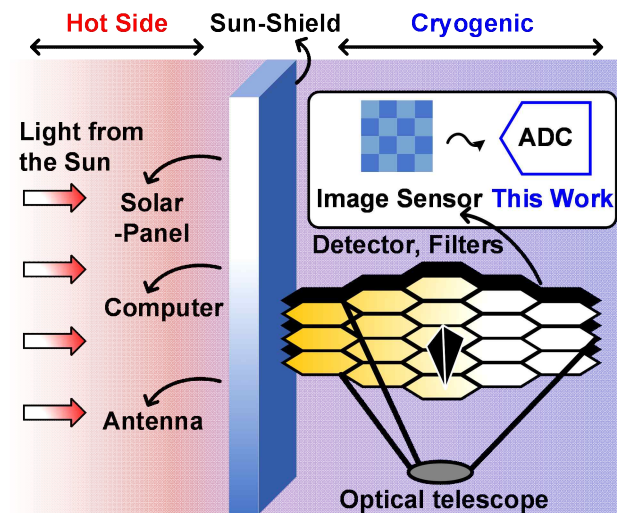


그림 1. 우주 망원경의 동작 환경 및 구성도
Fig. 1. Block diagram of space telescope and its operating environments.

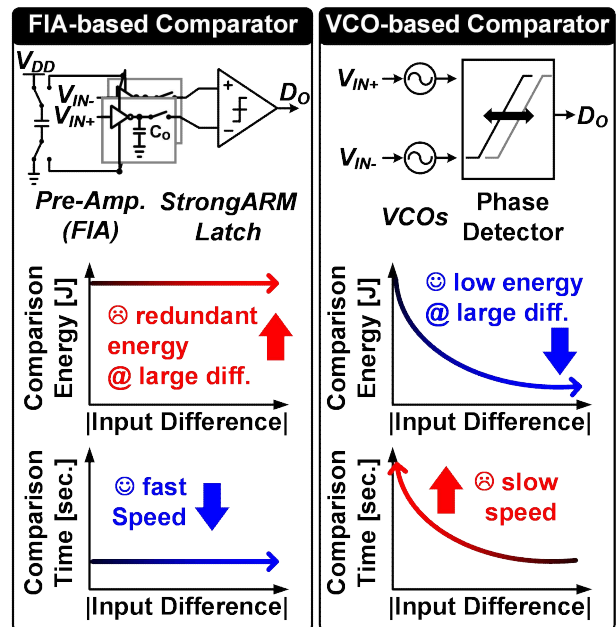


그림 2. FIA기반 비교기와 VCO기반 비교기의 비교도
Fig. 2. Comparison of FIA-based and VCO-based comparators.

Conversely, for small input differences, the phase difference becomes small, which automatically increases the number of oscillation cycles to achieve the necessary noise performance by consuming more energy. This exponential energy adaptation based on input difference allows VCO-based comparators to enhance energy efficiency in SAR ADCs. However, VCO-based comparator-assisted ADCs typically operate at low speeds of under a few MS/s [8], since the comparison time also exponentially scales as it is proportional to the change in the number of oscillation cycles.

This paper presents an FIA-based comparator that maintains both the high energy efficiency and fast comparison speed of the FIA, while incorporating the energy scalability of VCO-based comparators. The proposed comparator is implemented in an 11-bit 5 MS/s cryo-CMOS SAR ADC, which operates at a cryogenic temperature of 50 K.

This paper is organized as follows: Section II reviews the schematic and operation of the FIA-based comparator, while Section III describes the schematic and operation of the proposed

energy-scalable FIA-based comparator. Section IV demonstrates the implementation of an 11-bit cryo-CMOS SAR ADC using the proposed comparator with pre-layout simulation results, and the final section draws a conclusion.

II. FIA-based Comparator

Fig. 3(a) shows the block diagram of a conventional FIA-based comparator with a schematic of its pre-amplifier. During the reset phase, the reservoir capacitor (C_{RES}) is charged, while the output nodes of the inverter amplifiers are reset to a certain voltage (V_{CM}). During the pre-amplification phase, the FIA performs pre-amplification using the pre-charged charge from the reservoir capacitor. After a certain delay following pre-amplification, the second-stage StrongARM latch (Fig. 3(b)) is triggered to complete the quantization, as shown in Fig. 4(a). The FIA-based comparator features advanced energy efficiency using the current-reuse technique and

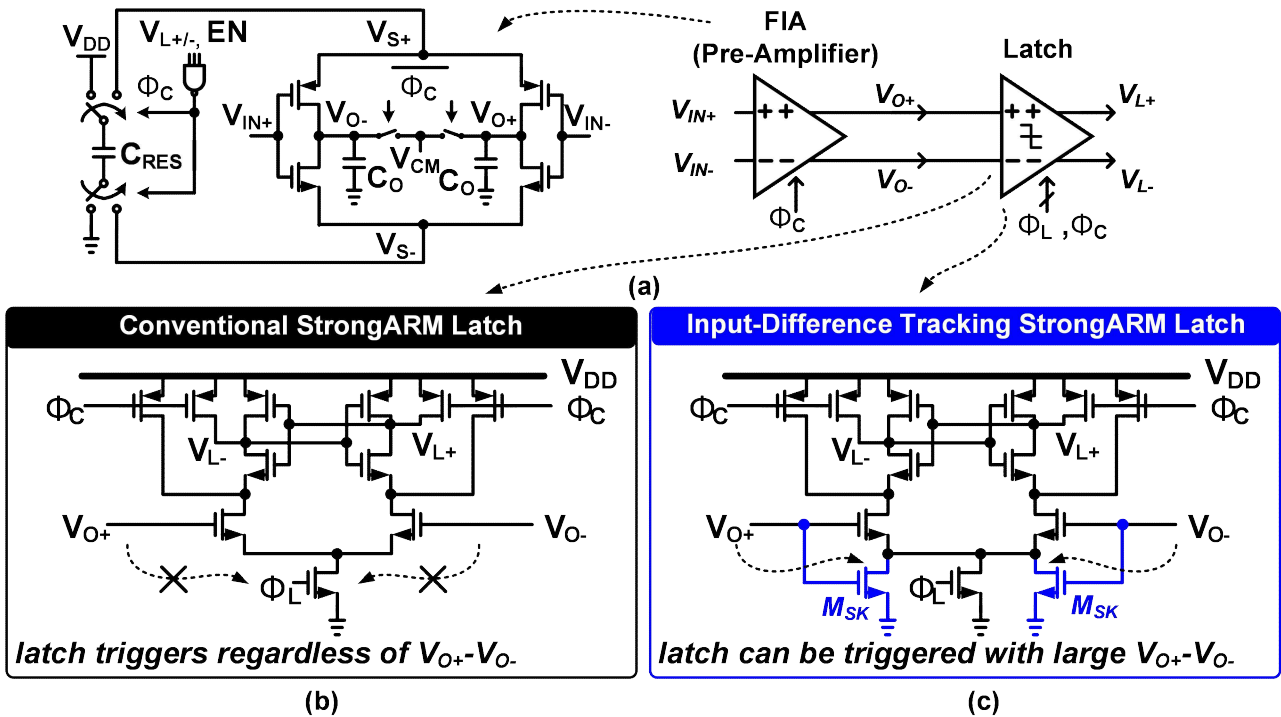


그림 3. (a) FIA기반 comparator의 구성도 및 pre-amplifier의 회로도, (b) 기존 StrongARM latch와 (c) 제안하는 입력차이 추적 StrongARM latch의 회로도

Fig. 3. (a) Block diagram of the FIA-based comparator with the schemaitc of its pre-amplifier, and schematics of (b) conventional StrongARM latch and (c) proposed input-difference tracking StrongARM latch.

possesses a certain degree of common-mode rejection, since the NMOS and PMOS in the inverter amplifiers share the same DC currents. However, the conventional FIA consumes nearly constant energy regardless of the input difference (Fig. 4(b)), since the latch is always triggered after a fixed delay following the pre-amplifier's trigger.

III. Proposed Two-Stage Comparator

Fig. 3(c) shows the schematic of the proposed input-difference tracking StrongARM latch. In the conventional FIA-based comparator, the second-stage StrongARM latch is always triggered after a fixed delay following the enabling of the pre-amplifier, as shown in Fig. 4(a). It consumes almost constant energy regardless of the input difference, as shown in Fig. 4(b). The proposed comparator utilizes the conventional FIA as its pre-amplifier, borrowing its fast comparison speed, high gain, and advanced gm/ID. Unlike the traditional StrongARM latch, the

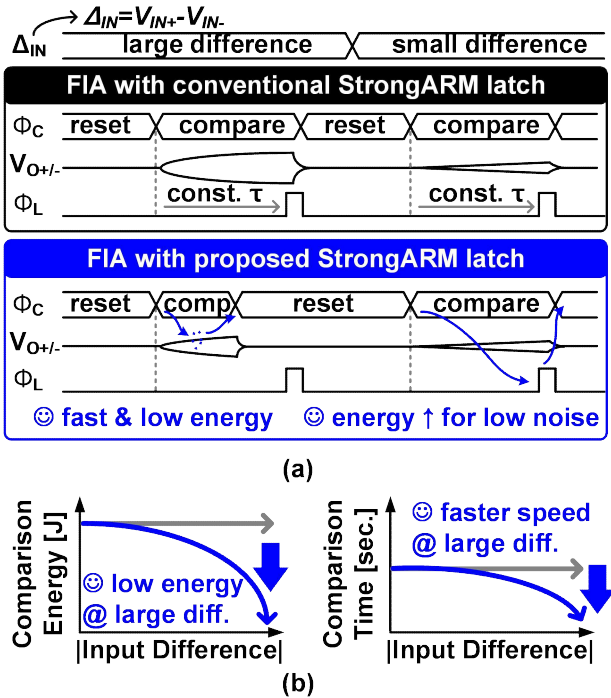


그림 4. (a) 기존 FIA-based와 제안하는 비교기의 타이밍 비교도와 (b) 에너지 소모량 및 비교 속도의 비교도

Fig. 4. (a) comparison of timing diagrams of the conventional and proposed FIA-based comparators and (b) their energy consumptions and comparison time.

delay time for triggering the second-stage latch is adjusted by reflecting the output difference of the pre-amplifier. To realize this, the sinking transistor (MSK in Fig. 3(c)) tracks the pre-amplifier's outputs to trigger the latch earlier when the input difference is large, as shown in Fig. 4(a). Conversely, for small input differences, the gate voltages of MSK are not high enough to be triggered; therefore, quantization is completed after a fixed delay, as in the conventional FIA-based comparator. The new FIA-based comparator allows fast latching for large input differences, eliminating redundant energy consumption, while maintaining higher energy consumption for small input differences to preserve low-noise performance. In addition, the proposed design features faster quantization speed for large input differences than the conventional one, since it quenches operation earlier.

Fig. 5 illustrates the simulation results of the energy consumption and comparison time of two FIA-based comparators at room and cryogenic temperatures. The proposed design performs faster and reduces energy consumption at large input differences by 49.6 % for 100 mV input differences at

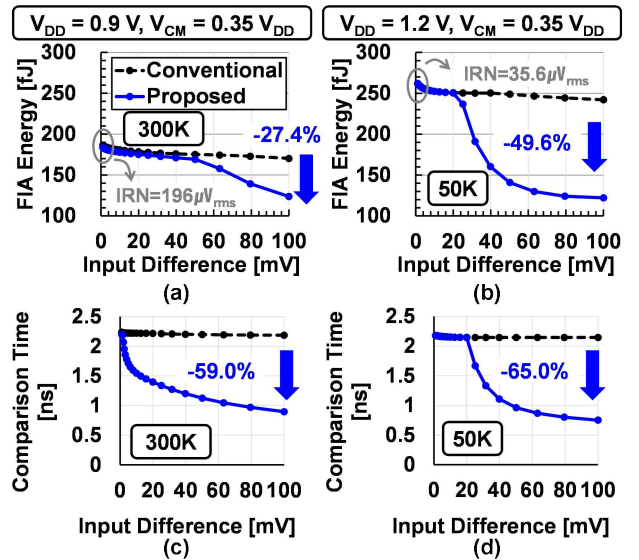


그림 5. 시뮬레이션 기반 pre-amplifier의 (a) 상온 및 (b) 극저온에서의 에너지 소모량과 (c) 상온 및 (d) 극저온에서의 비교 속도

Fig. 5. Simulated energy consumption in pre-amplifier at (a) room and (b) cryogenic temperatures, and comparison time at (c) room and (d) cryogenic temperatures.

cryogenic temperature, as shown in Fig. 4(b). When the input difference is small, the energy consumption is the same as that of the conventional FIA-based comparator, maintaining the same input-referred noise (IRN) of 196 μV_{rms} and 35.6 μV_{rms} at room and cryogenic temperatures, respectively. It also enables faster comparison speed, offering additional timing margin in asynchronous SAR ADCs.

IV. Cryo-CMOS SAR ADC

Fig. 6 shows the block diagram of an 11-bit cryo-CMOS SAR ADC using the proposed energy-scalable FIA-based comparator, implemented in 65-nm CMOS. The capacitive digital-to-analog converter (C-DAC) is realized with metal-oxide-metal (MoM) capacitors using split switching [9]. The ADC operates asynchronously through a timing controller, enabling operation with a master clock speed equal to the sampling rate, which allows the ADC to operate at slow speeds of a few kS/s, where it is sensitive to leakage current.

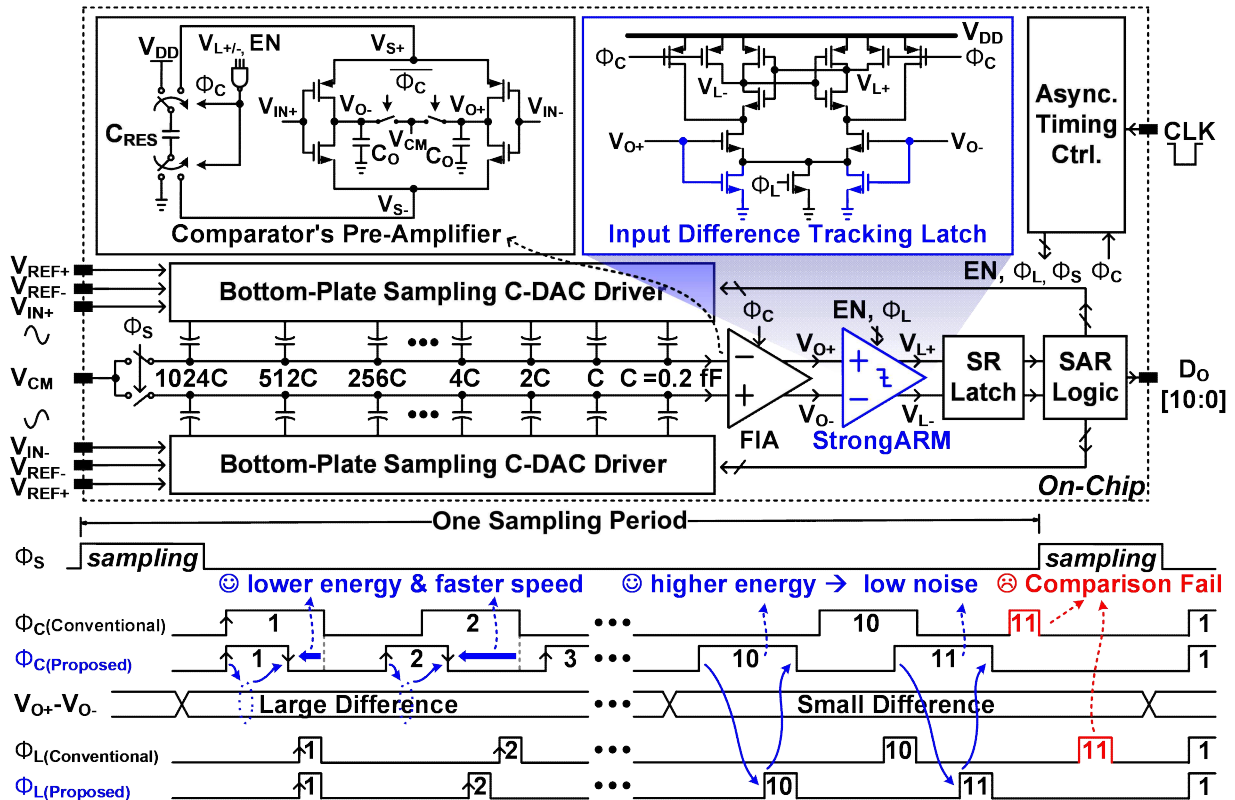


그림 6. 11-bit 극저온-CMOS SAR ADC의 구성도와 타이밍도
Fig. 6. Block and timing diagram of 11-bit Cryo-CMOS SAR ADC.

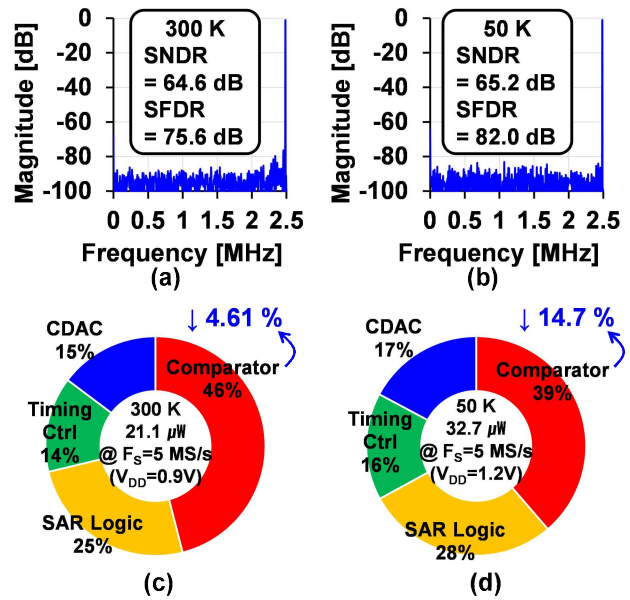


그림 7. (a) 상온 및 (b) 50 K 온도에서의 시뮬레이션 기반 ADC의 출력 스펙트럼과 (c) 상온 및 (d) 50 K 온도에서의 전력 소모 분포도

Fig. 7. Simulation results of the ADC's output spectra at (a) room and (b) 50 K temperatures, and its power breakdown at (c) room and (d) 50 K.

Fig. 7(a) and (b) show the ADC output spectra at 5 MS/s for room and 50 K cryogenic temperatures with near-Nyquist input frequencies. The

표 1. 제안하는 SAR ADC와 기존 방식의 성능 비교표
Table 1. Performance comparison of prior and proposed SAR ADCs.

	This Work**		[3]	[4]	[5]
Technology Node [nm]	65		65	350	-
Temp. [K]	300	50	300	300	300
Sampling Rate (Fs) [MS/s]	5		80	0.03	1
V _{DD} [V]	0.9	1.2	1.2	3.3	3
SNDR [dB]	64.6	65.2	70.3	68.6	71.6
SFDR [dB]	75.6	82.0	80.3	80.1	91
Power[mW]	0.021	0.033	13.8	24	2.3
FoMs* [dB]	175	174	165	127	155

* FoMs = SNDR (dB) + 10log₁₀(Fs/(2xPower))

** Pre-layout simulation

SNDR/SFDR are 64.6 dB/75.6 dB at 300 K and 65.2 dB/82.0 dB at 50 K, respectively. Fig. 7(c) and (d) show the ADC power breakdowns at room and cryogenic conditions, respectively. The energy in the comparator is reduced by 14.7 % at 50 K, compared to that of the conventional FIA-based comparator.

Table I summarizes a performance comparison between the proposed ADC and prior art. The proposed ADC consumes 0.021 mW (V_{DD} = 0.9 V) at sampling rate of 5 MS/s and achieves 175 dB FoMs at room temperature. It consumes 0.033 mW (V_{DD} = 1.2 V) at the same FS, achieving 174 dB FoMs at 50 K.

V. Conclusion

This paper proposes an energy-scalable FIA-based comparator that maintains the fast comparison speed and high g_m/I_D properties of the conventional FIA-based comparator, while simultaneously incorporating the energy-scalability feature of the VCO-based comparator. It is implemented in a 65-nm CMOS process for an 11-bit cryo-CMOS SAR ADC and features robust performance under both room and cryogenic conditions.

REFERENCES

- [1] K. Jason, "Scientific discovery with the James Webb space telescope." *Contemporary Physics* 59.3, pp. 251-290, 2018.
- [2] K. Martin, "Designing ADCs for the James Webb Space Telescope", *Aerospace & Defense Technology Magazine*, vol. 7, No. 5, Aug. 2022.
- [3] Z. Li et al., "An 80 MS/s 70.8 dB-SNDR Radiation-Tolerant Semi-Time-Interleaved Pipelined-SAR ADC for Space Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, Jan. 2025.
- [4] C. Tahar et al., "TID-Tolerant StrongARM Comparator and Sampling Network for Satellite Application High-Voltage ADCs," *2024 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Hiroshima, Japan, 2024.
- [5] "ADC128S102QML-SP," <https://www.ti.com/>, accessed on Apr. 20th, 2025.
- [6] "Cryogenic Data Acquisition ASIC", <https://science.nasa.gov/>, accessed on Apr. 20th, 2025.
- [7] X. Tang et al., "An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, April 2020.
- [8] K. Yoshioka and H. Ishikuro, "A 13b SAR ADC with eye-opening VCO based comparator," *40th European Solid State Circuits Conference (ESSCIRC)*, pp. 411-414, 2014.
- [9] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739-747, April 2007.

저 자 소 개



박창주 (비회원)
2019년 인하대학교 전자공학과
학사 졸업.
2021년 GIST 전기전자컴퓨터
공학부 석사 졸업.
2025년 KAIST 전기전자공학부
박사 졸업.

2025년-현재 한국전자통신연구원(ETRI)
위성탐재체 연구실 박사후연구원.
<주관심분야 : 아날로그 및 혼성신호 반도체 회
로설계>



이창엽 (비회원)
2019년 육군사관학교 전자공학과
학사 졸업.
2025년-현재 UST정보통신공학과
석사 재학.
<주관심분야 : RF 회로설계>



양민규 (비회원)
2020년 한양대학교 전자공학과
학사 졸업.
2022년 KAIST 전기전자공학부
석사 졸업.
2022년-현재 KAIST 전기전자
박사 재학.

<주관심분야 : 아날로그 및 혼성신호 반도체 회
로설계>



문성모 (비회원)
2003년 서울시립대학교
전자공학과 학사 졸업.
2005년 서울시립대학교
전자공학과 석사 졸업.
2005년-2008년 Analog Device
선임연구원.

2010년 서울시립대학교 전자공학과 박사 졸업.
2010년-현재 한국전자통신연구원(ETRI)
위성탐재체 연구실 기술총괄
2025년-현재 UST 정보통신공학과 교수
<주관심분야 : microwave, mmWave RF 반도체
회로설계>



이재혁 (비회원)
2024년 국립한밭대학교 정보통신
공학과 학사 졸업.
2025년-현재 UST정보통신공학과
석사 재학.
<주관심분야 : 신호처리, 제어, 통
신 및 RF 시스템>



장동필 (비회원)
1992년 충남대학교 전자공학과
학사 졸업.
1994년 충남대학교 전자공학과
석사 졸업.
2007년 충남대학교 전자공학과
박사 졸업.

1994년-현재 한국전자통신연구원(ETRI)
위성탐재체 연구실 실장
<주관심분야 : microwave, mmWave RF 반도체
회로설계>



김정명 (비회원)
2020년 아주대학교 전자공학과
학사 졸업.
2022년 KAIST 전기전자공학부
석사 졸업.
2022년-현재 KAIST 전기전자
박사 재학.

<주관심분야 : 전력 반도체 회로 설계>