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3-dB bandwidth enhanced InGaAs PIN photodiode by inductive CPW electrode for datacenter applications

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Abstract: We report on a 3-dB bandwidth extension technique achieved through a coplanar waveguide (CPW) electrode design that imposes inductive gains in a backside-lens-integrated InGaAs positive-intrinsic-negative (PIN) photodiode. The inductive CPW electrodes are analyzed in detail using an equivalent circuit model in which the transit time of the photo-generated carriers has been included. The transit times for the electrons and holes have been analyzed numerically. By including the transit time effect in the equivalent circuit model, the extracted RLC parameters show a good consistency with measured frequency response data. As a result, the 3-dB bandwidth has been extended from 48 GHz to over 67 GHz at a -2.5 V bias voltage simply by reconfiguring the CPW electrode design.

1. Introduction

The explosive growth in artificial intelligence and cloud computing services has been supported by massive high-capacity datacenter developments. In the advanced datacenters, optical transceivers are extensively adopted to cope with the surging data traffic. Single-lane transmission speed of transceivers for next-generation 800-Gbps and 1.6-Tbps has now increased to 224 Gbps [1]. For a transmission distance within 2 km, a PAM4 modulation format is mainly deployed. Therefore, it is desirable for optical transmitters and receivers to have a 3-dB bandwidth of 56 GHz or higher, corresponding to the Nyquist frequency of 112-Gbaud PAM4 transmission [2]. As for the optical receivers, surface-illuminated positive-intrinsic-negative (PIN) photodiodes are typically employed. These exhibit a trade-off between bandwidth and responsivity, which is determined by the thickness of the intrinsic InGaAs absorption layer. To achieve a higher bandwidth, a thinner absorption layer is preferred because the 3-dB bandwidth of photodiodes is determined not only by the RC time constant but also the transit time constant. Transit time is the duration required for an electron and hole pair generated via a photon absorption in the intrinsic layer to travel to the doped regions [3]. Therefore, to achieve both high responsivity and bandwidth simultaneously, it is common to partially p-dope the InGaAs absorption layer to reduce the travel distance of heavier holes, thereby compensating for the longer transit time of the holes relative to the electrons. In addition, a non-absorbing intrinsic or slightly n-doped layer is placed underneath as an additional intrinsic layer to maintain low capacitance. Capacitance is also related to the photodiode dimensions. As the dimensions of the photodiode become smaller, the corresponding capacitance decreases, and the 3-dB bandwidth improves [4]. Meanwhile, the 3-dB bandwidth of the photodiode is also affected by the parasitic capacitance and the series resistance. Since parasitic capacitance remains constant regardless of the photodiode dimensions, and the series resistance increases with smaller mesa diameters, both serve as limiting factors in improving the bandwidth through photodiode dimension scaling [5]. The parasitic capacitance of the electrodes is only about 10 to 20 fF. However, this actually takes up a large portion of the total

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capacitance that is typically required to be below 60 fF for operation above 50 GHz. The smaller the photodiode dimensions, the lower the alignment tolerance, which makes the light coupling to the photodiode more difficult. This challenge can be solved by employing a parabolic-shaped lens integrated into the backside of the substrate. The integrated backside-lens enables a large receiving window of 40 µm with a tolerance of -1 dB at a photodiode diameter of 10 µm [6]. This broad alignment tolerance is an unmatched advantage over waveguide-type photodiodes, which are a preferred photodiode structure for high-bandwidth operation due to their short transit time [7,8]. Considering the fabrication alignment tolerance between the frontside diode and the backside lens, the minimum mesa diameter of a typical backside-lens-integrated photodiode is 8 to 10 µm. These dimensional scaling limitations constrain the bandwidth improvement of the lens-integrated photodiodes. One alternative approach to extending the 3-dB bandwidth is to utilize the inductive peaking phenomenon in which the frequency response of the photodiode rises at an LC resonant frequency. This approach originated from CMOS amplifier design [9,10]. Raising the frequency response through the LC resonance can compensate for losses in the high-frequency range and extend the 3-dB bandwidth of the photodiode [11,12]. These inductive characteristics are implemented through a high-impedance coplanar waveguide (CPW) electrode configuration defined by parameters such as the signal electrode width, the spacing between the signal and ground electrodes, and the signal electrode length. Modified uni-travelling carrier (MUTC) InGaAs photodiodes have utilized the inductive peaking characteristics to operate above 100 GHz [13,14]. In addition, the inductive peaking has been applied to the packaging of the electro-absorption modulator lasers (EMLs), which enhances the bandwidth by optimizing wire bonding LC resonance characteristics [15].

In this paper, we present the 3-dB bandwidth enhancement results of the backside-lens-integrated surface-illuminated photodiodes using the inductive electrode designs. We have fabricated backside-lens-integrated InGaAs photodiodes with six different CPW electrode configurations and measured the 3-dB extension characteristics according to the electrode impedances. The diameter of the photodiode was set to 10 µm, showing a responsivity of 0.66 A/W at the 1.31 µm wavelength. The inductive signal electrodes have been analyzed in detail using an equivalent circuit model. The equivalent circuit includes the transit time region, which is determined by the carrier transit time constant. The carrier transit time has been calculated using commercial TCAD software. By fitting the R, L, and C parameters of the equivalent circuit with the measured RF return loss (S11) of the photodiodes on Smith charts, the precise values of the RLC parameters have been extracted. This has been validated by demonstrating good agreement between the simulated frequency response and the measured O/E response data. While the reference photodiode showed a 3-dB bandwidth of 48 GHz, the inductance-imposed photodiodes achieved a 3-dB bandwidth exceeding 67 GHz, which is sufficient to transmit PAM4 signals at data rates above 224 Gb/s for datacenter applications.

2. Device structure and fabrication

Figure 1(a) shows the schematic cross-section of the backside-lens-integrated InGaAs photodiode. The p-contact epitaxial structure has a 50-nm-thick p-InGaAs top contact layer with a Zn-doping concentration of $2 \times 10^{19} \text{cm}^{-3}$ and a 70-nm-thick p-InGaAsP electron-diffusion barrier layer. The p-absorption layer placed below consists of two p-InGaAs absorption layers with thicknesses of 110 nm and Zn-doping concentrations of $3 \times 10^{18} \text{cm}^{-3}$ and $9 \times 10^{17} \text{cm}^{-3}$, respectively. Beneath this region, a 380-nm-thick undoped InGaAs absorption layer and a 200-nm-thick slightly Si-doped InP layer constitute the intrinsic region. A 700-nm-thick InP layer with a Si-doping concentration of $2 \times 10^{18} \text{cm}^{-3}$ is placed at the bottom as the n-contact region. An anode metal layer on top of the p-InGaAs top contact layer is connected to the CPW electrode on the substrate through an air-bridge electrode. This air-bridge structure surrounded by air with a relative dielectric constant of 1 constitutes a high-impedance configuration and accounts for a large

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portion of the series inductance. In addition, the anode metal layer at the top of the diode acts as a reflecting mirror for the bottom-illuminated incident light onto the PIN diode, allowing it to pass through the absorption layer twice, resulting in increased responsivity. Approximately 30% of the responsivity is estimated to be attributable to light reflected from the anode metal electrode. On the backside of the InP substrate, the parabolic convex lens structure is integrated.

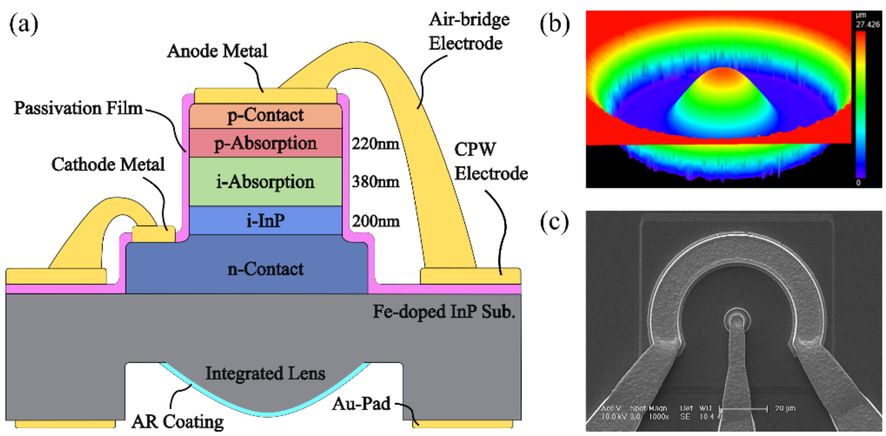

Fig. 1. (a) Schematic cross-sectional view of the backside-lens-integrated InGaAs photodiode. (b) 3D image of the integrated backside lens. (c) SEM image of the fabricated photodiode with the reference electrodes.

The diameter of the lens is 100 µm, and the height of the lens is 25 µm, recessed by 2 µm relative to the substrate plane to avoid collision. The radius of curvature is larger than 50 µm. An anti-reflection layer is coated onto the lens to reduce Fresnel reflection. Without the coating, more than 35% of the incident light is reflected at the lens interface. Figure 1(b) depicts a three-dimensional (3D) image of the fabricated lens. Figure 1(c) shows a scanning electron microscope (SEM) image of the photodiode with our reference electrode design.

Photodiodes were fabricated using a 2-inch semi-insulating InP wafer with the PIN epitaxy structure. The epitaxy structure was grown by metal-organic chemical vapor deposition (MOCVD). The fabrication process started with the formation of a circular Ti/Pt/Au ohmic contact electrode on the p-InGaAs top contact layer. It was followed by the formation of a cylindrical PIN diode mesa structure. This mesa structure was fabricated by wet-chemical etching down to the middle of the n-InP contact layer. A second mesa structure was formed by wet-etching again down to the bottom of the n-InP layer. A 300-nm-thick SiN layer was deposited as a passivation layer by plasma-enhanced chemical vapor deposition (PECVD). The passivation layer was partially removed by a dry-etching process to expose the semi-ring-shaped n-InP bottom contact layer and the circular p-metal top contact layer, respectively. A Ge/Au/Ni/Au ohmic contact electrode was formed on the opened n-InP semi-ring area. Thereafter, a gold plating process was applied to form a 2.5-µm-thick CPW transmission line and ground-signal-ground (GSG) pads. Through this plating process, the air-bridge electrodes were formed, connecting the p- and n-ohmic contact electrodes to the CPW electrode. After completing electrode formation, lapping and polishing processes were applied to the backside of the wafer to reduce the thickness to 150 µm and achieve a mirror-like surface. Finally, a recessed InP parabolic convex lens is formed on the backside of the wafer through an InP dry etching process using an ICP-RIE apparatus and a thermally reflowed photoresist mask pattern. This mask pattern consists of two parts formed through separate photolithography processes. One part is for the formation of parabolic convex lens and

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the other part is for the recessing of the parabolic convex lens below the substrate plane. The fabricated photodiode exhibited a responsivity of 0.66 A/W at a -2.5 V bias.

3. Inductive electrode design and device modeling

Figure 2 shows the top-view images of the fabricated photodiodes. Six CPW electrode designs are presented with the same PIN diode diameter of 10 µm and 125 µm-pitch-GSG contact pads of 60 µm diameter. Figure 2(a) is our previous reference electrode design where the width of the CPW electrode and the spacing between the signal and ground electrodes are gradually reduced for a smooth impedance transition. The air-bridge signal electrode has a taper length of 25 µm and a 13 µm length of straight line with a width of 5 µm. All six electrodes have the same total air-bridge length of 38 µm, and Fig. 2(a), (b), and (c) have a signal electrode length of 75 µm connecting the contact pad and the air-bridge electrode. Figure 2(b) shows that the signal electrode has a constant width of 20 µm and the spacing to the ground electrodes is kept at 105 µm. The wider spacing is intended to impose a higher impedance characteristic. Figure 2(c) and (d) have signal electrode widths of 10 µm and 5 µm, respectively, which induce higher inductances by reducing the signal electrode width relative to Fig. 2(b). Figure 2(e) and (f) have a signal electrode width of 5 µm, the same as in Fig. 2(d), and adopt a meandered signal electrode structure with a total signal electrode length of 313 µm and 513 µm, respectively, to achieve higher inductance relative to Fig. 2(d).

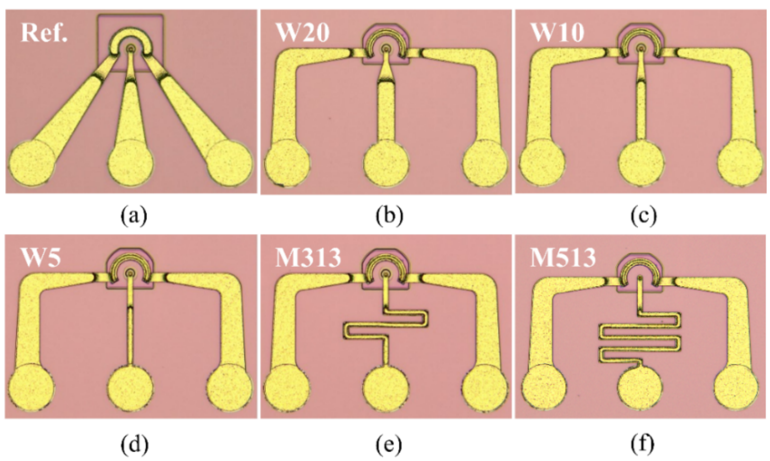

Fig. 2. Top view microscope images of the photodiodes with six different CPW electrode designs: (a) reference electrode, (b) signal line with a width of 20 µm, (c) 10 µm, and (d) 5 µm, with signal/ground spacings of 105 µm, 110 µm, and 112.5 µm, respectively, meandered signal lines with a width of 5 µm and lengths of (e) 313 µm, and (f) 513 µm.

To analyze RLC characteristics with respect to the electrode design, an equivalent circuit model of the photodiode was implemented using Advanced Design System (ADS) software. Figure 3 depicts the modeled equivalent circuit. The RC time constant region of Fig. 3 contains RLC parameters as follows: L_{cpw}, R_{cpw}, and C_{cpw} represent the inductance, resistance, and capacitance of the CPW transmission line including the GSG pads. C_{para}, R_s, C_j, and R_{sh} are denoted as the parasitic capacitance near the PIN diode anode/cathode electrodes, the series resistance, the junction capacitance, and the shunt resistance of the photodiode.

The transit time region is modeled as a first-order low-pass filter, and the parameters are detailed as: I_{in} for the input current proportional to the incident optical power, I_{tr} for the carrier transit current, I_{ph} for the photocurrent, R_{tr} and C_{tr} for the resistance and capacitance of the transit

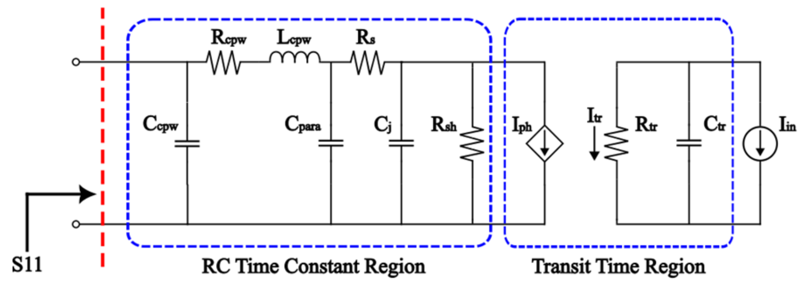

Fig. 3. Equivalent circuit model of the photodiode.

time region. The transit time (τ_{tr})-limited 3-dB bandwidth (f_{tr}) is determined by the product of the R_{tr} and C_{tr}. The transit time of the electrons and holes was calculated using commercial TCAD software (Lumerical CHARGE).

Figure 4 shows the transient response of the photodiode for electrons and holes. It depicts the propagation of the current pulse generated by light absorption in the absorption layer. The light turns on at the start of the simulation and turns off at 1 ps. This light pulse generates a current flow with respect to the bias voltage, and the current flux over time is recorded on the monitor. The transit time is defined by the time required for the current peak to travel to the monitor. The initial position of the current peak generated through the light pulse is set to 0.5 ps. The inset figure shows the simulation setup for electrons and holes. Figure 4(a) shows the simulation results for electrons. The light pulse is placed at the top of the p-absorption layer. The generated electrons travel through the p-absorption, i-absorption, and i-InP layers to the n-contact layer. The electron current monitor is placed at the bottom of the i-InP layer. The calculated transit times of the recorded electron current pulse on the monitor are 5.1, 4.3, 3.8, 3.6, and 3.0 ps for 0 V, -1 V, -2 V, -2.5 V, and -3 V bias voltages, respectively. Figure 4(b) shows the results for holes. The light pulse is placed at the bottom of the i-absorption layer. The generated hole current flows through the i-absorption layer to the p-absorption layer. The hole current monitor is placed at the top of the i-absorption layer. The calculated transit times are 8.3, 4.2, 3.2, 3.0, and 2.6 ps for 0 V, -1 V, -2 V, -2.5 V, and -3 V bias, respectively. Both current pulses exhibit dispersive characteristics, which decrease as the bias voltage increases. The transit time of conventional photodiodes is determined by the hole travel time. However, we engineered our PIN structure to make the hole travel time comparable to the electron travel time. The travel time of the generated electron pulse in the p-absorption layer to diffuse/drift into the i-absorption layer is about 1.2 ps regardless of the bias voltage. Then, the electron current pulse traverses the additional i-InP layer compared to the hole current. As a result, the transit time of the electrons becomes longer than that of the holes above -1 V bias. At the target bias voltage of -2.5 V, the transit time is determined to be 3.6 ps, limited by the electrons. The corresponding transit time-limited 3-dB bandwidth (f_{tr}) by the electron transit time is calculated to be 123.6 GHz using the relation $^{0.445}/_{\tau_{tr}}$. This f_{tr} is split into R_{tr} and C_{tr} in the equivalent circuit of Fig. 3 and set to 26 Ω and 48 fF, respectively. R_{sh} was fixed to 100 MΩ.

The S11 of the photodiodes was measured using a vector network analyzer (VNA) up to 67 GHz at a bias of -2.5 V. Figure 5(a)–(f) show Smith charts plotting the measured S11 scattering parameters (S-parameters) of the six different electrode designs and their fitted S-parameter curves for (a) Reference, (b) W20, (c) W10, (d) W5, (e) M313, and (f) M513, respectively. The dotted blue curves represent the measured data, and the red curves are the fitted S-parameter results from the equivalent circuit simulation in Fig. 3. Table 1 summarizes the extracted parameters.

The total capacitance, C_{total}, is the sum of C_{cpw}, C_{para}, and C_j, which was compared with the measured capacitance, $C_{measured}$, by a CV analyzer.

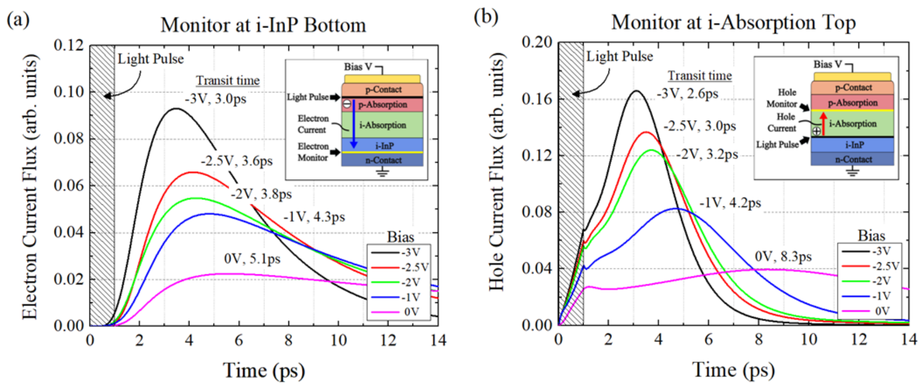

Fig. 4. Transit time simulation results for (a) electrons and (b) holes. Light pulse turns on for 1 ps and the generated electron and hole current pulses travel through the intrinsic region to the majority doping regions. Current monitor is placed at the end of the travel region and records the current flux. The transit time is calculated by the current peak travel time with respect to the applied bias voltage. The transit time is determined as the longer electron travel time due to the additional distances of p-absorption and i-InP layers except 0 V bias.

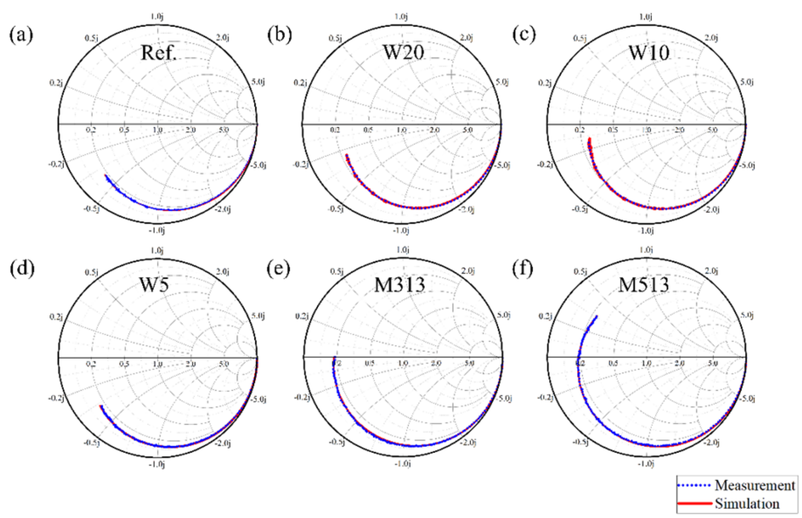

Fig. 5. Measured and simulated S11 Smith charts: (a) Reference, (b) W20, (c) W10, (d) W5, (e) M313, and (f) M513 electrode designs, respectively.

Table 1. Extracted RLC parameters from S11 fitting

Electrode Design	Rs	Rcpw	Lcpw	Ccpw	Cpara	Cj	Ctotal	CMeasured
Reference		8.2 Ω	64 pH	17 fF	33 fF		66.5 fF	66 fF
W20		9.5 Ω	95 pH	15 fF	30 fF		61.5 fF	64 fF
W10	36 Ω	8.7 Ω	112 pH	13 fF	30 fF	16.5 fF	59.5 fF	62 fF
W5		3.2 Ω	107 pH	14 fF	21 fF		51.5 fF	53 fF
M313		3.4 Ω	143 pH	16 fF	24 fF		56.5 fF	58 fF
M513		4.0 Ω	175 pH	18 fF	25.5 fF		60.0 fF	62.5 fF

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As shown in Table 1, R_s and C_j were fixed at 36 Ω and 16.5 fF, respectively, indicating that the PIN diode structure was unchanged while only the CPW electrode configuration and its parasitic parameters were modified. Both C_{total} and $C_{Measured}$ gradually decreased from the Reference electrode to the narrower signal electrodes W5. In contrast, these values increased from the W5 to M313 and M513 due to the increase in the signal electrode length. The inductance of the Reference was extracted as 64 pH. It increased by 31 pH to 95 pH in the W20. This increment can be attributed to the high impedance CPW electrode configuration owing to the increased signal/ground electrodes spacing in the air bridge as in Ref. [13]. It increased to about 110 pH in the W10 and W5 with narrower signal electrode widths. It increased by more than 30 pH from the W5 to M313 and from the M313 to M513, respectively, due to the increased signal electrode length of the meandered type.

4. O/E response measurements and discussion

The optoelectronic (OE) frequency response of the photodiodes has been measured by using the VNA and a thin-film lithium niobate (TFLN) electro-optical (EO) modulator of an 80-GHz bandwidth with a C-band light source. The measured S11 of the photodiodes was used, as shown in Fig. 5, to extract the RLC parameters. Figure 6 shows the measured frequency response of the photodiodes and the simulated S12 frequency response of the equivalent circuits. Since the transit time effect is considered in the circuit simulation, the measured and simulated data show good consistency. The 3-dB bandwidth of Reference design was measured at 48 GHz, whereas that of the W20 design extended to 58 GHz. The majority of the bandwidth extension is due to the inductance increment resulting from the enlarged spacing between the signal and ground electrodes. The W10 design was further extended up to 63 GHz by the inductance increment as summarized in Table 1. The OE responses of the W5, M313, and M513 designs were measured up to 67 GHz, constrained by the VNA frequency response range. The simulation results predicted the 3-dB bandwidths of 82 GHz, 80 GHz, and 77 GHz for the W5, M313, and M513 designs, respectively. The W5 design exhibited the greatest 3-dB bandwidth improvement, with an inductance of 107 pH and the lowest measured capacitance of 53 fF. The meandered designs of the M313 and M513 have higher inductances relative to the W5. However, they showed peak overshoots in the frequency responses, resulting in a reduced 3-dB bandwidth relative to the

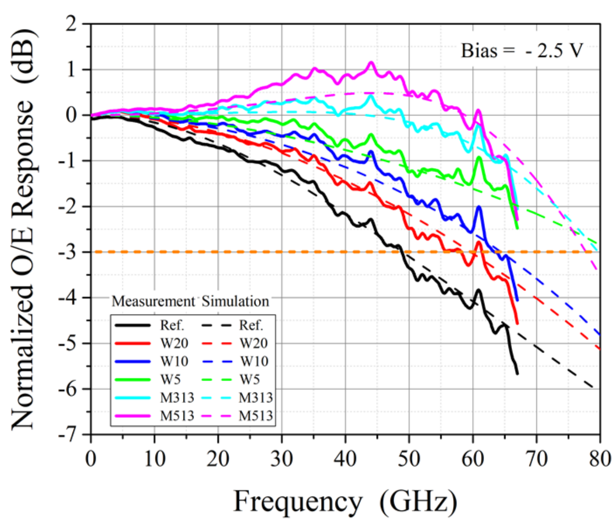

Fig. 6. Measured and simulated O/E responses with respect to the electrode designs.

W5. This indicates that the higher inductance does not necessarily result in a greater bandwidth increment. The difference between the measured and simulated results, specifically for the M513, is due to the imperfect circuit modeling of the inductances.

5. Conclusion

We have demonstrated that the 3-dB bandwidth of the backside-lens-integrated InGaAs photodiode can be effectively improved solely through the design configuration of the inductive electrode. Six different electrode designs were suggested and analyzed in detail using an equivalent circuit model to extract the R, L, and C parameters. The equivalent circuit contains the RC time constant region and the transit time region. The transit time for the electrons and holes was analyzed using numerical simulation. Since we designed the PIN diode structure for reducing the hole travel time, the transit time was determined as the electron travel time not the hole travel time. The calculated transit-time-limited 3-dB bandwidth is applied to the transit time region in the equivalent circuit. By including this transit time effect, the extracted values, obtained by fitting to the measured S11 data, were in good agreement with the measured O/E response curves. The 3-dB bandwidth of the reference conventional electrode design was 48 GHz at a bias voltage of -2.5 V and was extended to beyond 67 GHz through the electrode design optimization. The simulation predicted an optimum 3-dB bandwidth of 82 GHz with a 5-µm-wide straight design, corresponding to a performance improvement of 70.8%. We expect that conventional photodiodes can be utilized in next-generation datacenter applications requiring a 3-dB bandwidth exceeding 56 GHz by simply reconfiguring the electrode design.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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