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A Compact Inverter-Based Temperature Compensation for a Subthreshold Analogue Front-End in Noise-Shaping SAR ADC

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ABSTRACT

This letter presents an adaptive temperature compensation technique for a subthreshold analogue front-end (AFE) in low-power application. The conventional subthreshold AFE suffers from significant temperature dependency, compromising performance over a wide operating range. To overcome this critical issue, the proposed technique provides adaptive performance compensation, driven by a compact inverter-based sensor that identifies the current operating zone. This work was fabricated in a 180 nm CMOS process, where the core compensation blocks occupy a compact area of only 0.015 mm². To demonstrate its advantages, the proposed circuit was integrated with an AFE-embedded noise-shaping SAR ADC. Measurement results confirm robust performance for the entire system across a −40 to 80 °C range, with the proposed technique improving the average SNDR by 4.67 dB at low temperatures and achieving a power reduction of 4.02 μW at high temperatures. Notably, the compensation unit consumes less than 5.6 % of the total system power.

1 | Introduction

Analogue front-ends (AFEs) operating in the subthreshold region are widely adopted for low-power applications, particularly in the Internet of Things (IoT) and biomedical fields [1–3]. This is because the subthreshold region offers the highest transconductance efficiency (g_m/I_D) of any operating region, providing the maximum g_m for a given bias current [4]. However, the main disadvantage of this operating region is its inherent temperature dependency, originating from the exponential characteristic of the drain current. This dependency limits the reliable operating range and can compromise system performance. Therefore, a temperature compensation technique is required to ensure stable operation. For a temperature-compensated AFE, various approaches have been proposed, such as achieving high accuracy via precise analogue feedback [2], minimizing chip area and power through software post-

processing [3], or ensuring high flexibility with sophisticated digital architectures [5]. Although these methods achieve their respective goals, they exhibit clear trade-offs, including significant area overhead [2, 5] or the absence of real-time hardware compensation [3].

To address these limitations, this work introduces a new adaptive temperature compensation AFE optimized for low-power IoT systems. At its core, a compact, inverter-based temperature sensor adaptively identifies the current operating zone based on the AFE's performance limits, enabling a dynamic and targeted compensation. Notably, this real-time mechanism is enabled by a hardware-efficient implementation that reuses the complementary to absolute temperature (CTAT) voltage from the on-chip bandgap reference (BGR) and employs a PMOS-skewed inverter for the adaptive detection. The core contribution of this work is this approach, which ensures a wide operating temperature

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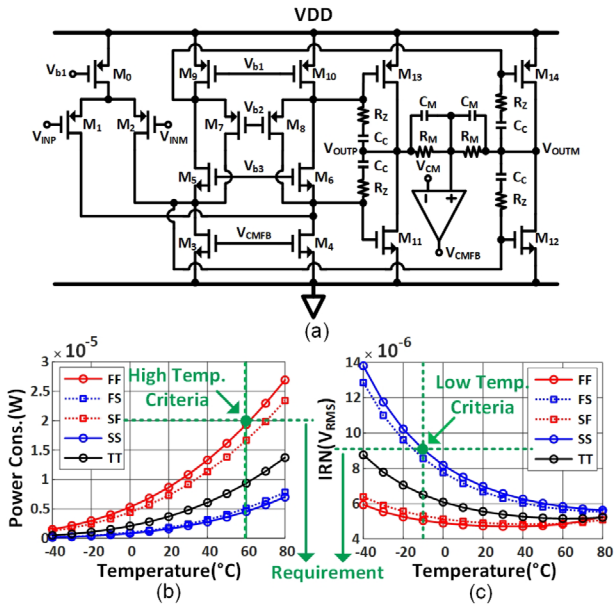


FIGURE 1 | (a) Circuit schematic of the AFE's core amplifier. (b) Simulated power consumption versus temperature across process corners. (c) Simulated input-referred noise versus temperature across process corners.

range while maximizing the crucial area and power efficiency for low-power applications.

2 | Determination of Temperature Criteria

Figure 1a shows the schematic of the designed AFE, where all MOSFETs operate in the subthreshold region. A PMOS input stage and a folded-cascode structure are employed for high gain and noise performance, while a class-AB output stage is used to ensure a wide output swing. However, subthreshold operation leads to significant performance variations with temperature. At low temperatures, the current supplied by the current source (M_0) to the input MOSFETs (M_1, M_2) decreases, reducing the g_m and thus degrading the input-referred noise (IRN) performance. Conversely, at high temperatures, the bias current increases, leading to higher current draw in each branch and a surge in total power consumption. This work establishes target specifications for IRN and power consumption to meet the stringent requirements of low-power IoT systems. Since the designed AFE is highly sensitive to process corners, simulations were performed under worst-case conditions to identify the specific temperatures at which its performance violates these target specifications, as depicted in Figure 1b,c. These identified points are defined as the low- and high-temperature criteria, which serve as the boundaries for partitioning the entire operating temperature range into three zones—low, mid, and high—for the proposed adaptive compensation.

3 | Proposed Adaptive Temperature Compensation System Architecture

To verify the performance of the proposed adaptive bias control (ABC) technique, a complete second-order AFE-embedded noise-

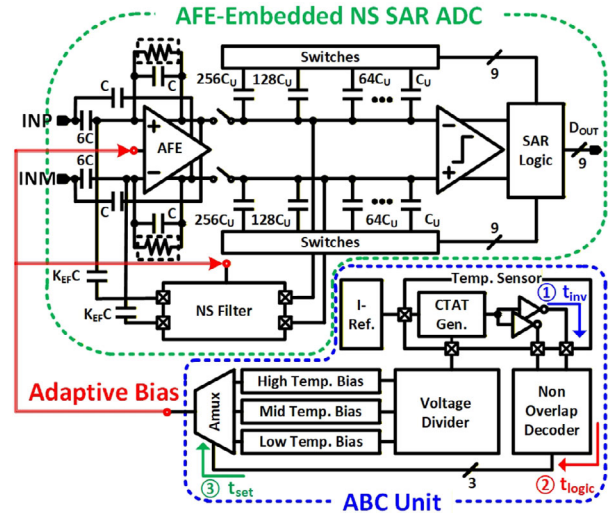


FIGURE 2 | Overall system architecture, including the AFE-embedded NS-SAR ADC and the proposed adaptive bias control unit.

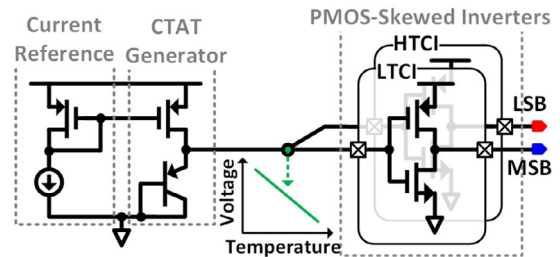


FIGURE 3 | Schematic of the proposed inverter-based temperature sensor.

shaping (NS) SAR ADC system was designed and fabricated, based on the architecture in [6]. Figure 2 shows the block diagram of the proposed overall system, where the components determining the ABC response time are indicated by circled numbers. A detailed discussion regarding this response time will be provided in a later section. While the ABC unit—consisting of a BGR, a temperature sensor, and an analogue multiplexer (AMUX)—is strategically applied to the AFE and NS filter to counteract g_m degradation, other critical blocks are designed to be inherently PVT-robust. Specifically, the reference circuitry is based on [7] to provide stable PVT-robust outputs, and the synchronous clock generator ensures sufficient timing margins across all corners. Furthermore, by segmenting the compensation into three temperature zones, the ABC technique significantly mitigates the design burden on the bias circuitry, ensuring superior stability and system integrity without imposing additional overhead on the reference sources.

3.1 | Inverter-Based Temperature Sensor

The core of the ABC unit is the temperature sensor, which is designed to detect the specific temperature criteria points where the AFE's performance (IRN or power consumption) would violate design requirements. As detailed in Figure 3, the sensor operates by comparing the CTAT voltage provided by the

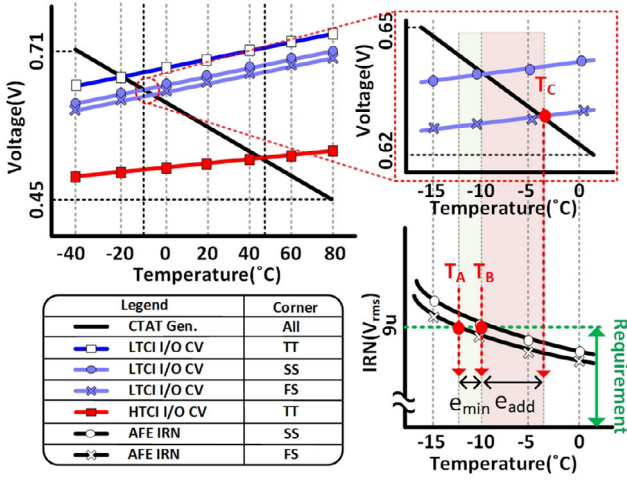


FIGURE 4 | Analysis of the temperature criteria shift and resulting errors due to process variations.

BGR with the I/O crossing voltages (CV) of two PMOS-skewed inverters: the low-temperature criteria inverter (LTCl) and the high-temperature criteria inverter (HTCl).

This approach offers two key advantages. First, the opposing temperature slopes of the CTAT voltage and the inverter's CV guarantee an intersection, ensuring reliable temperature detection. Second, by using the same PMOS-skewed inverter structure as the PMOS-dominant AFE, it inherently tracks shifts in the temperature criteria caused by process variations. This inverter-based approach provides an area- and power-efficient hardware solution that enables real-time compensation without complex circuitry.

3.2 | Analysis of Process Variation Impact

While the ABC technique is designed for temperature compensation, it is crucial to analyze how process variations affect the accuracy of the temperature criteria points. The AFE's performance is dominated by PMOS characteristics, and the sensor is designed accordingly; however, variations in the NMOS process corner can introduce errors to the criteria.

Analysing the exemplary case where the NMOS process corner shifts to fast (F) with Figure 4 reveals that two conflicting effects occur simultaneously.

First is the change in the AFE's own characteristics. Based on the designed AFE in Figure 1a, the V_{ds} of the gain stage transistors ($M_{3,4}$) decreases in the FS corner compared to the SS corner. This, in turn, increases the V_{sd} of the current source (M_0), which slightly boosts the current flowing into the input transistors ($M_{1,2}$). This slight increase in current enhances the g_m of the input MOS ($M_{1,2}$), improving the AFE's noise (IRN) performance. Therefore, the required low-temperature criterion should ideally shift down to a colder temperature (T_A). This deviation ($T_B - T_A$) from the worst-case (SS) criterion (T_B) introduces a minimal, acceptable error (e_{min}).

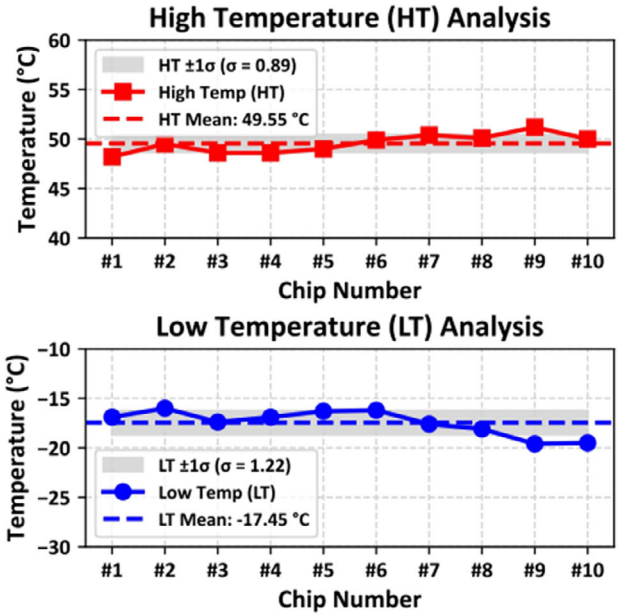


FIGURE 5 | Measured distribution of the low- and high-temperature criteria points for 10 fabricated chips.

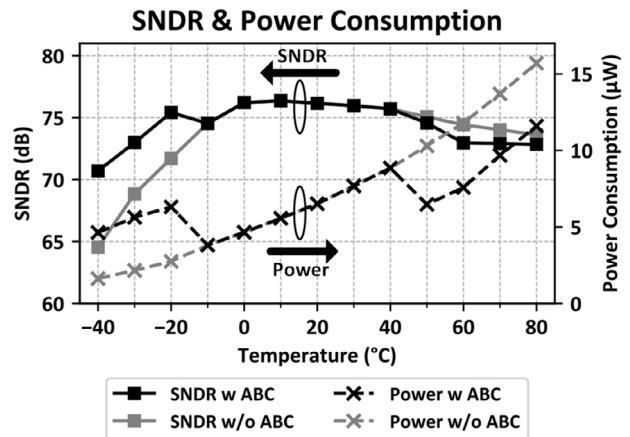


FIGURE 6 | Measured SNDR and power consumption versus temperature with and without the ABC technique enabled.

Second is the malfunction of the temperature sensor. However, in the same FS corner, the NMOS threshold voltage (V_{THN}) also decreases, which lowers the skewed inverter's CV. This causes the sensor to perceive the temperature as colder than it actually is, resulting in the detected low-temperature criterion erroneously shifting up to a warmer temperature (T_C). This additional, undesired error ($T_C - T_B$) corresponds to e_{add} .

$$CV(V) = \frac{(V_{DD} + V_{THP})\sqrt{\frac{\beta_P}{\beta_N}} + V_{THN}}{1 + \sqrt{\frac{\beta_P}{\beta_N}}} \quad (1)$$

$$e_{add}(^{\circ}C) = \frac{\Delta V_{THN}}{|CTAT \text{ Slope}| \times \left(1 + \sqrt{\frac{\beta_P}{\beta_N}}\right)} \quad (2)$$

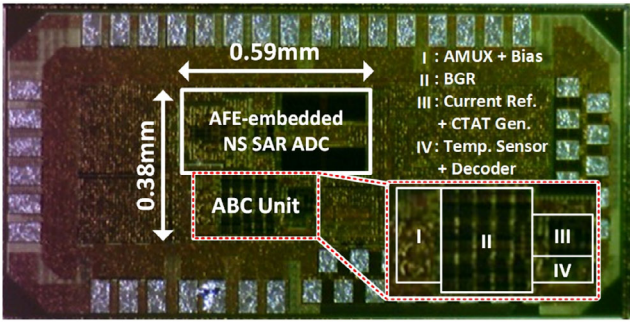


FIGURE 7 | Chip micrograph.

TABLE 1 | Measured performance and comparison of the proposed system.

Part I: AFE-embedded NS SAR ADC performance summary			
Supply (V)/sampling freq. (kHz)	1.0 / 64		
Bandwidth (kHz)/area (mm ²)	2.0 / 0.13		
Power consumption (μW)	27 °C	-40 °C	80 °C
- W/O ABC	7.3	1.6	15.7
- With ABC	—	4.6	11.6
SNDR (dB)	27 °C	-40 °C	80 °C
- W/O ABC	76.2	64.5	73.6
- With ABC	—	70.7	72.8
Part II: temperature compensation circuit performance comparison			
Parameters	This work	TACSI 2015 [2]	ISCAS 2025 [5]
Process (nm)	180	65	65
Temp. range (°C)	-40 to 80	-20 to 110	-20 to 100
Core area (mm ²)	0.015	0.012	0.156
Power (μ W)	0.24–0.89	~1	<0.195
Architecture	Inv.-based	Ana.-feedback	Dig.-tuning

Consequently, these opposing trends cause the adaptive bias to switch into the low-temperature mode prematurely at T_C , instead of the ideal point T_A . This activates the unnecessary high-current mode, leading to extra power consumption. The e_{add} term is directly related to the V_{THN} term in the inverter's CV equation (1), and the acceptable error temperature can be calculated via equation (2). Here, the parameter β used in equation (1) is defined as the product of the transistor's aspect ratio, carrier mobility (μ), and oxide capacitance (C_{OX}), where $\beta = \text{aspect ratio} \times \mu \times C_{\text{OX}}$. This formula provides a guideline for adjusting the CTAT slope and inverter sizing to mitigate this error. In this work, the maximum variation of the V_{THN} was first quantified through 100-run Monte Carlo simulations across five corner conditions. Subsequently, to ensure sufficient design margin, the PMOS-skewed inverter was sized by constraining

the maximum acceptable error to within 5 °C. Furthermore, the response time was assessed across process corners to ensure real-time stability. The worst case occurs at the SS corner during mid-to-low transitions; here, the increased V_{TH} minimizes the driving current, maximizing the sensor delay to $t_{\text{inv}} = 6.3 \mu\text{s}$ (① in Figure 2). Including the non-overlap decoder delay ($t_{\text{logic}} = 0.3 \mu\text{s}$, ②) and bias settling times ($t_{\text{set}} = 0.2 \mu\text{s}$, ③), the total response time is 6.8 μs . This remains within the 15.625 μs sampling period, enabling stable background compensation within a single conversion cycle.

4 | Measurement Results

This section presents the measurement results of the proposed system, fabricated in a 180 nm CMOS process and characterized across a temperature range of -40 to 80 °C.

Figure 5 shows the measured distribution of the temperature criteria points for 10 fabricated chips. The average low- and high-temperature criteria were measured at -17.45 and 49.55 °C, respectively. The standard deviations for the low- and high-temperature criteria were 1.29 and 0.94 °C, respectively. The maximum observed variations of 3.6 °C for the low-temperature criterion and 3.0 °C for the high-temperature criterion confirm that all chips operate within the predefined acceptable error margin. Figure 6 illustrates the effect of the proposed ABC technique on the measured SNDR and power consumption versus temperature. With the ABC technique, the average SNDR is improved by 4.67 dB in the low-temperature range, while power consumption is reduced by 4.02 μW in the high-temperature range with minimal performance degradation. This result demonstrates that the ABC technique effectively ensures the system's reliability under various temperature conditions. Figure 7 shows the micrograph of the fabricated chip. The active area of the AFE-embedded NS-SAR ADC is 0.13 mm². The proposed ABC unit (I + II + III + IV in Figure 7) occupies a total active area of 0.061 mm², of which the core blocks (III + IV in Figure 7), including the temperature sensor, decoder, CTAT generator, and current reference, account for only 0.015 mm², demonstrating a compact implementation. Table 1 provides an intuitive overview of the performance improvement from the ABC technique under worst-case conditions across room, low, and high temperatures. Moreover, while implemented in a 180 nm process, the proposed unit achieves sub- μW real-time compensation over -40 to 80 °C, demonstrating competitive area efficiency and superior robustness compared to contemporary 65 nm counterparts [2, 5].

5 | Conclusion

This letter presented a compact, inverter-based temperature compensation technique, fabricated and verified in a 180-nm CMOS process. The proposed ABC unit adaptively addresses the challenges of each operating zone to ensure performance stability across -40 to 80 °C with minimal overhead. Occupying a core area of only 0.015 mm², the ABC unit improves SNDR by 4.67 dB at low temperatures and saves 4.02 μW at high temperatures while consuming less than 5.6% of total system power. By providing a robust and area-efficient hardware solution

