Research Article Vol. 34, No. 6 / 23 Mar 2026 / Optics Express 11259
Optics EXPRESS

8-λ LAN-WDM TOSA for 800-Gb/s links with simplified, non-hermetic packaging

Soo-Yong Jung,[1] Eun Kyu Kang,[1] Won-Bae Kwon,[1] Sangjin Kwon,[1] Myunghwan Kim,[1] Gye-Sul Cho,[1] Hae Chung Kang,[1] Dae Woong Moon,[1] Seok-Jun Yun,[2] Young-Tak Han,[2] and Jongjin Lee[1,*]

[1] *Optical Packaging Research Section, Honam Research Division, Electronics and Telecommunications Research Institute (ETRI), Gwangju 61012, Republic of Korea*
[2] *Photonics/Wireless Devices Research Division, Electronics and Telecommunications Research Institute (ETRI), Daejeon 34129, Republic of Korea*
[*] *jongjin@etri.re.kr*

Abstract: We present an 8-λ local-area-network wavelength-division-multiplexing (LAN-WDM) transmitter optical subassembly (TOSA) for 800-Gb/s operation, using an epoxy-sealed, non-hermetic package for improved cost-effectiveness and manufacturability. To shorten packaging time and improve packaging yield, a ball-lens alignment scheme replaces a square lens, reducing per-lane alignment degrees of freedom from six to three. All eight wavelengths are locked to the LAN-WDM grid with a single thermoelectric cooler (TEC). In addition, inserting series DC-blocking capacitors in the electro-absorption-modulated laser (EML) radio-frequency (RF) path reduces the internal heat load, lowering the TEC input power from 1.294 W to 1.086 W ($\Delta P = 0.208$ W; 16.1% reduction). Under 53.125-Gbaud PAM4 modulation (8×106.25 Gb/s), the TOSA delivers clear eye diagrams with transmitter and dispersion eye closure for PAM4 (TDECQ) ≤ 3.0 dB and outer extinction ratio (ER) ≥ 3.7 dB across all lanes. In link tests with a PIN-photodiode receiver optical subassembly (ROSA), per-lane receiver sensitivities of −11.2 to −7.7 dBm are achieved after 20-km transmission at BER = 2.4×10^{-4}. These results indicate that the proposed non-hermetic 8-λ TOSA is a viable building block for ≥10-km intensity-modulated/direct-detect (IM/DD) 800-Gb/s deployments, with demonstrated operation over 20 km.

1. Introduction

The rapid growth of cloud services and AI workloads has driven an exponential rise in data traffic [1–4]. In particular, the proliferation of generative AI applications and large-scale accelerator platforms has accelerated upgrades of data-center networks. Consequently, transmitter optical subassemblies (TOSAs) for data centers and next-generation access networks must support higher transmission capacity [5–7].

To increase the capacity of TOSAs under fixed modulation bandwidth, the community has pursued advanced modulation and parallel transmission [5,8]. Modulation can be broadly divided into intensity-modulated/direct-detection (IM-DD) formats—predominantly four-level pulse-amplitude modulation (PAM4) for short- to medium-reach—and coherent formats—centered on quadrature amplitude modulation (QAM)—for longer reaches [9–14]. Although coherent has recently encroached on shorter distances, for 100-Gb/s and 200-Gb/s per-lane operation in 10-km-class links, IM-DD remains attractive owing to its lower power consumption and cost relative to coherent solutions [15,16]. Parallel transmission commonly adopts four-lane or eight-lane specifications: adding lanes scales capacity but increases the bill of materials and

#580570 https://doi.org/10.1364/OE.580570
Journal © 2026 Received 30 Sep 2025; revised 3 Mar 2026; accepted 5 Mar 2026; published 19 Mar 2026

Optics EXPRESS

the difficulty of assembling more components within compact transceiver form factors, thereby increasing packaging complexity and cost [17–23].

In intra–data-center optical interconnects, the O-band (1260–1360 nm) is commonly used because the fiber's zero-dispersion wavelength lies near 1310 nm, minimizing chromatic-dispersion penalties. As of 2025, IEEE 802.3df standardizes 800-GbE physical-medium-dependent (PMD) interfaces up to ~2 km, while ≥10-km 800-GbE optical PMDs remain under development within the P802.3dj project [24–26]. Industry literature often uses the shorthands "PLR8" (eight-lane parallel long reach) and "2×LR4" (dual 400G LR4) to describe implementations [27,28]. A PLR8-style approach employs eight parallel single-mode fibers per direction (16 fibers in total), thereby eliminating the need for wavelength-division-multiplexing (WDM) optics. As a result, the packaging complexity is mitigated at the expense of higher cabling cost. By contrast, a 2×LR4 module integrates two 400G LR4 engines on the CWDM4 grid, reducing fiber count to two duplex pairs (four fibers total), but increasing packaging complexity due to the internal multiplexer/demultiplexer (MUX/DEMUX). To further reduce cost, the use of a single duplex fiber interface is highly advantageous. However, placing eight channels on the 20-nm CWDM grid would require a spectral range from 1271 to 1411 nm, extending beyond the O-band where chromatic dispersion penalties become severe for 53.125-Gbaud PAM4 transmission over 10 km. This challenge motivates the use of local-area-network WDM (LAN-WDM), which keeps all eight channels within the low-dispersion O-band through finer channel spacing [29–32].

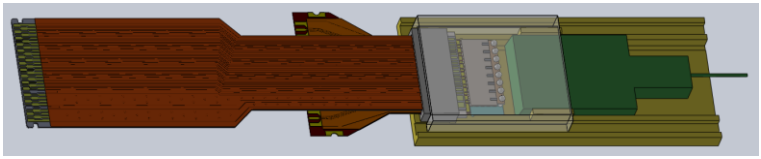
This work proposes an O-band 8-λ LAN-WDM TOSA for 800-Gb/s operation based on a non-hermetic and simplified packaging architecture. The proposed TOSA adopts a metal-substrate/ceramic-cover structure, reducing manufacturing cost relative to conventional hermetic packages with ceramic feedthroughs; the sealing step is simplified by epoxy sealing in place of seam welding. For the time-consuming alignment between the light sources and the arrayed-waveguide-grating (AWG) MUX, a ball lens is used instead of a conventional square lens, reducing the alignment degrees of freedom from six to three and thereby shortening the active-alignment time. Additionally, inserting series DC-blocking capacitors in the electro-absorption-modulated laser (EML) RF path at each electro-absorption modulator (EAM) electrode reduces the thermoelectric-cooler (TEC) heat load by 16.1%, enabling stable 8-λ control with a single TEC. Overall, these process and structural simplifications shorten production time, lowering manufacturing cost. The TOSA is intended for 800G transceivers in QSFP-DD800 and OSFP800 form factors, supporting a duplex interface with one fiber per direction. This paper details the TOSA's design, fabrication, and measured performance.

2. Design and fabrication of proposed 8-λ LAN-WDM TOSA

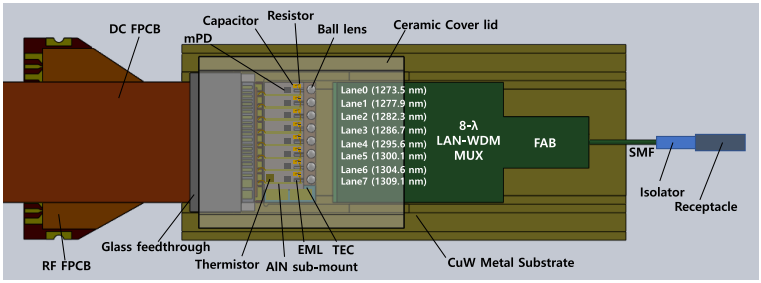
Figure 1 illustrates the proposed non-hermetic TOSA designed for low cost and low power: (a) a 3-D view and (b) a top view. To reduce cost, we adopt a non-hermetic sealing approach that epoxy-bonds a ceramic coverlid to a metal substrate, instead of conventional hermetic sealing with a metal package. The high-cost ceramic feedthrough traditionally used for electrical I/O is eliminated. Instead, radio-frequency (RF) and DC flexible printed circuit boards (FPCBs) are routed into the package, providing a more economical electrical interface. Although the sealing is non-hermetic, glass feedthrough inserts are bonded into the housing apertures to improve environmental isolation while allowing RF/DC FPCB routing. Two FPCBs—DC and RF—are introduced through the glass feedthrough; the RF FPCB is placed on the bottom side to shorten the bond-wire length to the EML transmission lines and thereby minimize RF loss.

Optical outputs from the eight EMLs are multiplexed by an 8-λ LAN-WDM AWG MUX and delivered over a single fiber. Each lane requires a coupling optic between the EML and the AWG MUX; in the proposed structure, a ball lens replaces the commonly used square (aspheric) lens. Owing to its rotational symmetry, the ball lens removes angular sensitivity, reduces the effective

Optics EXPRESS



(a)



(b)

Fig. 1. Schematic diagram of the proposed 8-λ LAN-WDM TOSA module: (a) 3D-view and (b) top-view of the TOSA.

alignment degrees of freedom from six to three (x, y, z only), and lowers alignment difficulty and time. A fiber-array block (FAB) is attached to the MUX output, enabling direct fiber egress without additional output-side lens alignment. The output receptacle integrates an optical isolator, which simplifies the TOSA structure and eliminates a separate isolator assembly step.

The TEC regulates the temperature of the eight EMLs mounted above it so that the emission wavelengths of all lanes remain within the LAN-WDM grid passbands. In the proposed design, a single shared TEC is sufficient to meet the wavelength-stability targets across lanes. The packaging stack comprises a copper–tungsten (CuW) baseplate, a TEC with aluminum nitride (AlN) ceramic plates, and an AlN submount for the EMLs. For efficient heat-spreading, the CuW baseplate (thermal conductivity $\approx 190\ \mathrm{W{\cdot}m^{-1}{\cdot}K^{-1}}$; CTE $\approx 7.0\times10^{-6}\ \mathrm{K^{-1}}$) is employed. Because AlN exhibits a CTE of $\approx 4.6\times10^{-6}\ \mathrm{K^{-1}}$, the CuW–AlN interface presents only a modest CTE offset of $\approx 2.4\times10^{-6}\ \mathrm{K^{-1}}$, which supports thermomechanical stability. The eight EMLs are placed on an 8-lane EML submount with 0.75-mm pitch. A larger lane pitch mitigates inter-lane thermal crosstalk; however, the compact QSFP-DD/-DD800 module envelope constrains the available volume, so we designed a compact TOSA of $11.4\times26\times3$ mm (W × L × H) to fit the module keep-out and thermal budget.

The EML chips are mounted on a single AlN submount, which provides favorable RF performance and efficient heat dissipation. On the submount, 50-Ω ground–signal–ground (GSG) transmission lines are implemented, and a 45–55-Ω tantalum-nitride (TaN) resistor is integrated near the EAM pad for impedance matching. To suppress a DC current through this matching element—and thereby lower static power that would otherwise add to the TEC heat load—we insert a series DC-blocking capacitor between the matching network and the EAM pad. In this topology, the matching resistor is seen at RF but is open at DC, so the quiescent dissipation term is effectively eliminated. A value of 100 nF was chosen as a compromise between size and bandwidth. The resulting RC high-pass corner is approximately 32 kHz, which is far below the spectrum of the 53.125-Gbaud PAM4 short stress pattern random quaternary (SSPRQ) stimulus which ranges from a few hundred kHz up to 26.56 GHz, so in-band attenuation is negligible. Because the 0.75-mm chip pitch left insufficient footprint for a 0402-class capacitor ($\approx 0.4\times0.2\times0.2$ mm (L × W × T)) in a lay-flat orientation, the capacitor was mounted on-edge

Optics EXPRESS

(upright). To avoid the longer bond wires and RF degradation that an upright part would introduce, we milled a cavity in the AlN submount and embedded the capacitor so that its top surface sits near the metallization plane, restoring short bond-wire lengths and consistent RF performance.

Figure 2 shows micrographs of the wire-bonded EML assembly, where the chip is connected to a matching resistor and an RF transmission line. In a high-density 8-lane engine, damage to a single chip during packaging can necessitate complex rework or result in the loss of the entire multi-chip set, significantly increasing manufacturing costs. To mitigate these risks and minimize RF parasitics, we adopted a ball-stitch bonding (daisy-chain) scheme instead of conventional wedge bonding. By applying a single continuous wire from the resistor pad to the EAM pad and finally to the transmission-line pad, we reduced the bonding step count and eliminated the need for multiple ball terminations on the small EAM pad. In typical bonding configurations, the parasitic capacitance (C_{par}) at the EAM pad node, primarily induced by the ball terminations, is one of the dominant factors limiting the operating bandwidth. The ball-stitch scheme effectively minimizes this C_{par} by removing the second ball termination, thereby pushing the parasitic-induced frequency limitation toward a higher range. This ensures that the measured frequency response (Fig. 6) accurately reflects the intrinsic EML performance rather than being restricted by bonding-related parasitic effects.

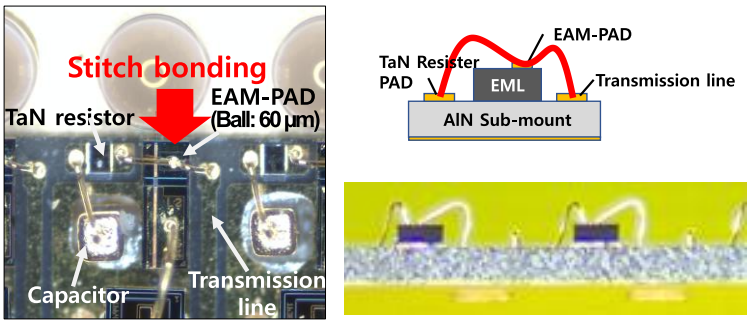


Fig. 2. Micrographs and design of the EML assembly: (Left) top-view of the ball-stitch bonding on the EAM pad, and (right) cross-sectional schematic of the EML on an AlN sub-mount.

To verify bond reliability with the stitch process, we performed a wire-pull test; the measured bond strength was 10.3 gf, which exceeds the MIL-STD-883 criterion of 3.0 gf, indicating no reliability concerns with the adopted bonding method [33].

To mitigate performance degradation of the EMLs due to optical back-reflections from the MUX waveguides, the MUX facet was polished at 8°, and an LC receptacle with an integrated optical isolator was used on the output fiber pigtail. Integrating the isolator at the receptacle eliminates the need for per-lane isolators inside the package, which simplifies assembly, shortens the optical path, and reduces sensitivity to optical-axis drift under external mechanical or thermal stress. The measured back-reflection was < -37.5 dB across all lanes, comfortably meeting the transmitter-reflectance limit of ≤ -26 dB [34].

For coupling from each EML to the MUX, 0.5-mm diameter high-index ball lenses (LAB0050, Knight Optical; LASFN35, n $\approx$ 1.978 at 1310 nm) with AR coating were employed. These lenses provide the necessary focusing capability for efficient light collection from the EML facet into the MUX interface. Replacing conventional aspheric or plano-convex lenses with ball lenses reduces the alignment degrees of freedom from six (x, y, z, ϕ_x, ϕ_y, ϕ_z) to three (x, y, z), thereby shortening alignment time and lowering manufacturing cost. The eight ball lenses were fixed between the EMLs and the AWG MUX using UV-curable epoxy at predetermined positions that balance coupling efficiency and tolerance to cure-shrinkage-induced misalignment. After alignment, the

Optics EXPRESS

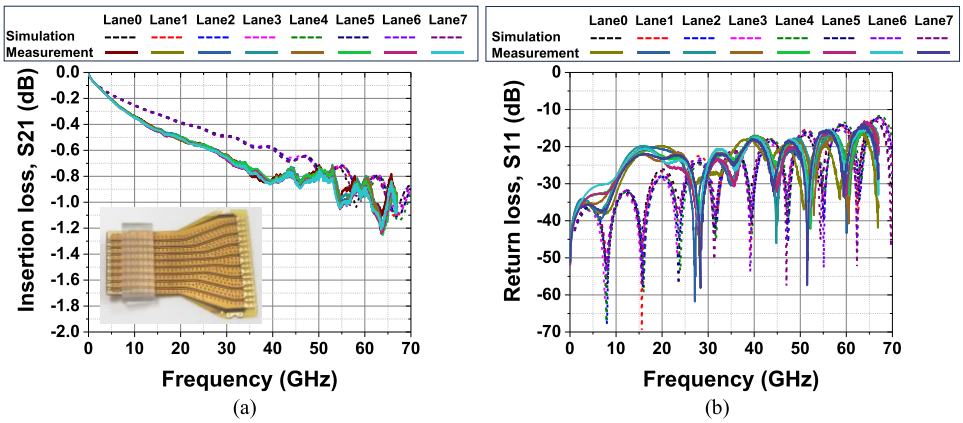


Fig. 3. Simulated and measured RF response of the RF FPCB passing through the glass feedthrough insert: (a) insertion loss, S21 (inset: photograph of the RF FPCB seated in the glass feedthrough insert) and (b) return loss, S11.

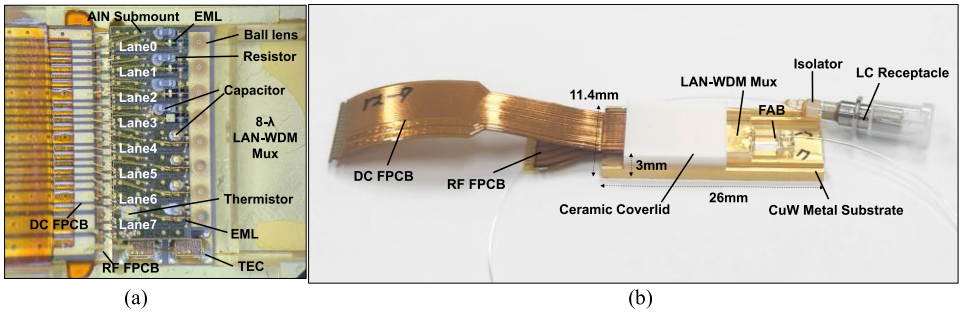


Fig. 4. (a) Enlarged internal view and (b) full photograph of the fabricated 800Gb/s 8-λ LAN-WDM TOSA.

EML-to-ball-lens gap was ≈ 40 µm, and the ball-lens-to-MUX distance was ≈ 1100 µm. In this work, two types of EMLs were employed across the 8 lanes: prototype R&D EML chips (Lanes 0–3) and commercial EMLs (HL13BCP00-Ln, Lumentum; Lanes 4–7). Despite the different chip sources, all EMLs were operated under identical electrical and thermal conditions (TEC at 45 °C, DFB bias of 80 mA). The per-lane EML output power was 10.0–11.7 dBm (L0–L7: 11.7, 10.0, 11.5, 11.3, 11.6, 11.0, 11.3, 11.0 dBm). After the MUX, the fiber-pigtail power was 3.2–4.8 dBm (L0–L7: 4.6, 3.7, 3.6, 4.8, 4.2, 3.8, 4.3, 3.2 dBm), with an estimated pre-MUX coupling efficiency of 32%–46%. These results demonstrate consistent electro-optical performance across all lanes, providing a reliable baseline for the system-level link budget.

To simplify manufacturing and improve throughput, the TOSA employs non-hermetic, polymeric (epoxy) sealing in place of seam-welded hermetic sealing [35]. Aluminum-free EMLs were selected so that a non-hermetic package can be used without compromising device reliability. A low-outgassing commercial epoxy was dispensed and vacuum-degassed to remove trapped bubbles before cure. To assess environmental robustness of the epoxy-sealed assembly—known to be susceptible to heat and humidity—we conducted the Telcordia GR-468-CORE damp-heat test (85 °C/85% RH, 500 h) on the TOSA. After exposure, the variation in optical output power was 0.04–0.47 dB across all lanes, which satisfies the acceptance criterion of $|\Delta P_{opt}| \leq 0.5$ dB. The presented 500-hour reliability results represent a preliminary verification of the proposed TOSA, and extended testing in accordance with full Telcordia requirements will be conducted

Optics EXPRESS

in future work. In a separate helium fine-leak measurement at room temperature, the package exhibited an equivalent leak rate of 5×10^{-8} atm·cc/s (He). While polymeric-sealed packages are not hermetic by definition, the measured leakage together with the 85/85 results indicates sufficient moisture-ingress resistance for the intended operating environment. Although epoxy outgassing can raise the internal moisture content even when sealed under nitrogen, typical data-center conditions keep the internal temperature safely above the ambient dew point, making condensation-related failures unlikely in normal operation.

Figure 3 shows the simulated and measured RF response of the RF FPCB that passes through the glass feedthrough insert. After inserting the FPCB into the glass feedthrough slot, the remaining slot–FPCB clearance was backfilled with epoxy to provide mechanical retention and seal against moisture ingress. The RF FPCB adopts a ground–signal–ground (GSG) coplanar waveguide with ground (CPWG) topology. The input pads are laid out with a 1.5-mm pitch to interface with the transceiver PCB in the assembled module, whereas the output pads follow the 0.75-mm lane pitch toward the EML array. The transmission line length is 14 mm, and the trace width and gap were optimized by 3D full-wave electromagnetic (EM) simulations in Ansys HFSS for a 50-Ω characteristic impedance. S-parameter measurements confirm that the epoxy-filled feedthrough introduces negligible RF degradation: over 0.01–60 GHz, the insertion loss remains $\leq$ 1 dB, and the return loss is $\geq$ 15 dB, consistent with the simulations.

Figures 4(a) and 4(b) show, respectively, an enlarged internal view and photographs of the fabricated 8-λ LAN-WDM 800-Gb/s TOSA. The size of the TOSA, excluding the RF/DC FPCBs and the fiber pigtail, is $11.4 \times 26 \times 3$ mm (W × L × H); this footprint fits within the internal volume of the QSFP-DD800 form factor. The eight EMLs are assembled on an AlN 8-lane submount with a 0.75-mm pitch, realizing 50-Ω GSG RF interconnects. A 45–55-Ω TaN series resistor followed by a 100-nF DC-blocking capacitor is integrated near the EAM pad, and the optical engine is mounted on a CuW baseplate with a single shared TEC.

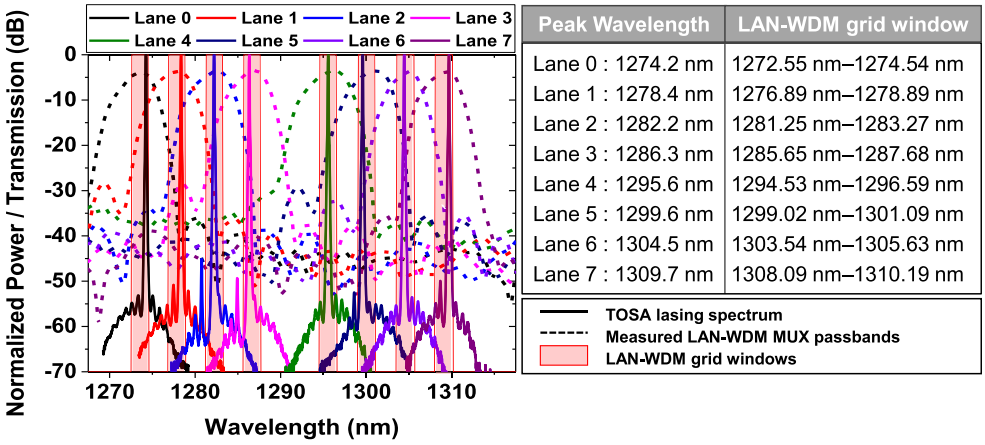
3. Experimental results

Figure 5 shows the emission spectra of the EMLs for Lanes 0–7, measured at the TOSA output while enabling one lane at a time, together with the measured passbands of the 8-channel LAN-WDM MUX. Each EML was biased at 80 mA and the TEC was set to 45 °C. All lanes exhibit a side-mode suppression ratio (SMSR) of $\geq$ 40 dB. The emission wavelengths lie within the 8-λ LAN-WDM center-wavelength specification (1273.5, 1277.9, 1282.3, 1286.7, 1295.6, 1300.1, 1304.6, 1309.1 nm), with a detuning $|\Delta\lambda|$ of 0.03–0.74 nm. The shaded regions in Fig. 5 represent the wavelength windows defined by the 8-λ LAN-WDM grid, within which each EML wavelength is properly aligned with sufficient margin to ensure reliable filtering and minimal spectral distortion.

Figure 6 shows the small-signal electro-optical (E/O) magnitude response of the 8-λ LAN-WDM TOSA measured with a Keysight N4373D lightwave component analyzer (LCA) at a laser bias of 80 mA, an EAM reverse bias of −0.7 V, and a TEC temperature of 45 °C. The coaxial cable, bias-tee, and probe were de-embedded so that the RF reference plane is at the TOSA RF FPCB pad, which was directly probed. The FPCB GSG traces are 50 Ω up to the pad; however, because the pad geometry is co-designed for solder attachment to the host PCB land pattern, probing the bare pad introduces a residual impedance mismatch. The measured 3-dB E/O modulation bandwidths across the eight lanes range from 30.0 to 36.7 GHz; all lanes therefore exceed the 26.5-GHz Nyquist frequency for 53-Gbaud PAM4, leaving margin for transmitter/receiver equalization.

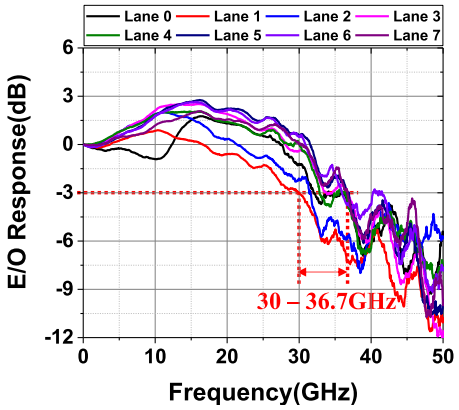
Figure 7 shows the test setup used to evaluate the fabricated TOSA. We measured optical eye diagrams and bit-error-rate (BER) for a 53.125-Gbaud PAM4 signal. A PAM4 waveform generated by a Maxlinear MxL93682 digital signal processor (DSP) evaluation board (EVB) was delivered to the 8-λ LAN-WDM TOSA through an RF probe. The DSP integrates a high-speed

Optics EXPRESS



Peak Wavelength	LAN-WDM grid window
Lane 0 : 1274.2 nm	1272.55 nm–1274.54 nm
Lane 1 : 1278.4 nm	1276.89 nm–1278.89 nm
Lane 2 : 1282.2 nm	1281.25 nm–1283.27 nm
Lane 3 : 1286.3 nm	1285.65 nm–1287.68 nm
Lane 4 : 1295.6 nm	1294.53 nm–1296.59 nm
Lane 5 : 1299.6 nm	1299.02 nm–1301.09 nm
Lane 6 : 1304.5 nm	1303.54 nm–1305.63 nm
Lane 7 : 1309.7 nm	1308.09 nm–1310.19 nm

Fig. 5. Emission spectra of the 8 lanes at the TOSA output, together with the measured LAN-WDM MUX passbands and the LAN-WDM grid wavelength windows. Bias: 80 mA; TEC: 45 °C.



3dB Bandwidth
Lane 0 : 32.0 GHz
Lane 1 : 30.0 GHz
Lane 2 : 31.4 GHz
Lane 3 : 33.8 GHz
Lane 4 : 32.8 GHz
Lane 5 : 36.7 GHz
Lane 6 : 36.0 GHz
Lane 7 : 36.7 GHz

Fig. 6. Small-signal E/O frequency responses of the 8-λ LAN-WDM TOSA measured at 80 mA laser bias, −0.7 V EAM bias, and TEC temperature of 45 °C.

output driver capable of directly driving the EML, and therefore no separate external driver chip was required in the experimental setup. Laser bias currents were supplied to the EMLs' DFB-LDs by a current source, and a TEC controller maintained the TOSA temperature. The EAM bias voltage was provided together with the PAM4 RF drive by the DSP EVB. Eye diagrams were captured using a Keysight 86100D digital communication analyzer (DCA) equipped with a 65-GHz optical module (N1030A). For BER measurements, the optical output was detected by a PIN-PD receiver optical subassembly (ROSA), and the resulting electrical signal was input to the DSP EVB for BER evaluation.

Figure 8 shows back-to-back (B2B) eye diagrams of 53.125-Gbaud PAM4 signals from each lane of the fabricated 8-λ LAN-WDM TOSA. The DFB-LD bias current was set to 70–100 mA and the EAM reverse bias to −0.5 to −0.9 V, while the TOSA TEC was held at 45 °C. Transmitter and dispersion eye closure for PAM4 (TDECQ) was evaluated using the IEEE 802.3 reference equalizer with a 5-tap feed-forward equalizer (FFE). To enable a fair comparison of modulation quality across lanes, the received optical power was normalized to −2 dBm for all channels when measuring the PAM4 eye diagrams and extracting TDECQ values. Across the eight lanes, the

Optics EXPRESS

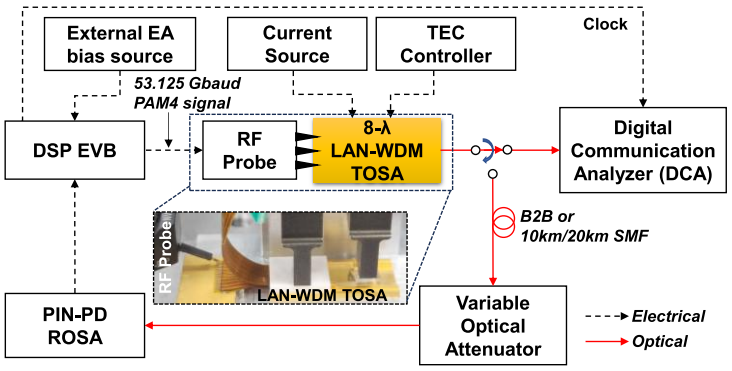


Fig. 7. Test setup for evaluating the fabricated 8-λ LAN-WDM TOSA.

outer extinction ratio (outer-ER) is 3.73–5.67 dB and TDECQ is 1.59–2.93 dB. Although lanes 0 and 1 exhibit slightly higher TDECQ and lower outer-ER than the others, all lanes remain compliant with the specification limits (TDECQ ≤ 3.9 dB, outer-ER ≥ 3.5 dB) [34]. Notably, at the time of writing, there is currently no published IEEE or MSA specification for 8-lane, ≥ 10-km, 800-Gb/s WDM transmitters; therefore, we reference the widely adopted 400G-LR4-10 criteria for context.

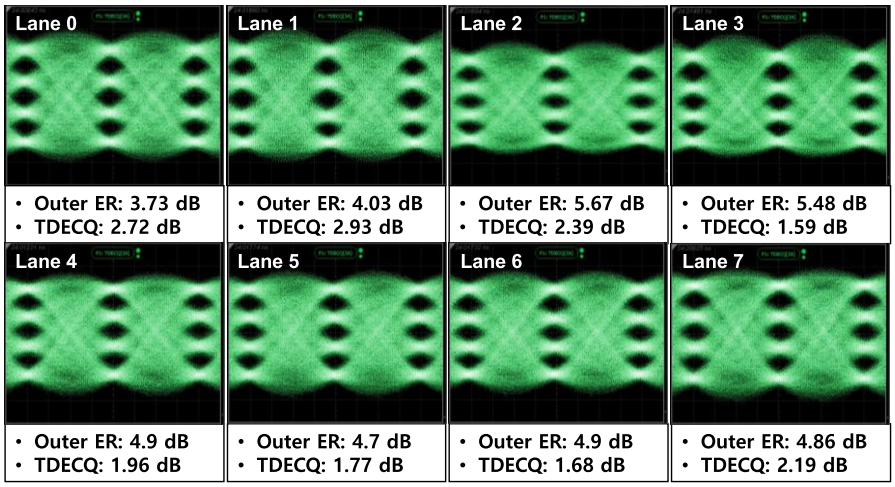


Fig. 8. Measured optical eye diagrams of 53.125-Gbaud PAM4 signals for each lane of the fabricated 8-λ LAN-WDM TOSA. All measurements were obtained at a normalized received optical power of −2 dBm to ensure consistent evaluation conditions.

Figure 9 presents the BER curves of the 53.125-Gbaud PAM4 optical outputs from each lane of the 8-λ LAN-WDM TOSA after (a) back-to-back (B2B) transmission and after propagation over single-mode fiber (SMF) for (b) 10 km and (c) 20 km. Table 1 summarizes the receiver sensitivity at BER = 2.4×10^{-4} and the corresponding distance-induced penalties for the eight lanes. Receiver sensitivities are reported in dBm and rounded to 0.1 dB; penalties are computed from the unrounded measurements and then rounded for display. Penalties are defined as Sensitivity(distance) − Sensitivity(B2B), so positive values indicate degradation.

With a PIN-PD ROSA, the per-lane sensitivities at BER = 2.4×10^{-4} span −11.1 to −9.0 dBm for B2B, −11.1 to −8.7 dBm after 10 km, and −11.2 to −7.7 dBm after 20 km. In B2B measurements,

Optics EXPRESS

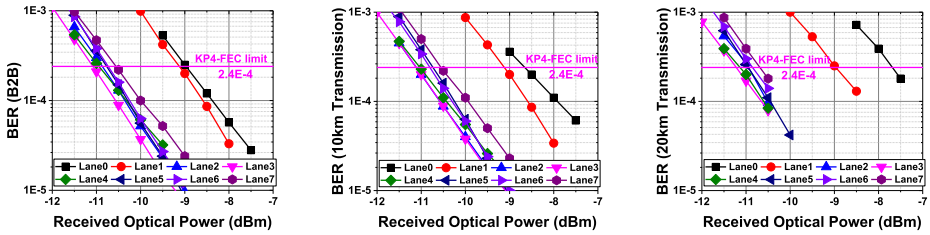


Fig. 9. BER curves of the 53.125-Gbaud PAM4 outputs from each lane of the 8-λ LAN-WDM TOSA for (a) back-to-back (B2B), (b) 10 km, and (c) 20 km transmission.

Table 1. Receiver sensitivity at BER = 2.4×10^{-4} and distance-induced penalties for the eight lanes.

Unit: sensitivities in dBm, penalties in dB

	Lane0	Lane1	Lane2	Lane3	Lane4	Lane5	Lane6	Lane7
Back-to-back (B2B)	-9.0	-9.1	-10.9	-11.1	-10.9	-10.8	-10.7	-10.6
10 km	-8.7	-9.1	-11.1	-11.1	-11.0	-10.7	-10.8	-10.6
20 km	-7.7	-9.0	-11.0	-11.2	-11.1	-11.0	-10.9	-10.7
Penalty @10 km	0.3	0	-0.3	0	-0.1	0	-0.1	0
Penalty @20 km	1.3	0.2	-0.1	-0.1	-0.2	-0.2	-0.2	-0.1

[a]Penalty = Sensitivity(distance) − Sensitivity(B2B); positive = worse (more power required).
[b]Values rounded to 0.1 dB. Penalties are computed from unrounded measurements and then rounded for display.

lane 0 and lane 1 exhibit sensitivities of −9.0 dBm and −9.1 dBm, respectively—about 1.5 dB higher (i.e., poorer) than the remaining lanes (−11.1 to −10.6 dBm). This degradation is consistent with their higher TDECQ and lower outer-ER, which stem from the sub-optimal E/O response and modulation characteristics of the prototype R&D EML chips used in these lanes. As shown in Fig. 6, Lane 0 suffers from a frequency dip near 10 GHz, while Lane 1 possesses the narrowest 3-dB bandwidth (30.0 GHz), both of which contribute to TDECQ elevation. Additionally, the relatively immature design of the prototype EMLs leads to a reduced outer-ER, further penalizing the receiver sensitivity. While the frequency dip observed in lane 0 is primarily attributed to the intrinsic characteristics of the prototype chip, further optimization of the packaging process—such as fine-tuning the bonding wire lengths to minimize parasitic resonance—could potentially mitigate this effect in future iterations.

For distance-induced penalties, all lanes except lane 0 remain within ±0.2 dB at both 10 km and 20 km, i.e., on the order of the ±0.1–0.2 dB measurement repeatability. This weak distance dependence is attributed to the small residual chromatic dispersion (CD) near the O-band zero-dispersion region around 1310 nm, which keeps the in-band frequency response relatively flat and limits inter-symbol interference (ISI) growth [36,37]. In contrast, lane 0 exhibits a penalty of 0.3 dB at 10 km and 1.3 dB at 20 km, which we attribute to its shorter wavelength being farther from the zero-dispersion point (larger |D|) together with its less favorable ER/TDECQ, leading to stronger CD–chirp interaction and increased ISI.

Table 2 summarizes the TEC power consumption of the 8-λ LAN-WDM TOSA with and without inserting a DC-blocking capacitor in the EAM RF path of the EML. Measurements were taken at an ambient temperature of 70 °C with the TEC set to 45 °C. Each lane's EAM was biased at −0.7 V and all eight lanes were driven with a 53.125-Gbaud PAM4 signal. At a DFB-LD bias current of 80 mA, the TEC input power decreased from 1.294 W (without DC-block) to 1.086 W (with DC-block), corresponding to a reduction of 0.208 W (≈16%). The reduction

Optics EXPRESS

originates from lowering the DC current through the EAM and its matching network when the series DC-block is inserted. With an EAM bias of −0.7 V, the EAM current drops from ∼45 mA to ∼15 mA (Δ≈30 mA), which reduces electrical dissipation by about 21 mW per lane (0.7 V × 30 mA). For eight lanes, this amounts to ≈0.168 W less internal heat. The smaller heat load reduces the required TEC lift and therefore the TEC input power, consistent with the measured 0.208 W decrease. The additional ∼40 mW relative to the simple 8× per-lane estimate is attributed to shifts in the TEC operating point (ΔT and control duty) and measurement repeatability.

Table 2. TEC power consumption with and without insertion of a series DC-blocking capacitor in the EAM path.

DFB-LD bias current (mA)	EAM bias voltage (V)	TEC power consumption (W)		Reduction ΔP (W, %)
		without DC-block	with DC-block	
80	−0.7	1.294	1.086	0.208 (16.1%)

4. Conclusion

We developed an 8-λ LAN-WDM TOSA that supports 8 × 106.25-Gb/s PAM4 operation on the LAN-WDM grid and a duplex interface with one fiber per direction. The module employs an epoxy-sealed, non-hermetic package and replaces a conventional square lens with a ball-lens alignment scheme, reducing per-lane alignment degrees of freedom from six to three and thereby shortening optical packaging time for the eight-lane assembly. In addition, inserting series DC-blocking capacitors in the EML RF path lowers the TEC input power from 1.294 W to 1.086 W (ΔP = 0.208 W; 16.1% savings).

Across lanes, SMSR exceeds 40 dB and LAN-WDM center-wavelength deviations range from 0.03 to 0.74 nm. Under 53.125-Gbaud PAM4 operation, clear eye diagrams are obtained with TDECQ = 1.59–2.93 dB and outer ER = 3.73–5.67 dB. With a PIN-PD ROSA, the measured per-lane receiver sensitivities at BER = 2.4×10^{-4} are −11.1 to −9.0 dBm (back-to-back), −11.1 to −8.7 dBm (10 km), and −11.2 to −7.7 dBm (20 km).

These results indicate that the proposed TOSA is a viable candidate for IM/DD 800-Gb/s deployments over distances exceeding 10 km, with demonstrated operation at 20 km. Furthermore, although the current 500-hour reliability data shows stable performance trends, full-scale qualification in accordance with industry standards, such as Telcordia GR-468 (e.g., 2,000 hours), remains a necessary step for future commercial deployment. We also examined the feasibility of a single-fiber LAN-WDM solution; future work will extend link-level demonstrations and investigate receiver-side options with a rigorous assessment of bandwidth, linearity, and excess-noise trade-offs.

Funding. Institute for Information and Communications Technology Promotion (IITP) funded by Korean government Ministry of Science and ICT (MIST) (RS-2021-II210395); Electronics and Telecommunications Research Institute grant funded by the Korea government (25ZK1150).

Acknowledgment. Institute for Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (RS-2021-II210395, Development of 800-Gbps optical transceiver for intra datacenter networks); Electronics and Telecommunications Research Institute (ETRI) grant funded by the Korea government (25ZK1150, Honam Region Regional Industry-based ICT Convergence Technology Advancement Support Project).

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. Cisco Annual Internet Report(2018–2023), White Paper (2020).

Optics EXPRESS

2. Q. Cheng, M. Bahadori, M. Glick, *et al.*, "Recent advances in optical technologies for data centers: a review," Optica **5**(11), 1354–1370 (2018).
3. T. Hoefler, A. Hendel, and D. Roweth, "The convergence of hyperscale data center and high-performance computing networks," Computer **55**(7), 29–37 (2022).
4. M. Y. Teh, Z. Wu, M. Glick, *et al.*, "Performance trade-offs in reconfigurable networks for HPC," J. Opt. Commun. Netw. **14**(6), 454–468 (2022).
5. M. Vallo and P. Mukish, "Global insights into the key technology enabling the exponential growth of digital communication networks," Proc. SPIE **11712**, 12 (2021).
6. G Pluggable MSA White Paper, "Enabling the next generation of cloud & AI using 800 Gb/s optical module," (2020).
7. P. Maniotis, L. Schares, D. M. Kuchta, *et al.*, "Toward higher-radix switches with co-packaged optics for improved network locality in data center and HPC networks," J. Opt. Commun. Netw. **14**(6), C1 (2022).
8. I. Tomkos, A. Tolmachev, A. Agmon, *et al.*, "Low-cost/power coherent transceivers for intra-datacenter interconnections and 5G fronthaul links," *ICTON 2019*, We.C1.2 (2019).
9. X. Zhou, R. Urata, and H. Liu, "Beyond 1Tb/s intra-data center interconnect technology: IM-DD or Coherent?" J. Lightwave Technol. **38**(2), 475–484 (2020).
10. J. Cheng, C. Xie, Y. Chen, *et al.*, "Comparision of coherent and IMDD transceivers for intra datacenter optical interconnects," *OFC2019*, W1F.2 (2019).
11. J. K. Perin, A. Shastri, and J. M. Kahn, "Data center links beyond 100Gbps per wavelength," Opt. Fib. Technol. **44**, 69–85 (2018).
12. X. Pang, O. Ozolins, R. Lin, *et al.*, "200 Gbps/lane IM/DD technologies for short reach optical interconnects," J. Lightwave Technol. **38**(2), 492–503 (2020).
13. S.-J. Yun, Y.-T. Han, D.-H. Lee, *et al.*, "112-Gbaud PAM4 operation of lumped-EML with 150-um EAM length using LC resonance based on matching resistance optimization," J. Lightwave Technol. **42**(1), 229–235 (2024).
14. S. Y. Lee, Y.-T. Han, J.-H. Kim, *et al.*, "Cost-effective 400-Gbps micro-intradyne coherent receiver using optical butt-coupling and FPCB wirings," Opt. Express **26**(22), 28453–28460 (2018).
15. S. Wilkinson, "The move to coherent inside the datacenter," *ECOC2023, Market Focus, Cignal AI* (2023).
16. X. Zhou, C. F. Lam, R. Urata, *et al.*, "State-of-the-Art 800G/1.6 T datacom interconnects and outlook for 3.2 T," *OFC 2023*, W3D.1 (2023).
17. T. Murao, N. Yasui, K. Mochizuki, *et al.*, "Lens alignment technique using high-power laser for hybrid integrated multi-channel transmitter optical sub-assemblies," IEEE Photonics Technol. Lett. **25**(20), 1958–1960 (2013).
18. E. K. Kang, S.-Y. Jung, S. Kwon, *et al.*, "Through-glass-via interposer for high-speed electrical interfacing in a 400 Gbps optical engine for on-board optics and pluggable optical transceivers," J. Lightwave Technol. **43**(11), 5390–5399 (2025).
19. Y.-T. Han, O.-K. Kwon, D.-H. Lee, *et al.*, "A cost-effective 25-Gb/s EML TOSA using all-inone FPCB wiring and metal optical bench," Opt. Express **21**(22), 26962–26971 (2013).
20. S.-J. Yun, Y.-T. Han, S.-T. Kim, *et al.*, "Optical subassembly modules using light sources butt-coupled with silica-based PLC," IEEE Photonics Technol. Lett. **32**(2), 132–135 (2020).
21. S.-J. Yun, Y.-T. Han, S.-T. Kim, *et al.*, "Compact hybrid-Integrated 4×800Gbps TROSA module using optical butt-coupling of DML/SI-PD and silica AWG chips,," J. Lightwave Technol. **39**(8), 2468–2475 (2021).
22. J. Liu, Q. Huang, and J. Xia, "High assembly tolerance and cost-effective 100-Gb/s TOSA with silica-PLC AWG multiplexer," IEEE Photonics J. **11**(4), 1–9 (2019).
23. S. Kanazawa, T. shindo, M. Chen, *et al.*, "High output power SOA Assisted extended reach EADFB Laser (AXEL) TOSA for 400-Gbit/s 40-km fiber-amplifier-less transmission," J. Lightwave Technol. **39**(4), 1089–1095 (2021).
24. IEEE Standards Association, "IEEE Std 802.3df-2024: IEEE standard for ethernet amendment 9: media access control parameters for 800 Gb/s and physical layers and management parameters for 400 Gb/s and 800 Gb/s Operation" (2024).
25. J. Maniloff, "Coherent solutions for 10 & 40 km 800 Gb/s objectives in 802.3dj," IEEE 802.3dj Task Force contribution (2023).
26. IEEE 802.3 Working Group, "The state of IEEE 802.3 Ethernet (P802.3dj closing report)," plenary report (2024).
27. FS.com, "800GBASE-PLR8 QSFP-DD 1310 nm 10 km Transceiver—Datasheet" (2022).
28. Smartoptics, "OSFP112 800G 2×LR4, CMIS5—Datasheet" (2024).
29. N. Ohata, Y. Kawamoto, M. Binkai, *et al.*, "A compact integrated LAN-WDM EML TOSA employing stripline with an aperture in the FPC," J. Lightwave Technol. **38**(12), 3246–3251 (2020).
30. X. Liu and Q. Fan, "Inter-Channel FWM mitigation techniques for 800G-LR4, 1.6T-LR8, 400G-ER4 and 5G fronthaul applications based on O-Band WDM," J. Lightwave Technol. **42**(3), 1085–1094 (2024).
31. J. Zhang, Q. Wang, J. Zhang, *et al.*, "Demonstration of terabit/s LAN-WDM for the evolution of B5G/6G fronthaul networks," IEEE Photonics J. **15**(4), 1–9 (2023).
32. J. Potet, M. Gay, L. Bramerie, *et al.*, "Real-time 400 Gbit/s PAM-4 optical link over 30 km for future access network," *OFC 2023*, San Diego, CA, USA, 1–3 (2023).
33. U.S. Department of Defence, "Test method standard microcircuits," MIL-STD-883 (2011).
34. G Lambda MSA Group, 400G-LR4-10 Technical Specification (2020).
35. United States Department of Defence, "Performance specification: hybrid microcircuits, general specification for," MIL-PRF-38543H, (2010).

Optics EXPRESS

36. G. P. Agrawal, *Fiber-Optic Communication Systems*, 4th ed. (Wiley, 2012).
37. W. Wang, Z. Zhang, J. Yu, *et al.*, "Transmitter and receiver DSP for 112 Gbit/s PAM-4 amplifier-less transmissions using 25G-class EML and APD," Opt. Express **26**(18), 22673–22686 (2018).