Received: 16 April 2025 | Revised: 8 August 2025 | Accepted: 16 September 2025

DOI: 10.4218/etrij.2025-0176

ORIGINAL ARTICLE

ETRI Journal WILEY

125-GHz-band RF receiver front end using 40 nm complementary metal–oxide–semiconductor technology

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Funding information
This work was supported by an Institute of Information and Communications Technology Planning and Evaluation (IITP) grant funded by the Korean government (MSIT) (No. 2022-0-01016, Development of ultra-precision low-cost sub-THz pulse-based radar chip).

Abstract

This paper presents a 125-GHz-band radio-frequency (RF) receiver front end designed for radar applications using 40 nm complementary metal–oxide–semiconductor (CMOS) technology. The receiver front-end chip integrates a five-stage single-to-differential low-noise amplifier, transconductance I/Q driver, quadrature I/Q passive mixer, quadrature I/Q transimpedance amplifier, single-to-differential local oscillator (LO) driver, and quadrature I/Q LO generator. Designing an I/Q receiver front end for the 125-GHz band is particularly challenging due to the difficulty of generating and maintaining well-matched I/Q signals at such high frequencies. This work demonstrates highly matched I/Q signal outputs using a simplified circuit architecture that achieves both low power consumption and a compact core chip size. Measurement results of the RF receiver front-end chip reveal a conversion gain of 30 dB, 3 dB bandwidth ranging from 121 GHz to 129 GHz, an input P1dB of −30 dBm, and a double-sideband noise figure of 11.4 dB. The measured gain and phase mismatches between the I and Q channels are only 0.1 dB and 3.6°, respectively. The chip operates with low power consumption, drawing only 80 mA from a 1 V supply. It also features a compact core area of 0.22 mm^2.

KEYWORDS
complementary metal–oxide-semiconductor, Radar, radio frequency, receiver front end, sub-THz

1 | INTRODUCTION

Compared with microwave radar, sub-THz waves offer advantages such as smaller size, lighter weight, and higher spatial resolution. These characteristics enable diverse applications in healthcare, including medical imaging, noninvasive monitoring, object detection, remote surgery, and delivery systems; security applications, including intelligent security systems, border surveillance, personal security screening, traffic monitoring, and unmanned monitoring systems; and entertainment and sports applications such as competitive sports, virtual reality, motion-sensing games, concert venues, and fitness monitoring [1].

Sub-THz-wave radar operates within the frequency band of 100 GHz to 300 GHz (wavelengths of 1 to 3 mm), and our work focuses on the 125 GHz frequency, corresponding to a wavelength of 2.4 mm. In our study, the unity gain frequency (fT) of the 40 nm complementary metal–oxide–semiconductor (CMOS) technology used

was approximately 280 GHz. This high fT value supports the design of effective radio-frequency (RF) receivers in the 125 GHz band [2–5].

This paper introduces a 125-GHz-band RF receiver front end developed using 40 nm CMOS process technology. The receiver front end integrates components such as a low-noise amplifier (LNA), transconductance I/Q driver, quadrature I/Q passive mixer, quadrature I/Q transimpedance amplifier, single-to-differential local oscillator (LO) driver, and quadrature I/Q LO generator. Section 2 outlines the radar system architecture and integrated RF receiver front-end structure. Section 3 presents the details of the circuit design. Section 4 presents measurement results, and Section 5 concludes this paper.

2 | STRUCTURE DESIGN

Figure 1 presents a block diagram of a 2-TX 3-RX time-division multiplexing, multiple-input multiple-output (TDM-MIMO) pulse radar transceiver consisting of transmitter, receiver, and frequency synthesizer sections. The transmitter section includes a TDM-MIMO pulse generator and two RF transmitter channels. The pulse generator, which is structured as a delay-locked loop, generates pulse trains and alternately transmits them to each RF transmitter. Each RF transmitter consists of a frequency up-converting mixer and a power amplifier (PA). The receiver section consists of three RF receiver channels, with an LNA, a frequency down-converting I/Q mixer, an I/Q low-pass filter, a variable-gain I/Q amplifier, and an I/Q analog-to-digital converter comprising each channel. The radar signal processor calculates range, velocity, and angle information. In the 2-TX 3-RX configuration, six virtual array datasets from the receiver are used for angle calculation via fast Fourier transformation, which enhances angle resolution in pulse radar.

Table 1 summarizes the design specifications of the radar transceiver. These specifications are provided for the antenna-on-package configuration. The target range

TABLE 1 Design specification of the radar transceiver.

Design target parameter		**Value**
Radar waveform type		Pulse
Carrier Frequency		122.5 GHz
(RCS = 2 m^2, SNR ← P_d = 0.9,P_{fa} = 1e-6, Non-fluctuating/ Coherent)		
Resolution	Range (cm)	15
	Angle (deg)	<10
Target speed max. (m/s)		122 (441 km/h)
Specification Results		**Value**
PRI (us)		5
Antenna gain (dB)		4
Required SNR (dB)		12.60
Receiver NF (dB)		16.02
Waveform bandwidth (GHz)		1
Dwell time (m/s) = PRI*8000		40
Velocity resolution (m/s)		30.06e-3
TX peak power (dBm)		8
Detection range (m)		5.07

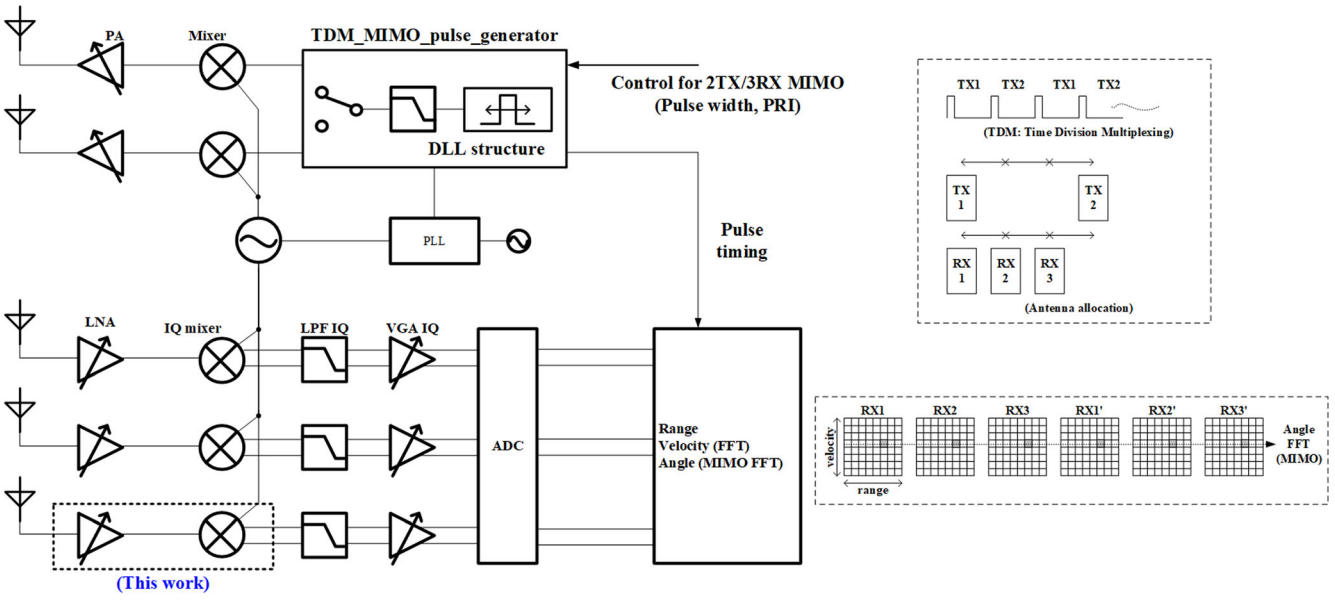

FIGURE 1 Block diagram of a 2-TX 3-RX TDM MIMO pulse radar transceiver.

resolution is 15 cm, which is achieved using a 1 GHz bandwidth. The resulting radar detection range is approximately 5 m.

We implemented the 125-GHz-band RF receiver front end illustrated in Figure 2, which consists of the following cascaded components: a low noise amplifier, transconductance IQ driver (IQ_Gm), quadrature I/Q passive mixer, quadrature I/Q transimpedance amplifier, single-to-differential LO driver, and quadrature I/Q LO generator. The 125-GHz-band LO signal is supplied externally by a frequency quadrupler, which is not considered in this work.

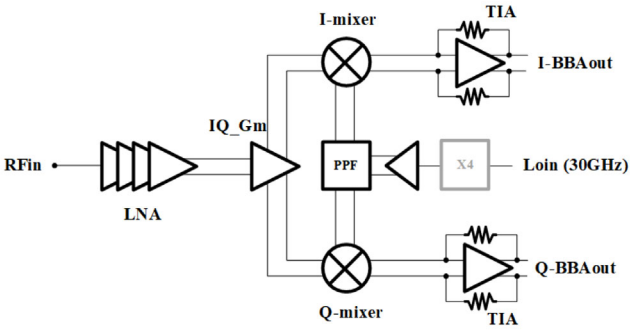

FIGURE 2 125-GHz-band RF receiver front-end block diagram.

3 | CIRCUIT DESCRIPTIONS

Figure 3 presents a five-stage single-to-differential low-noise amplifier circuit operating at 125 GHz. The circuit begins with an external single-ended input signal that is converted into a differential signal using a balun transformer. The input side of the balun transformer includes a series capacitor for AC coupling, whereas the output side features a center-tap capacitor to facilitate wideband single-to-differential operation. The core amplifier structure employs a common-source differential amplifier design coupled with the next stage via a transformer. This transformer coupling offers advantages such as simple

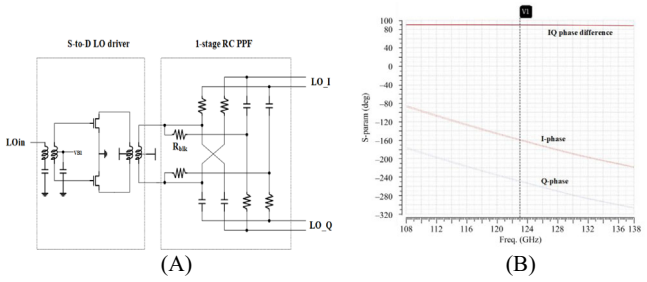

FIGURE 5 Single-to-differential LO driver and quadrature I/Q LO generator: (A) circuit schematic and (B) EM-simulated I/Q phase response.

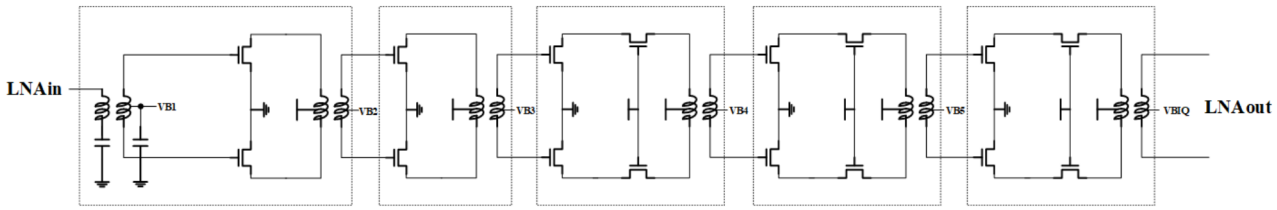

FIGURE 3 125GHz band five-stage single-to-differential low-noise amplifier circuit.

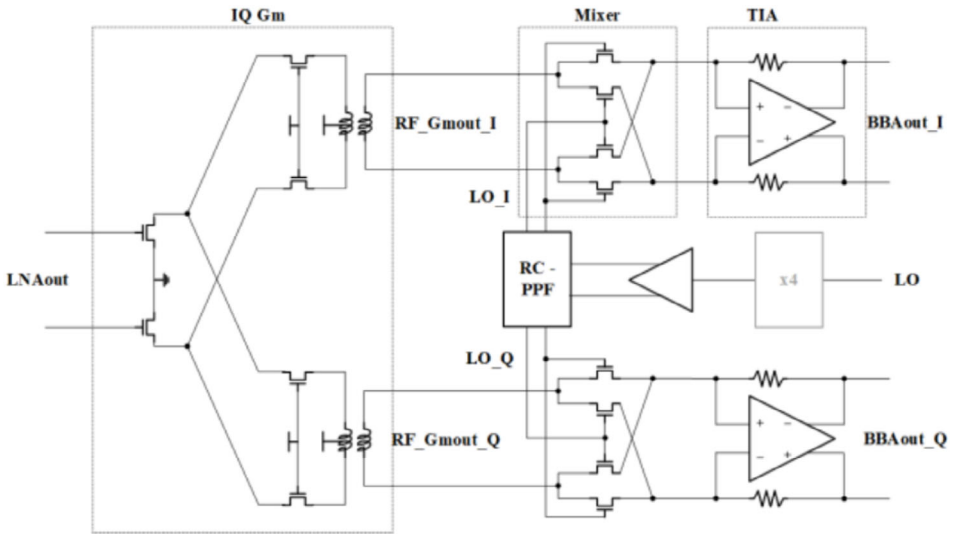

FIGURE 4 125 GHz band quadrature I/Q mixer circuit.

design and minimized interconnection length. Each of the five common-source amplifier stages is optimized to achieve a significant gain of approximately 30 dB [6].

Figure 4 illustrates the quadrature I/Q mixer circuit designed for operation at 125 GHz. Passive mixers employ a straightforward circuit structure but exhibit relatively high noise. Consequently, a front-end low-noise amplifier was designed to achieve significant gain. The IQ-Gm structure employs a cascaded amplifier configuration. The common differential input transistor of the IQ-Gm converts the voltage signals into current signals, which are then transferred to each I/Q branch transistor. The mixer itself is based on a balanced passive mixer structure with down-converted current signals being subsequently converted back to voltage signals using a baseband transimpedance amplifier.

Figure 5A presents the single-to-differential LO driver and quadrature I/Q LO generator circuit. The driver circuit includes a balun transformer and a differential common-source amplifier with a transformer load. The quadrature I/Q LO generator circuit utilizes an RC polyphase filter design. Although various techniques exist for

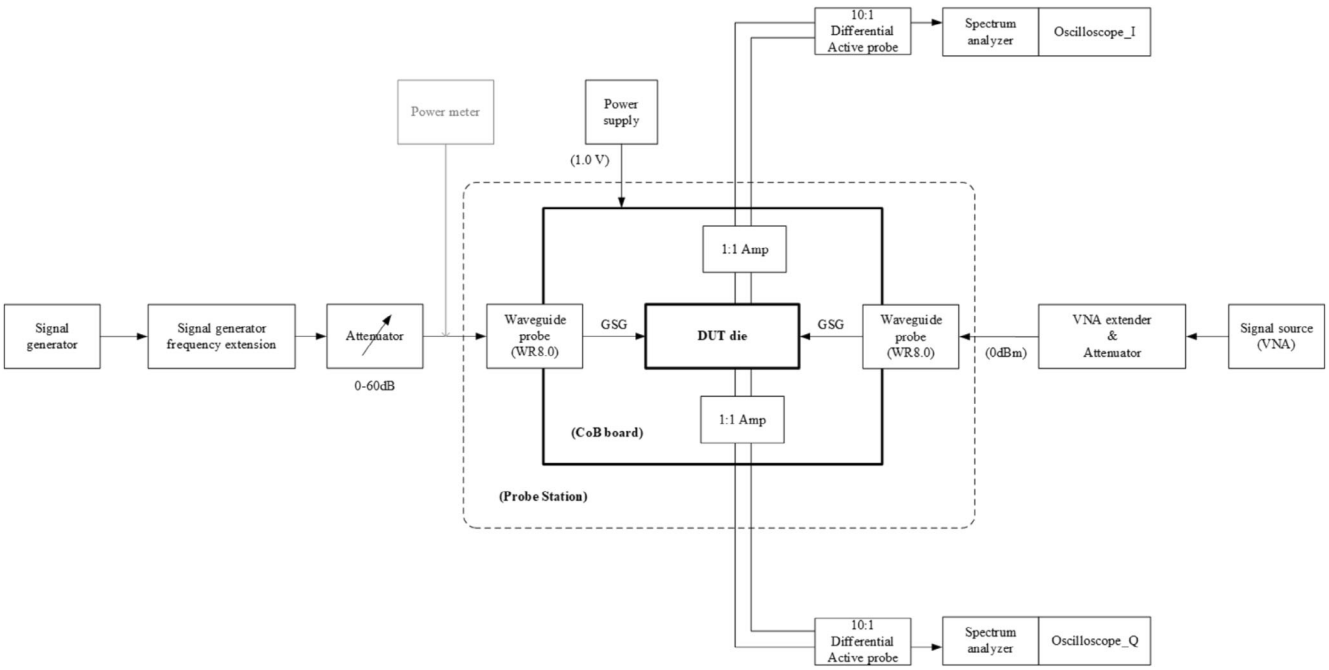

FIGURE 6 Measurement setup for conversion gain, P1dB, I/Q gain, and phase mismatch.

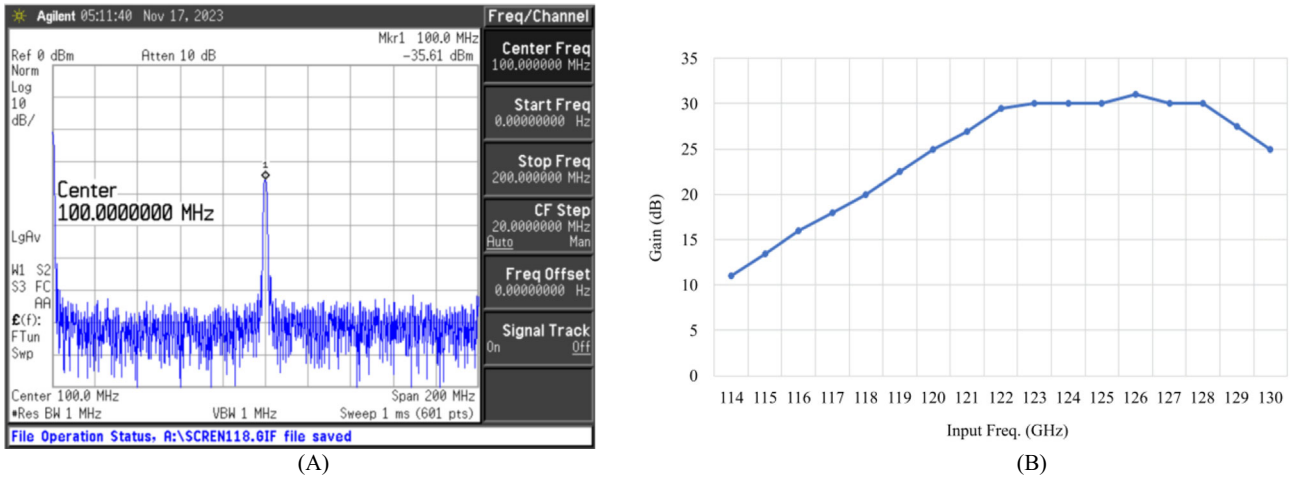

FIGURE 7 Measured gain characteristics of receiver front end: (A) output spectrum (RFin = −45 dBm @122.1GHz, LOin = 0 dBm @122 GHz, output by 10:1 active probe) and (B) conversion gain versus input frequency of RF receiver front end.

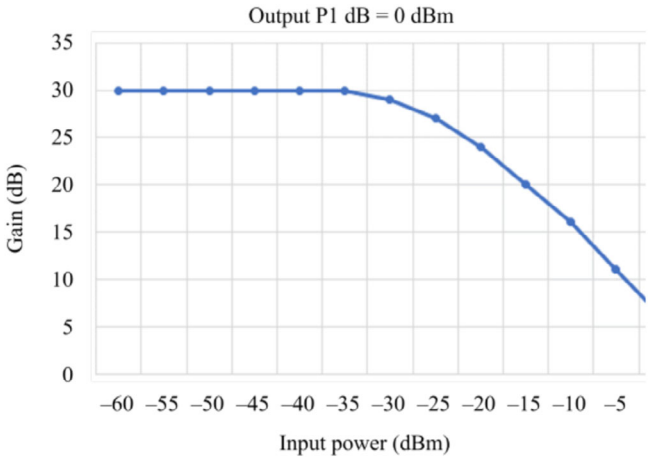

FIGURE 8 Measured gain versus input power of RF receiver front end. (RFin = 122.1 GHz, Loin = 122 GHz).

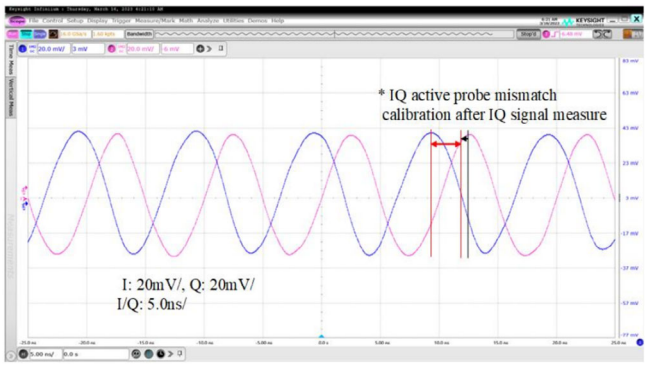

FIGURE 9 Measured 100 MHz I/Q output of the RF receiver front end.

quadrature LO generation, including quadrature voltage-controlled oscillators (VCOs), VCOs combined with RC or LC polyphase filters, and hybrid I/Q couplers, these approaches are generally complex and less suitable for the sub-THz frequency band because of their high frequency and circuit complexity. In contrast, the RC polyphase filter offers a straightforward structure that is relatively easy to implement. The proposed RC polyphase filter employs a single-stage structure capable of supplying sufficient LO power to a passive mixer. Figure 5B presents the electromagnetic (EM)-simulated I/Q phase response of the designed I/Q LO generator [7–22].

4 | MEASUREMENT RESULTS

Figure 6 presents the measurement setup for the conversion gain, P1dB, and I/Q mismatch. To measure the conversion gain and P1dB, 125-GHz-band RF input and LO input signals were generated using a frequency multiplier connected to a signal generator. The frequency-multiplied RF input signal was delivered to a waveguide probe via a controllable RF attenuator. The baseband signal was measured using a 10:1 differentially active probe.

Figure 7A illustrates the measured output power of −35 dBm from the RF receiver front end under conditions with RFin = −45 dBm at 122.1 GHz and Loin = 0 dBm at 122 GHz. Figure 7B presents the measured conversion gain versus the input frequency of the RF receiver front end. The 3 dB bandwidth spans the frequency range of 121 GHz to 129 GHz.

Figure 8 presents the measured gain versus the input power of the receiver front end.

FIGURE 10 Measurement setup for the noise figure.

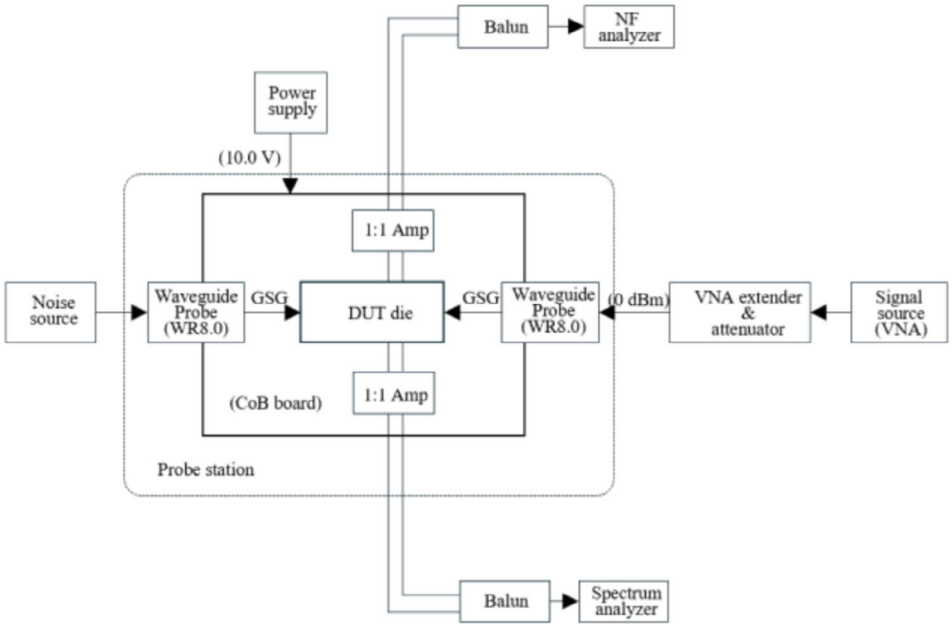

Figure 9 presents the measured 100 MHz I/Q output of the RF receiver front end. In this study, two types of chips were fabricated for testing I/Q LO generation. One chip used the same component values for all resistors in the RC polyphase filter, whereas the other varied the values for the I and Q resistors. The results in Figure 9 were obtained from the test chip with identical component values for all resistors in the RC polyphase filter. The measured gain and phase mismatches between channels I and Q were 0.1 dB and 3.6°, respectively. The measurement results presented in Figure 11 include the I/Q phase offset of the I/Q differential active probes, with the inherent I/Q phase offset subtracted from the final measurement results.

Figure 10 presents the noise figure measurement setup. For noise figure measurements, a commercial noise source was connected to the input side of the LNA. Figure 11 presents the measured single-sideband noise figure of the RF receiver front end. The 1.2 dB value for the waveguide probe (GGB ind. Model 140) is included in the measured noise figure. The resultant double-sided band noise figure was 11.4 dB after de-embedding the probe loss to evaluate the chip's intrinsic performance. The bandwidth of the output intermediate-frequency band was reduced due to the parasitic effects of the 1:1 amplifier and printed circuit board.

Table 2 summarizes the results of PVT simulations, as well as experimentally measured results, and compares them with the results reported in previous studies. The

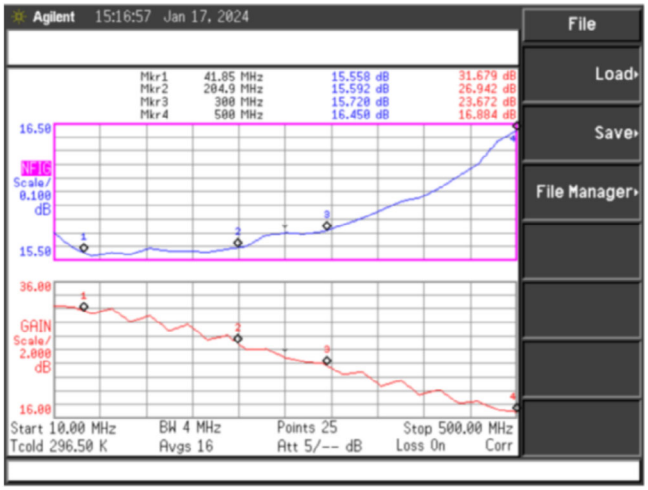

FIGURE 11 Measured single-sideband noise figure of the RF receiver front end.

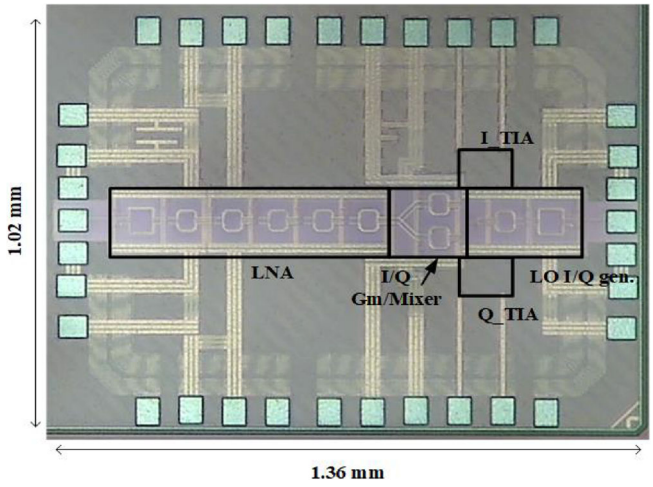

FIGURE 12 Die microphotograph of the 120-GHz-band RF receiver front end.

TABLE 2 Summary of measurement results and comparisons.

	0.35 um SiGe Bipolar [12]	28 nm CMOS [13]	65 nm CMOS [14]	40 nm CMOS [15]	22 nm FinFET [16]	This work (40 nm CMOS)	
						PVT sim. (FF/TT/SS)	Mea.
Supply voltage (V)	3.3	1.0/1.5	1.7/1.0	-	1.0	**1.0**	**1.0**
Frequency (GHz), 3 dB BW	122	102–129	110–125	120	140	**–/118–129/–**	**121–129**
RX gain (dB)	23	39	27.5	28.2	15	**34/33/31**	**30**
NF (dB)	14	8.4	12.7	10.8	12.4	**9.5/9.7/10.5**	**11.4 (DSB)**
Loss of LO driver & IQ gen. (dB)	-	-	-	-	-	**5/5.5/7.5**	-
RX IQ imbalance gain (dB), phase (degree)	-	-	-	-	-	**0.14,1/0.05,2.5/1.7, 9**	**0.1, 3.6**
Input P1dB (dBm)	−9	−35.8	−31	-	−14.8	-	**−30**
Power cons. (mW)	495	51	174	153.4	123	**84/78/61**	**80**
Area (mm^2)	6	0.89	3.06	1.52	0.7	-	**0.22**

chip was integrated using 40 nm CMOS technology, and the total current consumption of the RF receiver front end was approximately 80 mA with a 1.0 V supply voltage.

Figure 12 presents a microphotograph of the integrated chip, which occupies a core area of 0.22 mm^2. All I/O pads for the IF signals and power supply, except for the LO and RF inputs, were protected using standard electrostatic discharge cells.

5 | CONCLUSION

This paper presented a 125-GHz band RF receiver front end designed for radar applications using 40 nm CMOS technology. The receiver front-end chip integrates a five-stage single-to-differential low-noise amplifier, transconductance I/Q driver, quadrature I/Q passive mixer, quadrature I/Q transimpedance amplifier, single-to-differential LO driver, and quadrature I/Q LO generator.

The front-end chip of the RF receiver achieved a conversion gain of 30 dB with a 3 dB bandwidth in the frequency range of 121 to 129 GHz. It exhibits an input P1dB of −30 dBm and a measured double-sideband noise figure of 11.4 dB. The measured gain mismatch and phase mismatch between the I and Q channels are 0.1 dB and 3.6°, respectively. The chip operates with a current consumption of 80 mA with a 1 V supply voltage and occupies a compact core chip size of 0.22 mm^2.

ACKNOWLEDGMENTS

This work was supported by an Institute of Information and Communications Technology Planning and Evaluation (IITP) grant funded by the Korean government (MSIT) (No.2022-0-01016, Development of ultra-precision low-cost sub-THz pulse-based radar chip).

CONFLICT OF INTEREST STATEMENT

The authors declare that there are no conflicts of interest.

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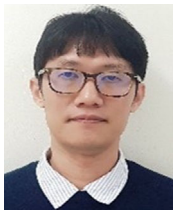

Dong-Woo Kang received his BS degree, MS degree, and PhD in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea in 2001, 2003, and 2007, respectively. From September 2007 to September of 2010, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla, CA, USA. From 2010 to 2013, he worked for the Samsung DMC R&D Center, Suwon, Republic of Korea. Since May 2013, he has been with the Electronics and Telecommunications Research Institute. His research interests include CMOS ICs for millimeter wave and terahertz circuits and systems.

Bon-Tae Koo received his MS degree in Electrical Engineering from Korea University, Seoul, Republic of Korea in 1991. In 1991, he worked with the System Semiconductor Division, Hyundai Electronics Company, Ichon, Korea, where he was involved in the chip design of the video codec and DVB modem. From 1993 to 1995, he worked with HEA, San Jose, USA, where he was responsible for designing the MPEG2 video codec chip. From 1996 to 1997, he worked with TVCOM, Sandiago, USA to design the DVB modem chip. In 1998, he joined Dongbu Electronics as a team leader with the System Semiconductor Lab and focused on the methodology of semiconductor chip design. In 1999, he joined the Application SoC team at ETRI, where he was a team leader, and his research activities included the chip design of MPEG4 video, T-DMB receiver, LTE femtocell modem, and DSP processor. In 2016, he joined the RF research group at ETRI, where he is currently the project leader. His research activities focus on millimeter-wave AI radars.

How to cite this article: S.-H. Han, D.-W. Kang, and B.-T. Koo, *125-GHz-band RF receiver front end using 40 nm complementary metal–oxide–semiconductor technology*, ETRI Journal **48** (2026), 723–730, DOI 10.4218/etrij.2025-0176.