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Comparative study of planar-gate and T-gate GaN HEMTs with gate length scaling

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ABSTRACT

This study compares planar-gate and T-gate GaN high-electron-mobility transistors with gate lengths scaled from 450 to 60 nm. The effects of gate length scaling and gate geometry on DC and RF performance are systematically evaluated. Both structures show increasing drain current and transconductance with scaling until short-channel effects become pronounced near 100 nm, where threshold-voltage roll-off and increased drain-induced barrier lowering are observed. The T-gate devices exhibit superior RF performance, reaching cutoff and maximum oscillation frequencies of 83 and 127 GHz, respectively, at 60 nm, compared with 47 and 79 GHz for the planar-gate devices at 100 nm. The T-gate also shows lower extrinsic capacitance of 0.48 pF/mm and a shorter delay time of 1.9 ps. These results confirm that the T-gate offers stronger immunity to short-channel effects than the planar-gate structure, maintaining excellent RF performance even under aggressive gate length scaling.

1. Introduction

The continuous evolution of wireless communication, radar and satellite systems toward higher frequencies and greater data throughput demands power devices with the capability of delivering high gain, high efficiency, and thermal robustness under extreme operating conditions [1]. In these advanced systems, the RF performance of the transistor—typically characterized by its cut-off frequency (f_T) and maximum oscillation frequency (f_{max})—serves as a key determinant of overall system capability. The enhancement of these RF characteristics allows for faster signal amplification and wider bandwidth, which directly contribute to higher transmission efficiency and reduced power consumption at the circuit and system levels. In this context, GaN-based high-electron-mobility transistors (HEMTs) have emerged as key enabling devices due to their superior electron mobility and high breakdown electric field, which together enable high-power and high-frequency operation [2,3]. To fully exploit these advantages of GaN, systematic investigations on gate length (L_G) scaling and gate structure optimization are required, as these are two critical factors governing the high-frequency behavior of GaN HEMTs [4,5].

L_G scaling plays a pivotal role in enhancing the intrinsic speed of GaN HEMTs by directly affecting carrier transit time, transconductance, and parasitic delay components. However, aggressive scaling also intensifies short-channel effects (*SCEs*), potentially degrading device performance. In addition to L_G scaling, gate structure significantly influences RF characteristics through gate resistance (R_G) and parasitic capacitances (C_{gs} and C_{gd}) [6]. A conventional planar-gate (P-gate) design offers fabrication simplicity but suffers from high parasitic capacitance, limiting f_T and f_{max}. In contrast, the T-gate architecture mitigates parasitic capacitance. While numerous studies have separately investigated L_G scaling or gate structure optimization [7–13], comprehensive analyses considering both factors remain limited. Therefore, a systematic comparison is needed to clarify their combined influence on device performance.

In this work, we present a comparative study of P-gate and T-gate GaN HEMTs with L_G scaling to elucidate how gate geometry and dimensional scaling collectively influence DC and RF performance. This provides a deeper understanding and identifies optimal geometric configurations for achieving high-performance GaN HEMTs applicable to millimeter-wave and high-power electronic systems.

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2. Fabrication

The epitaxial structure was grown on a SiC substrate and consisted of a 1 nm GaN cap, 20 nm $Al_{0.3}Ga_{0.7}N$ barrier, 160 nm GaN channel, and 1.8 μm Fe-doped AlN buffer. The source and drain ohmic contacts were formed by electron-beam evaporation of Ti/Al/Ni/Au, followed by rapid thermal annealing at 850 °C for 30 s. Device isolation was achieved through phosphorus ion implantation, after which a 60 nm 1st SiN layer was deposited using plasma-enhanced chemical vapor deposition. Contact via for the source and drain electrodes were opened by reactive ion etching, and Ti/Au was deposited to complete the metal pads. The gate region was defined by electron-beam lithography, and the underlying 1st SiN was selectively etched using inductively coupled plasma with a CF_4-based chemistry. Subsequently, P-gate and T-gate structures were fabricated by electron-beam lithography and metal deposition, following procedures described in Ref. [14]. Finally, the devices were passivated with 2nd SiN and via were opened for electrical access. The fabricated devices used in this study had the following dimensions: gate width (W_G) = 2 × 100 μm, gate length (L_G) = 60, 100, 150, 250, and 450 nm, and source to drain spacing (L_{SD}) = 4 μm. A cross-sectional schematic of (a) P-gate and (b) T-gate GaN HEMTs, along with focused ion beam (FIB) cross-sectional images of each gate structure, are shown in Fig. 1.

3. Results and discussion

Fig. 2 shows the transfer characteristics of (a) P-gate and (b) T-gate GaN HEMTs measured at a drain bias (V_D) of 8 V for various L_G ranging from 450 nm to 60 nm. A distinct threshold voltage (V_{TH}) roll-off is observed for both devices as L_G is scaled down. The g_m reaches its peak at L_G = 100 nm and subsequently decreases as *SCEs* become pronounced. Both P-gate and T-gate devices exhibit similar scaling behavior. The I_D measured at V_{TH} + 3 V increases with decreasing L_G and reaches its maximum around L_G = 100 to 150 nm, after which it begins to decline. This trend indicates that while shorter L_G enhance current drivability due to reduced channel resistance and increased carrier velocity, further scaling introduces negative effects that limit the achievable current.

According to G. H. Jessen et al. [15], *SCEs* in GaN HEMTs emerge when the L_G becomes less than approximately five times the barrier thickness ($L_G \leq T_{barrier} \times 5$). Considering that the AlGaN barrier thickness in this experiment is 20 nm, *SCEs* are expected to occur near L_G = 100 nm. At the L_G below this point, the V_{TH} begins to roll-off

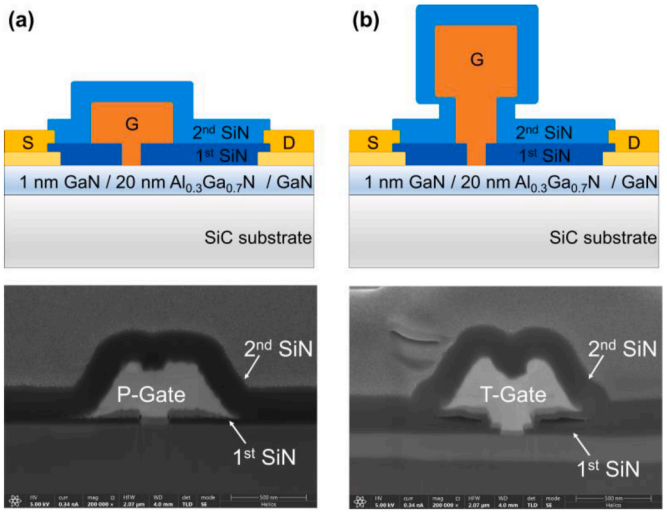

Fig. 1. Cross-sectional schematics of the fabricated (a) P-gate and (b) T-gate GaN HEMTs, along with cross-sectional focused ion beam (FIB) images of each gate structure.

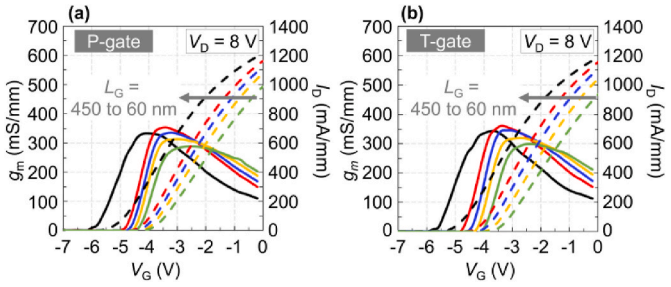

Fig. 2. Transfer characteristics of (a) P-gate and (b) T-gate GaN HEMTs measured at V_D = 8 V.

rapidly, the g_m decreases, and the frequency performance degrades. To analyze these phenomena in more detail, the extracted V_{TH}, g_m, and drain-induced barrier lowering (*DIBL*) are plotted as functions of L_G in Fig. 3 for P-gate and T-gate GaN HEMTs.

As shown in Fig. 3(a), V_{TH} becomes more negative in both devices as L_G decreases, shifting from approximately − 4.0 V at 450 nm to − 5.7 V at 60 nm. The T-gate devices exhibit a slightly higher V_{TH} (by about + 0.2 V) compared to the P-gate counterparts. However, this small difference is likely due to minor variations in epitaxial growth or process conditions rather than inherent structural differences between the two gate types. The drastic negative shift of V_{TH} from L_G = 100 nm confirms the onset of *SCEs*, where the drain electric field penetrates into the

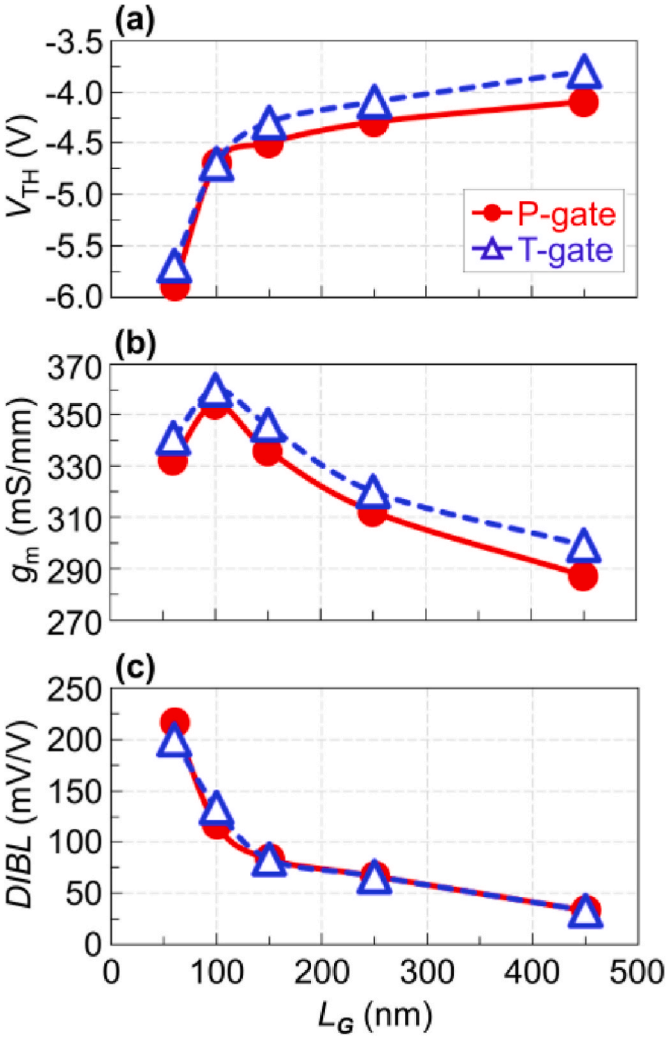

Fig. 3. (a) V_{TH}, (b) g_m, and (c) *DIBL* as a function of L_G.

channel and lowers the potential barrier, thereby weakening gate control. In Fig. 3(b), the g_m increases as L_G is reduced down to approximately 100 nm, reaching a maximum of around 340 to 350 mS/mm, but slightly decreases at 60 nm. This behavior indicates that L_G scaling initially enhances channel modulation and carrier velocity due to stronger electric fields and reduced channel resistance, but excessive shortening L_G leads to negative effects. Across all L_G, the T-gate devices show slightly higher g_m (by about + 10 mS/mm). As confirmed in the FIB cross-sectional images, P-gate electrode is formed across the gate-defined region, which directly contacts the AlGaN barrier, and also extends over the SiN layer on both sides. Consequently, the electrode formed on the SiN layer influences the channel, in addition to the primary gate-defined region. This configuration ultimately causes the electric field within the channel layer to be distributed. Conversely, the major dimension of the T-gate electrode is formed in the gate-defined region, with only a minimal area extending over the SiN layer. This geometry allows the electric field to be concentrated more effectively on the channel, leading to enhanced gate control and a higher g_m. Meanwhile, the *DIBL* characteristics shown in Fig. 3(c) increase significantly as L_G decreases, exceeding 200 mV/V at 60 nm for both devices. No substantial difference in *DIBL* is observed between the P-gate and T-gate devices, suggesting that both structures experience similar levels of *DIBL* at deeply scaled L_G. Overall, these results confirm that the *SCEs* in both P-gate and T-gate GaN HEMTs become pronounced near $L_G = 100$ nm, consistent with the theoretical prediction of $L_G = T_{barrier} \times 5$. While both devices exhibit comparable *DIBL* behavior, the T-gate maintains superior g_m due to its improved field concentration, validating its advantage for high-frequency operation in the short-channel regime.

Fig. 4 shows (a) f_T and (b) f_{max} as a function of L_G for both P-gate and T-gate AlGaN/GaN HEMTs. The RF characteristics were measured using an Agilent N5245A PNA-X network analyzer, and on-wafer open and short patterns were employed to de-embed the parasitic capacitances and inductances. f_T and f_{max} were extracted from the current gain ($|h_{21}|^2$) and the maximum available or stable power gain (*MAG/MSG*), respectively. As expected, f_T and f_{max} increase markedly with decreasing L_G, reflecting enhanced g_m at scaled L_G. For the P-gate devices, f_T increases from approximately 30 GHz at L_G = 450 nm to 47 GHz at 100 nm, whereas the T-gate devices exhibit significantly higher values, reaching 83 GHz at 60 nm. A similar trend is observed for f_{max}, where the P-gate devices achieve 79 GHz at 100 nm, while the T-gate devices reach 127 GHz at 60 nm. The performance gap between the two gate architectures widens as L_G decreases, highlighting the advantage of the T-gate design in mitigating parasitic effects and sustaining high-frequency performance. An interesting observation is that while the P-gate devices show a peak in f_T and f_{max} near L_G = 100 nm followed by a reduction at 60 nm, the T-gate devices continue to exhibit performance improvement down to the $L_G = 60$ nm. This behavior diverges from the DC trend, where both devices showed maximum g_m at L_G = 100 nm before decreasing. The fact that the T-gate maintains rising RF performance despite the drop in g_m suggests that it possesses greater resilience to *SCEs*. The detailed physical mechanisms behind this enhanced *SCEs* immunity will be discussed later.

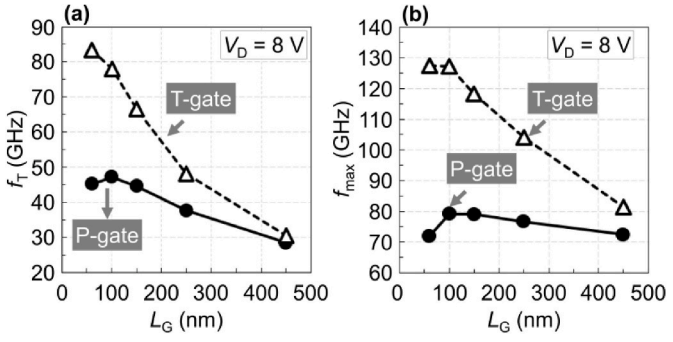

Fig. 4. (a) f_T and (b) f_{max} of P-gate and T-gate GaN HEMTs as a function of L_G.

Fig. 5 shows the RF characteristics of the fabricated devices over a frequency range from 1 to 50 GHz at $V_D = 8$ V. The representative results are presented for the devices exhibiting the highest RF performance: (a) the P-gate device with L_G = 100 nm and (b) the T-gate device with $L_G = 60$ nm. The P-gate device achieved f_T/f_{max} = 47/79 GHz, whereas the T-gate device reached significantly higher values of 83/127 GHz.

Fig. 6(a) shows the variation of f_T as a function of gate bias (V_G) for the P-gate and T-gate GaN HEMTs. As V_G increases, f_T rises, reaches a peak, and then gradually decreases. Both devices exhibit similar bias-dependent behavior, indicating that the linearity of f_T with respect to V_G is nearly identical for the two gate structures. Fig. 6(b) presents the product of $f_T \times L_G$, which serves as an important figure of merit for evaluating the scaling efficiency. For the P-gate, $f_T \times L_G$ decreases from 12.7 GHz μm at L_G = 450 nm to 2.7 GHz μm at $L_G = 60$ nm, while the T-gate decreases from 13.6 GHz μm to 5 GHz μm over the same range. Both P-gate and T-gate devices show a decreasing trend due to the increased influence of *SCEs* and parasitic capacitance. Notably, the T-gate device maintains a higher $f_T \times L_G$ than the P-gate, demonstrating its superior scaling efficiency and stronger immunity to short-channel degradation.

To clarify the physical origin of the superior RF performance of the T-gate and to understand how parasitic effects contribute to the scaling behavior, the parasitic capacitance (C_p) of both devices was further analyzed. Fig. 7(a) shows the equivalent small-signal capacitance, which consists of intrinsic capacitances ($C_{gs.int}$, $C_{gd.int}$) located beneath the gate region and extrinsic capacitances ($C_{gs.ext}$, $C_{gd.ext}$) formed between the gate and the access regions. These parasitic elements play a dominant role in determining the delay time, and the correlation between parasitic components and delay behavior will be analyzed below.

The delay time (τ) can be expressed as [16].

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \tag{1}$$

where τ_t is the carrier transit time under the gate, τ_{ext} is the parasitic charging delay, and τ_{par} represents the parasitic resistance delay associated with the source and drain access regions.

The τ_t can be described as

$$\tau_t = \frac{C_{gs.int} + C_{gd.int}}{g_m} = \frac{L_G}{v_e} \tag{2}$$

$C_{gs.int}$ and $C_{gd.int}$ decrease with L_G scaling, reflecting the reduced overlap area between the gate and the channel region.

The parasitic charging delay is given by

$$\tau_{ext} = \frac{C_{gs.ext} + C_{gd.ext}}{g_m} \tag{3}$$

$C_{gs.ext}$ and $C_{gd.ext}$ remain constant with respect to L_G but become dominant at shorter L_G due to enhanced fringing effects, which significantly

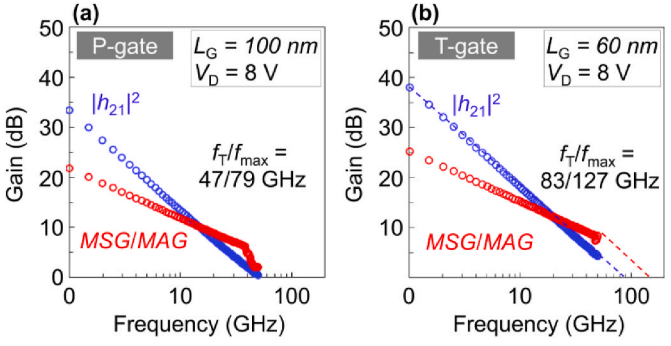

Fig. 5. RF characteristics of (a) P-gate at L_G = 100 nm and (b) T-gate at L_G = 60 nm GaN HEMTs measured at V_D = 8 V.

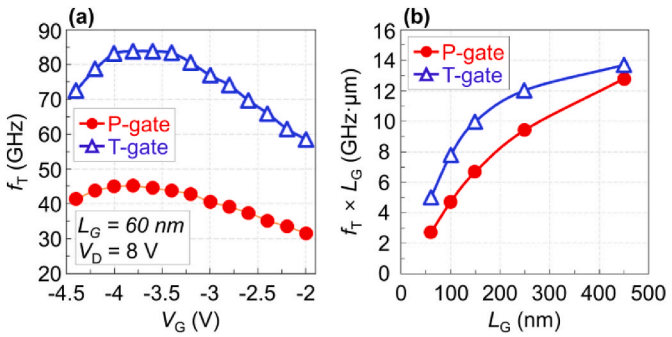

Fig. 6. (a) f_T as a function of V_G and (b) $f_T \times L_G$ as a function of L_G for P-gate and T-gate GaN HEMTs.

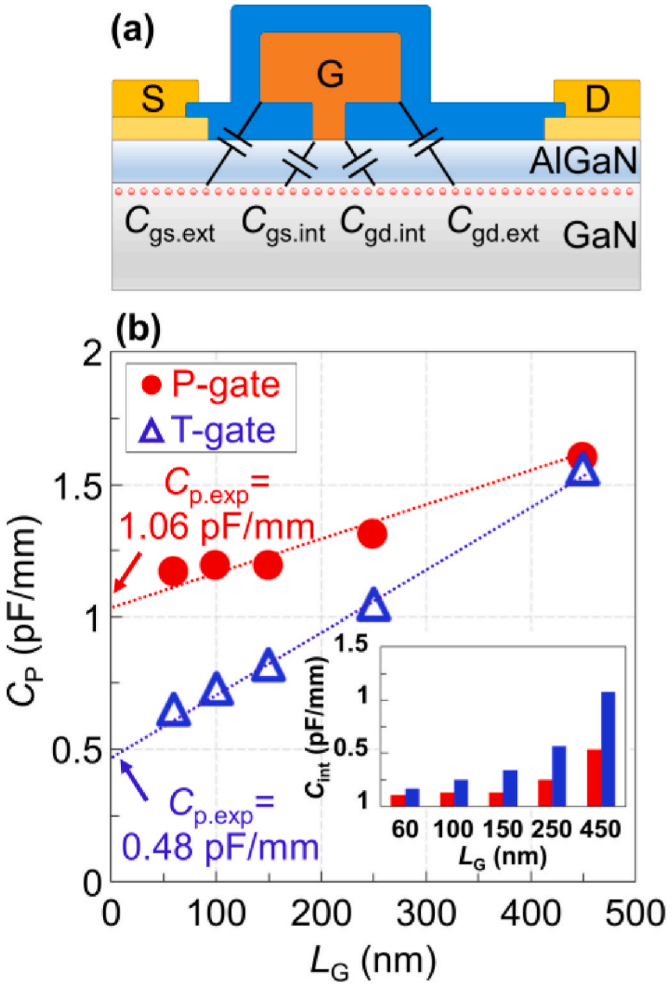

Fig. 7. (a) Equivalent small-signal capacitance and (b) C_P versus L_G for P-gate and T-gate GaN HEMTs. Inset:C_{int} versus L_G for P-gate and T-gate GaN HEMTs.

affect high-frequency performance [17].

The parasitic resistance delay below is mainly associated with R_s as well as R_d.

$$\tau_{par} = C_{gd}(R_s + R_d)\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{g_0}{g_m}\right] \quad (4)$$

As both the P-gate and T-gate devices had the same epitaxial structure and fabrication process, R_s and R_d are identical; hence, this term can be neglected.

Fig. 7(b) shows the parasitic capacitance ($C_p = C_{gs.int} + C_{gd.int} + C_{gs.ext} + C_{gd.ext}$) as a function of L_G. For both devices, C_p decreases linearly with L_G scaling. By linear extrapolation, the intercept at $L_G = 0$ represents the extrinsic parasitic capacitance ($C_{P.ext} = C_{gs.ext} + C_{gd.ext}$). The P-gate devices exhibit a higher $C_{P.ext}$ = 1.06 pF/mm compared to the T-gate with $C_{P.ext}$ = 0.48 pF/mm, indicating that the T-gate structure effectively reduces the capacitance between the gate electrode and the access regions. This reduction in $C_{P.ext}$ can be attributed to the narrower gate footprint and the smaller fringing field coupling of the T-gate head. The inset of Fig. 7(b) shows the variation of intrinsic capacitance (C_{int}) with L_G, derived from $C_{int} = C_P - C_{ext}$. Interestingly, the T-gate exhibits higher C_{int} than the P-gate, even though C_{int} is primarily dependent on L_G. This difference arises from the stronger electric-field coupling in the T-gate geometry. The narrow gate foot and the overhanging T-head concentrate the electric field more effectively into the channel region, enhancing charge modulation and increasing the intrinsic gate-to-channel capacitance. In contrast, the P-gate, with its planar structure, produces a broader and weaker electric field distribution across the passivation layer, resulting in lower coupling efficiency and smaller C_{int}. As the L_G scales down, C_{int} in the T-gate continues to decrease smoothly, whereas that of the P-gate tends to saturate below 100 nm, reflecting the reduced field control and onset of strong short-channel effects in the planar structure. These results indicate that the T-gate is more robust against RF performance degradation in the short-channel regime. Although both devices exhibit comparable *DIBL*, the reduced parasitic loading of the T-gate helps sustain its high-frequency performance under aggressive L_G scaling.

Fig. 8 summarizes the delay time as a function of L_G extracted using (1). The P-gate devices exhibit longer delay time across all dimensions, decreasing from 5.6 ps at 450 nm to 3.5 ps at 60 nm. Conversely, the T-gate devices consistently maintain shorter delay time, ranging from 5.2 ps at 450 nm to 1.9 ps at 60 nm. This reduction in delay time reflects the effects of smaller C_P, which enable faster RF response behavior.

4. Conclusion

In this study, a comparative analysis of P-gate and T-gate GaN HEMTs was performed to evaluate the combined influence of L_G scaling

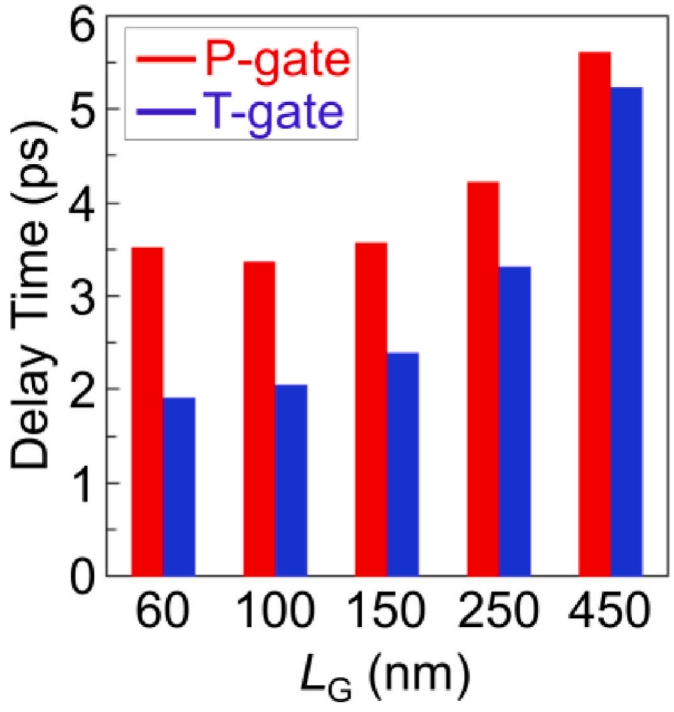

Fig. 8. Delay time as a function of L_G for P-gate and T-gate GaN HEMTs.

and gate geometry on device performance. Both device types exhibited clear *SCEs* near L_G = 100 nm, accompanied by a V_{TH} roll-off, g_m degradation and sharp increase in *DIBL*. The T-gate structure consistently outperformed the P-gate in high-frequency characteristics, achieving maximum f_T/f_{max} = 83/127 GHz at L_G = 60 nm, while the P-gate reached maximum f_T/f_{max} = 47/79 GHz at L_G = 100 nm. Capacitance analysis confirmed that the T-gate device possesses significantly lower $C_{P,ext}$ of 0.48 pF/mm and shorter delay time (1.9 ps). These structural advantages enhance RF performance in the short-channel regime, confirming that the T-gate architecture possesses stronger immunity to *SCEs* than the P-gate design.

This study provides clear experimental evidence that L_G scaling and gate-structure optimization—particularly through the use of a T-gate configuration—is essential for achieving superior frequency response of GaN HEMTs in millimeter-wave and high-power applications.

Declaration of generative AI and AI-assisted technologies in the manuscript preparation process

During the preparation of this work, the authors used ChatGPT (OpenAI) to improve the language and readability of the manuscript. After using this tool, the authors reviewed and edited the content as needed and take full responsibility for the content of the published article.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

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