3-Level Envelope Delta-Sigma Modulation RF Signal Generator for High-Efficiency Transmitters

Yongho Seo, Youngkyun Cho, Seong Gon Choi, and Changwan Kim

This paper presents a 0.13 µm CMOS 3-level envelope delta-sigma modulation (EDSM) RF signal generator, which synthesizes a 2.6 GHz-centered fully symmetrical 3-level EDSM signal for high-efficiency power amplifier architectures. It consists of an I-Q phase modulator, a Class B wideband buffer, an up-conversion mixer, a D2S, and a Class AB wideband drive amplifier. To preserve fast phase transition in the 3-state envelope level, the wideband buffer has an RLC load and the driver amplifier uses a second-order BPF as its load to provide enough bandwidth. To achieve an accurate 3-state envelope level in the up-mixer output, the LO bias level is optimized. The I-Q phase modulator adopts a modified quadrature passive mixer topology and mitigates the I-Q crosstalk problem using a 50% duty cycle in LO clocks. The fabricated chip provides an average output power of −1.5 dBm and an error vector magnitude (EVM) of 3.89% for 3GPP LTE 64 QAM input signals with a channel bandwidth of 10/20 MHz, as well as consuming 60 mW for both channels from a 1.2 V/2.5 V supply voltage.

Keywords: CMOS, envelope delta-sigma modulation, EDSM, power amplifier, polar modulator, RF transmitter, 3GPP LTE.

Manuscript received Feb. 18, 2014; revised July 3, 2014; accepted Aug. 5, 2014.

This work was supported by National Research Foundation of Korea Grant funded by the Korean Government (2009-0065311) and also supported by the ICT R&D Program of MSIP/IITP (14-000-04-001, Development of 5G Mobile Communication Technologies for Hyper-connected Smart Services).

Yongho Seo (syh3039@hanmail.net) and Changwan Kim (corresponding author, cwkim@dau.ac.kr) are with the Department of Electronic Engineering, Dong-A University, Busan, Rep. of Korea.

Youngkyun Cho (ykcho@etri.re.kr) is with the Communications & Internet Research Laboratory, ETRI, Daejeon, Rep. of Korea.

Seong Gon Choi (sgchoi@cbnu.ac.kr) is with the College of Electrical & Computer Engineering, Chungbuk National University, Cheongju, Rep. of Korea.

I. Introduction

In high-data-rate wireless systems, such as 3GPP Long-Term Evolution (LTE) and Worldwide Interoperability for Microwave Access (WiMAX), tremendous efforts to enhance power amplifier (PA) efficiency have led to new transmitter architectures employing a particular 1-bit encoder, such as delta-sigma modulation (DSM) or pulse-width modulation (PWM) [1]–[4]. However, due to such encoders having low coding efficiency, excessive power loss and efficiency degradation cannot be avoided. To enhance the cording efficiency of an encoder, we previously proposed the new transmitter architecture [5] shown in Fig. 1. In Fig. 1, a multilevel envelope delta-sigma modulation (ML-EDSM) scheme is used to enhance the coding efficiency using a 3-level (zero, $A(t)_{max}/2$, and $A(t)_{max}$) envelope signal instead of a conventional 2-level signal. However, 3-level envelope modulation can degrade the PA efficiency, as the PA cannot operate in a saturated region under a single supply voltage for a middle-level envelope signal $A(t)_{max}/2$. To overcome this problem, a dual-supply injection method is applied in the PA,

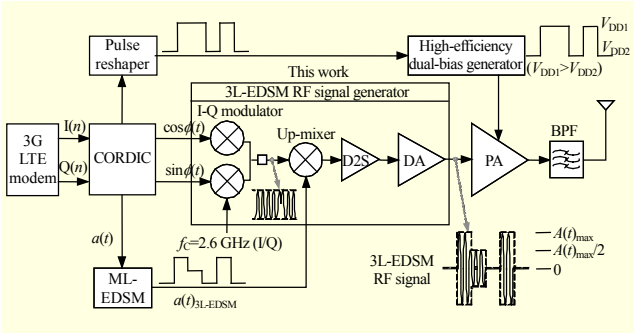


Fig. 1. Block diagram of proposed transmitter in [5].

as shown in Fig. 1. For the maximum-level envelope signal, $A(t)_{max}$, the PA operates in the saturated region under a high supply voltage of V_{DD1}. However, when $A(t)_{max}$ becomes $A(t)_{max}/2$, the dual-supply network switches V_{DD1} ($V_{DD1} > V_{DD2}$) to the low supply voltage of V_{DD2} concurrently. Accordingly, the PA can always operate in the saturated region for the 3-level envelope signal, avoiding any degradation of its efficiency. Finally, the proposed transmitter can achieve high encoding efficiency without degradation of the efficiency of the PA, leading to a new alternative for the implementation of high-efficiency transmitters.

This paper proposes a 2.6 GHz 3-level EDSM RF signal generator for the previously proposed PA architecture in [5], which is implemented in 0.13 μm CMOS technology. It consists of an I-Q phase modulator, a Class B wideband buffer, an up-conversion mixer, a differential-to-single-ended signal converter (D2S), and a Class AB wideband driver amplifier (DA). In Fig. 1, the envelope signal, $a(t)$, is converted to a 3-level PWM signal by an ML-EDSM for higher coding efficiency, while the baseband I-Q phase signals, $\cos\phi(t)$ and $\sin\phi(t)$, are up-converted into a pure phase-modulated 2.6 GHz signal by an I-Q phase modulator. Using these two signals, an up-conversion mixer and D2S generate a 3-level EDSM RF signal centered at 2.6 GHz. The 3-level EDSM RF signal is further amplified by a DA and then delivered to a PA. This is the first paper to describe a 3-level EDSM RF signal generator for high-efficiency transmitters.

II. Circuit Design

In Fig. 2, the baseband I-Q phase signals, $\cos\phi(t)$ and $\sin\phi(t)$, which are generated from our Coordinate Rotation Digital Computer (CORDIC), are up-converted into a 2.6 GHz phase-modulated signal by the proposed I-Q phase modulator. The 2.6 GHz phase-modulated signal is used to turn on and turn off the switching transistors of the following up-conversion mixer. The 2.6 GHz quadrature LO tones for the I-Q phase modulator are provided from an internal divide-by-two circuit. The proposed I-Q phase modulator adopts a double-balanced quadrature passive mixer topology to minimize LO leakage and so as to have low distortion. However, due to no reverse isolation in the passive mixer, an I-Q crosstalk problem occurs since one mixer switch from the I channel and the other mixer switch from the Q channel are simultaneously operating at any given moment [6]–[7]. To mitigate the I-Q crosstalk problem, instead of an LO-2LO mixer [6] or a 25% duty-cycle passive mixer [7], a passive mixer topology (described in [8]) has been modified and then used in this work. The LO-2LO mixer and 25% duty-cycle mixer need additional circuits, such as LO buffers and LO clock generators. This leads to additional dc current consumption and chip area. In the proposed mixer, shown in Fig. 2, for conventional 50% duty-cycle LO clocks, two switches are connected in series to form an AND function to achieve an effective 25% duty-cycle switching. Thus, I and Q channels cannot be connected at the same time, which is the same condition of the 25% duty-cycle mixer. Accordingly, the proposed passive mixer can eliminate the I-Q crosstalk problem without additional circuit blocks or dc power consumption.

To drive the up-conversion mixer effectively, the phase-modulated signal is further amplified by a wideband buffer, which has a 3-bit gain-control function. Since the phase-modulated signal has a constant envelope, the proposed wideband buffer is Class B biased, which leads to low dc

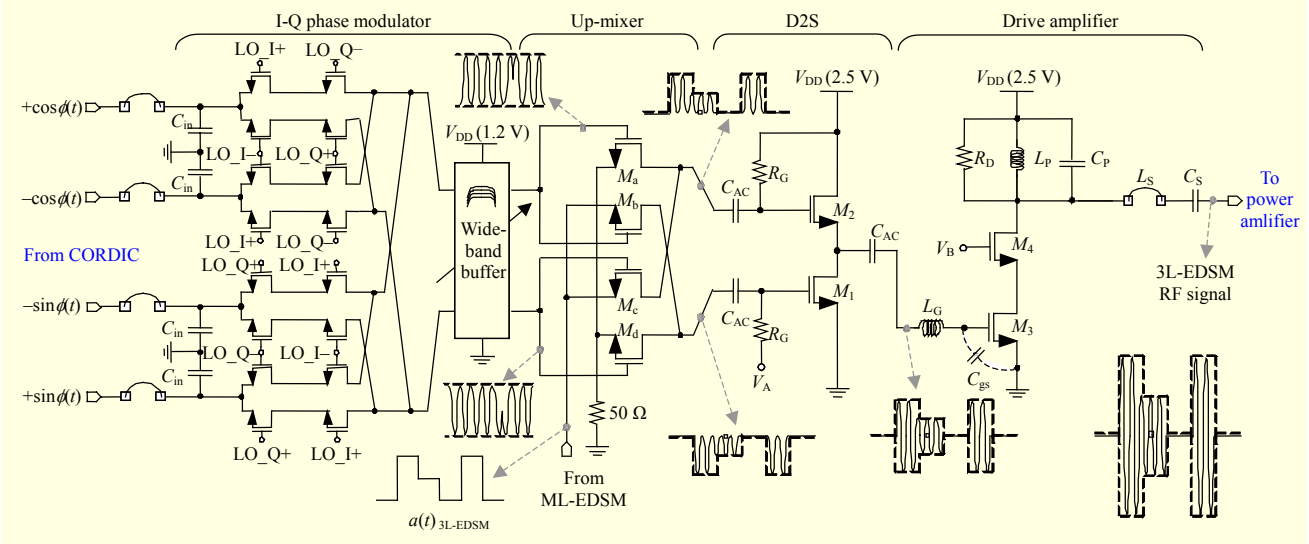


Fig. 2. Schematic diagram of proposed 3L-EDSM RF signal generator.

power consumption. In addition, to preserve fast phase transitions in the output waveform, the wideband buffer uses an RLC resonant load to achieve a bandwidth of 1.5 GHz centered at 2.6 GHz.

In Fig. 2, the second stage is the up-conversion mixer (M_a, M_b, M_c, and M_d), which synthesizes the 3-level EDSM RF signal by using two input signals: a *single-ended* 3-state (0 V, 0.25 V, and 0.5 V) PWM signal from the ML-EDSM circuit and a *differential* 2.6 GHz phase-modulated signal from the I-Q phase modulator. To minimize LO leakage, the up-conversion mixer is designed on a double-balanced passive mixer topology, as shown in Fig. 2. However, since the 3-level PWM input signal is provided as a single-ended signal in our transmitter, one input is connected to the output of the ML-EDSM, but the other is connected to a 50 Ω resistor for circuit balancing, which is equal to the output impedance of the ML-EDSM circuit. In Fig. 2, for the 3-level (0 V, 0.25 V, and 0.5 V) PWM input signal, to achieve an accurate 3-state envelope level in the up-mixer output waveform, the magnitude from the first level (0 V) to the second level (0.25 V), A, and the magnitude from the second level (0.25 V) to the third level (0.5 V), B, should be equal. To ensure that the ratio A/B is equal to one, the relation between the gate dc-bias level of the up-mixer (M_a, M_b, M_c, and M_d), $V_{LO,dc}$, and the magnitude of the LO amplitude, $V_{LO,pp}$, has been evaluated, as shown in Fig. 3. Figure 3 shows the ratio A/B becomes one at $V_{LO,dc}$ = 0.66 V for LO amplitudes from 500 mV_{PP} to 1 V_{PP}, which can be practically achieved from the proposed wideband buffer. Even if $V_{LO,pp}$ is smaller than 500 mV_{PP}, the ratio A/B = 1 can be maintained by digitally controlling $V_{LO,dc}$. Finally, by adopting $V_{LO,dc}$ = 0.66 V, the ratio A/B = 1 can be guaranteed in the proposed up-conversion mixer.

In Fig. 2, to achieve a single-ended 3-level EDSM RF signal, the differential output signal of the up-conversion mixer should be extracted by a D2S. The D2S can be located at the output of the up-conversion mixer or at the output of the DA. If the D2S is located at the output of the DA, then large signals amplified by the DA cannot be accommodated in the D2S. As a result, the 3-state envelope level can be seriously distorted at the D2S output. In addition, the DA should be designed as a differential topology, which consumes twice the dc power consumption and die area compared to the single-ended DA. Accordingly, the proposed D2S directly follows the up-conversion mixer in this work, as shown in Fig. 2. The proposed D2S is made up of a combination of a common-drain (CD) amplifier, M_2, and a common-source (CS) amplifier, M_1, where M_1 and M_2 are realized using thick-oxide MOSFETs to permit a high voltage swing under a 2.5 V supply voltage. To make the 3-level EDSM RF signal fully symmetric up and down at the D2S output, the voltage gains of the two amplifiers are made almost

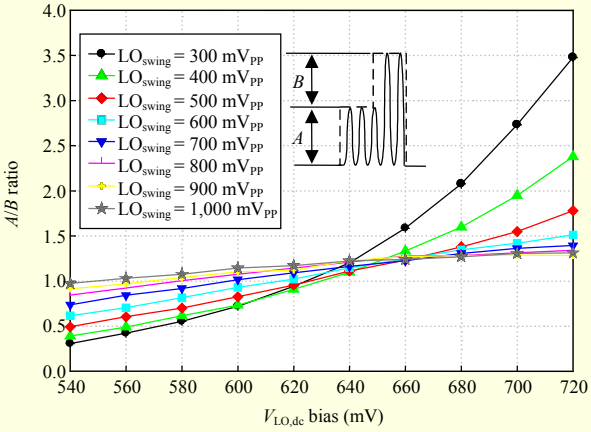
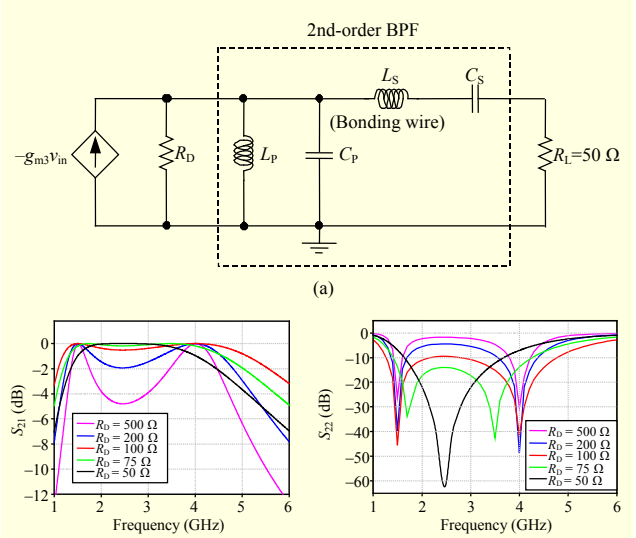


Fig. 3. Relationship between LO bias level and LO amplitude.

the same by optimizing the size of their input transistors, M_1 (W/L = 60 μm/0.35 μm) and M_2 (W/L = 50 μm/0.35 μm). The proposed DA is a single-ended Class AB cascode CS amplifier (M_3 and M_4) with a 1 dB output compression point (OP_{1dB}) of +10 dBm. It can provide an average output power level of +0 dBm due to a peak-to-average power ratio (PAPR) of 10 dB. In Fig. 2, the input transistor M_3 is Class AB biased for high efficiency, and the cascode transistor M_4 is realized in thick-gate NMOS for high output voltage swing. To prevent any phase-transition distortion or spectral regrowth, the DA has been designed to achieve both enough bandwidth and high linearity [9]. Our simulation results show that the required bandwidth is more than four times the ML-EDSM's sampling frequency of 522.24 MHz.

Previously reported wideband amplifiers are dominated by three different topologies: shunt-feedback, shunt-peaking, and distributed amplifiers. The shunt-feedback amplifier [10] provides respectable wideband matching and flat gain but suffers from large dc power dissipation. The shunt-peaking amplifiers [11]–[12] can also provide flat gain over a wide frequency band, but they cannot provide high output power due to a voltage drop across a resistive load. The distributed amplifiers [13]–[14] tend to consume a large amount of dc current due to the distribution of multiple amplifying stages. In Fig. 2, to achieve broadband gain characteristics and 50 Ω output matching to an external PA, the proposed DA adopts a second-order band-pass filter (BPF) as its load, which consists of L_P, C_P, L_S, and C_S. Here, L_S and L_p are realized by a bonding wire inductance and on-chip spiral inductor, respectively, and C_S is an off-chip capacitor. The parasitic capacitance by the output pad is included in C_P. For clarity, Fig. 4(a) shows the small-signal equivalent circuit for the output part of the overall DA, where $-g_{m3}v_{in}$ and R_D represent the small-signal output current and resistive load of the DA, respectively, and

ETRI Journal, Volume 36, Number 6, December 2014
http://dx.doi.org/10.4218/etrij.14.0114.0176



R_D (Ω)	R_L (Ω)	C_P (pF)	L_P (nH)	C_S (pF)	L_S (nH)
50	50	1.27	3.31	1.32	3.18
75		0.86	4.90	1.32	3.18
100		**0.63**	**6.63**	**1.32**	**3.18**
200		0.55	7.65	0.76	5.53
500		0.38	10.9	0.44	9.54

(b)

Fig. 4. Characterization of DA: (a) small-signal equivalent circuit and (b) theoretical values of the BPF parameters and simulated curves according to the various values of R_D (50 Ω, 75 Ω, 100 Ω, 200 Ω, and 500 Ω). Here, R_D represents the resistive load of DA.

R_L = 50 Ω represents an input impedance of the following PA. As Fig. 4(a) demonstrates, the small-signal equivalent circuit for the output of the DA is exactly the same as the second-order BPF topology. Figure 4(b) shows the theoretical values of the BPF parameters and simulated frequency-response curves according to various values of R_D for a targeted −3 dB bandwidth of 2.5 GHz (that is, 1.5 GHz to 4 GHz) for R_L = 50 Ω. In Fig. 4(b), when R_D = 50 Ω, the BPF shows the best wideband gain curve (S_{21}) and broadband 50 Ω matching (S_{22}). In addition, since the quality factor Q of the BPF is small due to R_D = 50 Ω, the output voltage swing at the drain of M_4 is small, which leads to improvement of the DA linearity. However, to achieve an OP_{1dB} of +10 dBm, the transconductance g_{m3} of the input transistor M_3 should be increased due to the small value of R_D, which leads to high dc power consumption. Thus, considering dc power consumption, wideband characteristics, and linearity, the R_D of 100 Ω has been chosen for the proposed DA. As shown in Fig. 4(b), though R_D = 100 Ω is not matched to R_L = 50 Ω, S_{21} still shows a −3 dB bandwidth from 1.5 GHz to 4 GHz and S_{22} is less than −10 dB over the same frequency range. In addition, because the output voltage swing at the DA is not very wide due to R_D = 100 Ω, the cascode transistor M_4 can operate in the saturation region while the proposed DA delivers its maximum output power of +10 dBm. The proposed DA, under maximum-power operation, draws a dc current of 13.5 mA from a 2.5 V supply voltage. Finally, the proposed DA with the second-order BPF can achieve high output power, flat gain, and broadband output matching, while consuming moderate dc power consumption.

Although the proposed BPF can provide a wide bandwidth at the DA output, a gain reduction may occur at a high frequency range due to unexpected parasitic capacitances. To mitigate this problem, a series-peaking on-chip spiral inductor, L_G, is used to tune out the gate-source capacitance, C_{gs}, of M_3 at 3.5 GHz to give more amplification to the input signal. Finally, the proposed DA provides an overall bandwidth of 3 GHz centered at the 2.6 GHz carrier frequency.

III. Measurement Results

The proposed 3-level EDSM RF signal generator has been implemented in 0.13 μm CMOS technology, as shown in Fig. 5. The I-Q phase modulator and wideband buffer consume 6.5 mA from a 1.2 V supply, and the other circuits (up-conversion mixer, D2S, and DA) consume 20.5 mA from a 2.5 V supply.

The fabricated chips were packaged and then mounted on a test board. To apply a 3G LTE input signal to the test board, its phase and envelope signals were separately generated; the baseband I-Q phase signal is provided from a vector signal generator and the 3-level EDSM signal from an ML-EDSM chip, which is not described in this paper but which is also implemented in 0.13 μm CMOS technology. The 2.6 GHz quadrature LO tones for the I-Q phase modulator are provided from an internal divide-by-two circuit by using an external 5.2 GHz signal.

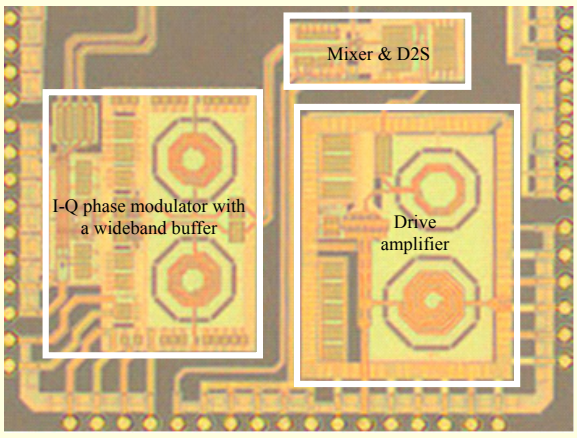


Fig. 5. Chip photograph (core area is 2 mm^2).

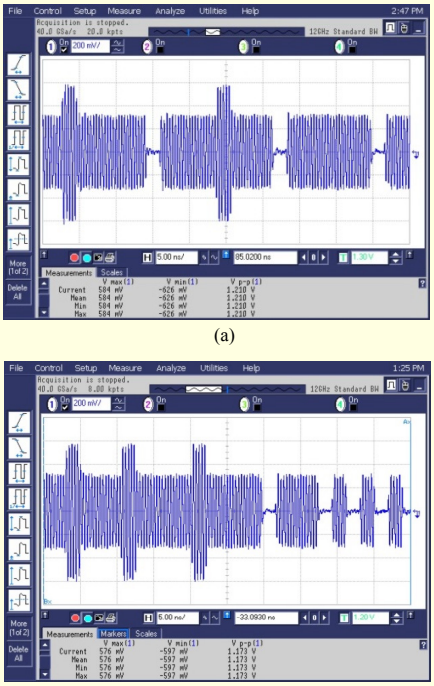


Fig. 6. Probed 3L-EDSM RF signal waveforms for (a) channel bandwidth of 10 MHz and (b) channel bandwidth of 20 MHz.

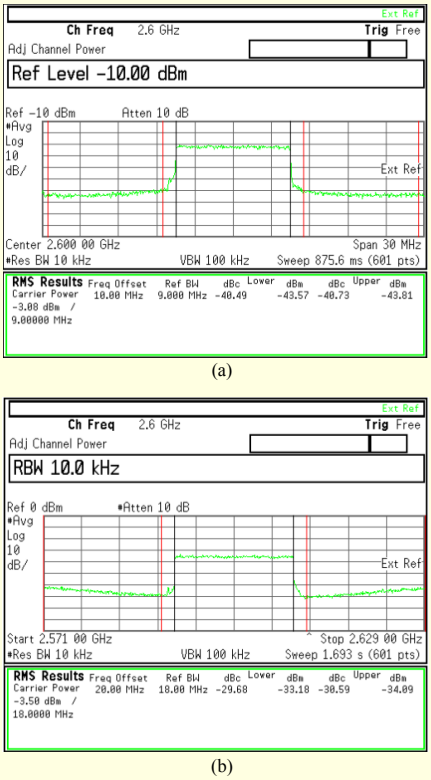


Fig. 7. Output power spectrums for (a) channel bandwidth of 10 MHz and (b) channel bandwidth of 20 MHz.

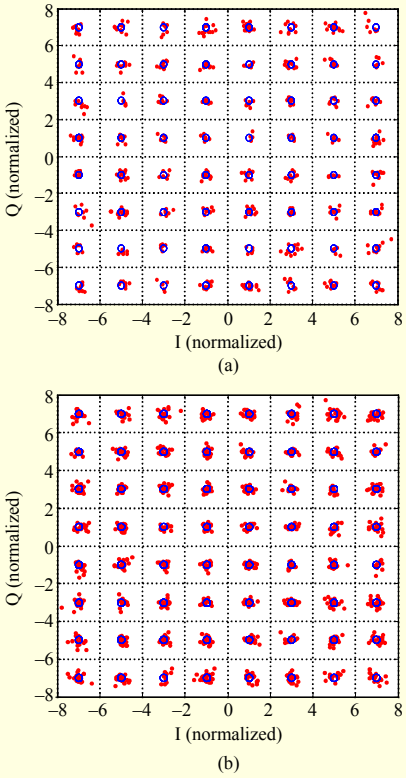


Fig. 8. Measured EVM constellation for (a) channel bandwidth of 10 MHz (EVM = 3.89%) and (b) channel bandwidth of 20 MHz (EVM = 3.89%).

Table 1. Performance summary.

RF carrier frequency		2.6 GHz	
Chip core area		2 mm^2	
Technology		0.13 μm CMOS	
Total dc power consumption		60 mW	
Supply voltage		1.2 V/2.5 V	
3G LTE channel-BW		10 MHz	20 MHz
Channel power (dBm)		–1*	–1.5*
ACLR (dBc)	Lower band	–40.4	–29.6
	Upper band	–40.7	–30.5
EVM of 64 QAM (%)		3.89	3.89

*Cable loss of 2 dB has been calibrated.

Figures 6, 7, and 8 show the measured results of the fabricated chip having a 3G LTE input signal with a channel bandwidth of 10 MHz/20 MHz. The sampling rate of the ML-EDSM is 522.24 MHz. Figure 6 shows the measured time-domain waveforms of the 3-level EDSM RF signal at the DA output. Due to sufficient bandwidth for all the signal paths and an optimized LO biasing level for the up-conversion mixer, the

output waveforms have a sharp phase transition in each envelope level and horizontally symmetrical 3-level envelope variation. Figure 7 gives the measured output power spectrums. In Fig. 7(a), an average output power of –1 dBm (cable loss of 2 dB is calibrated) and an adjacent channel leakage ratio (ACLR) of more than 40 dBc at a 10 MHz offset have been measured for the input 3G LTE signal with a channel bandwidth of 10 MHz. Figure 7(b) shows a measured 20 MHz channel power of –1.5 dBm and ACLR of more than 29.6 dBc at a 20 MHz offset. The ACLR can be further improved by increasing the ML-EDSM's sampling frequency. The measured EVM of 3.89% for both two-channel bandwidths is shown in Fig. 8. The measured results with the 3G LTE signals are summarized in Table 1.

IV. Conclusion

This paper has presented a 3-level envelope delta-sigma modulation (3L-EDSM) RF signal generator, which is implemented in 0.13μm CMOS technology. The measurement results demonstrate that the proposed 3-level EDSM RF signal generator can be adopted for the new PA architecture described in [5]. Finally, the proposed PA architecture with the 3-level EDSM RF signal generator can serve as an alternative for the implementation of high-efficiency transmitters, which are required in high-data-rate wireless systems, such as LTE/LTE-Advanced picocell base station and user equipment, WiMAX, wireless local area network, and so on.

References

[1] Y. Wang, "An Improved Kahn Transmitter Architecture Based on Delta-Sigma Modulation," *IEEE MTT-S Int. Microw. Symp. Dig.*, Philadelphia, PA, USA, vol. 2, June 8–13, 2003, pp. 1327–1330.

[2] M. Nielsen and T. Larsen, "A Transmitter Architecture Based on Delta-Sigma Modulation and Switch-Mode Power Amplification," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 8, Aug. 2007, pp. 735–739.

[3] C. Berland et al., "A Transmitter Architecture for Nonconstant Envelope Modulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 1, Jan. 2006, pp. 13–17.

[4] J. Choi et al., "A Delta-Sigma-Digitized Polar RF Transmitter," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, Dec. 2007, pp. 2679–2690.

[5] J.H. Kim et al., "60% High-Efficient 3G LTE Power Amplifier with Three-Level Delta Sigma Modulation Assisted by Dual Supply Injection," *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, USA, June 5–10, 2011, pp. 1–4.

[6] T. Sowlati et al., "Single-Chip Multiband WCDMA/HSDPA/HSUPA/EGPRS Transceiver with Diversity Receiver and 3G Digital RF Interface without SAW Filters in Transmitter 13G Receiver Paths," *ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 8–12, 2009, pp. 116–117.

[7] X. He and J.V. Sinderen, "A 45 nm Low-Power SAW-less WCDMA Transmit Modulator Using Direct Quadrature Voltage Modulation," *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, Feb. 8–12, 2009, pp. 120–121.

[8] F. Tillman, N. Troedsson, and H. Sjland, "A 1.2 Volt 1.8 GHz CMOS Quadrature Front-End," *Symp. VLSI Circuits Dig. Techn. Papers*, June 17–19, 2004, pp. 362–365.

[9] B. Razavi, *RF Microelectronics,* New Jersey, USA: Prentice Hall PTR, 1998, pp. 91–93.

[10] K.W. Kobayashi, "An 8 W 250 MHz to 3 GHz Decade-Bandwidth Low-Noise GaN MMIC Feedback Amplifier with > +51 dBm OIP3," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, Oct. 2012, pp. 2316–2326.

[11] A. Bevilacqua and A.M. Niknejad, "An Ultrawideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receiver," *IEEE Int. Solid-State Circuits Conf. Dig. Techn. Papers*, San Francisco, CA, USA, Feb. 15–19, 2004, pp. 382–383.

[12] R. Sapawi et al., "Low Group Delay 3.1–10.6 GHz CMOS Power Amplifier for UWB Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 1, Jan. 2012, pp. 41–43.

[13] C.-Y. Hsiao, T.-Y. Su, and S.S.H. Hsu, "CMOS Distributed Amplifiers Using Gate-Drain Transformer Feedback Technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, Aug. 2013, pp. 2901–2910.

[14] K. Moez and M. Elmasry, "A 10 dB 44 GHz Loss-Compensated CMOS Distributed Amplifier," *IEEE Int. Solid-State Circuits Conf. Dig. Techn. Papers*, San Francisco, CA, USA, Feb. 11–15, 2007, pp. 548–549.

Yongho Seo received his BS and MS degrees in electronics engineering from Dong-A University, Busan, Rep. of Korea, in 2009 and 2011, respectively. He is currently working toward his PhD degree at Radio Frequency Integrated Circuit laboratory, Dong-A University. His main research interests are wideband/multiband CMOS RF transceiver design for wireless local area networks and cellular applications.

Youngkyun Cho received his BS degree from Ajou University, Suwon, Rep. of Korea, in 2001 and his MS degree from Pohang University of Science and Technology, Pohang, Rep. of Korea, in 2003, both in electrical and electronics engineering. He is currently with the Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea, as a senior researcher. His research interests are novel devices; mixed signal circuits; Nyquist; and oversampling rate ADCs and transceivers. He was the recipient of the best paper award at the IEEE Nanotechnology Materials and Devices Conference in 2006 and was twice awarded the prize at the National Semiconductor Design Contest in 2009 and 2014.

Seong Gon Choi received his BS degree in electrical engineering from Kyungpook National University, Daegu, Rep. of Korea, in 1990 and his MS and PhD degrees from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1999 and 2004, respectively. Currently, he is an associate professor at the College of Electrical & Computer Engineering, Chungbuk National University, Cheongju, Rep. of Korea. His main research interests are mobile communications; green networks; smart grids (future power grid); and high-speed network architectures and protocols.

Changwan Kim received his BS degree in electrical engineering from the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Rep. of Korea, in 1997 and his MS and PhD degrees in electronic engineering from the Information and Communications University, Daejeon, Rep. of Korea, in 2003 and 2006, respectively. From 2006 to 2007, he worked for the Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea. Since 2007, he has been with the Department of Electronic Engineering, Dong-A University, Busan, Rep. of Korea, where he is now an associate professor. His main research interests are wideband/multiband CMOS RF transceiver design and system-level integration of transceivers.

ETRI Journal, Volume 36, Number 6, December 2014
http://dx.doi.org/10.4218/etrij.14.0114.0176