Effect of Oxygen Binding Energy on the Stability of Indium-Gallium-Zinc-Oxide Thin-Film Transistors

Woo-Seok Cheong, Jonghyurk Park, and Jae-Heon Shin

From a practical viewpoint, the topic of electrical stability in oxide thin-film transistors (TFTs) has attracted strong interest from researchers. Positive bias stress and constant current stress tests on indium-gallium-zinc-oxide (IGZO)-TFTs have revealed that an IGZO-TFT with a larger Ga portion has stronger stability, which is closely related with the strong binding of O atoms, as determined from an X-ray photoelectron spectroscopy analysis.

Keywords: In-Ga-Zn oxide, IGZO, electrical stability, thin-film transistor, XPS, oxygen binding energy.

I. Introduction

Currently, oxide semiconductor-based thin-film transistors (TFTs) have shown desirable electrical properties, such as high mobility at over 10 cm^2/Vs and a low subthreshold swing at below 0.2 V/decade [1] and are thus potential candidates for device applications in 3-D memory and ring oscillators and for use as backplanes in both active matrix organic light emission diodes (AM-OLEDs) and TFT liquid crystal displays [2]-[4]. For real applications of such products, the most important aspect is to guarantee reliability of an oxide-TFT against external electrical stresses.

On the other hand, over the past ten years, the mechanisms responsible for the electrical instability of amorphous silicon-based TFTs have been well clarified, leading to two directions, that is, charge-trapping in the gate insulator and charge-injection at the channel, owing to the breaking of weak Si-Si bonds [5], [6]. A simple analysis of the electrical instability of oxide-TFTs was conducted using the bias-stress-induced and stretched-exponential time dependence of a threshold voltage shift [7], which is an empirical model for explaining the charge-trapping in amorphous Si-TFTs [6].

Instability as a result of the channel composition in zinc-tin-oxide TFTs [8], the effect of the atmosphere on the electrical instability of bottom-gate indium-gallium-zinc-oxide TFTs (IGZO-TFTs) [9], the effect of the process parameters on the electrical stability of IGZO-TFTs, and the effect of the interface roughness on the electrical stability of top-gate IGZO-TFTs [10] have all been reported recently. Additionally, the effects of interfacial dielectric layers on the electrical stability of low-temperature processed IGZO-TFTs have been investigated [11]. The IGZO-TFT with an O_2 plasma-treated SiN_x-based insulator has shown an improved bias stability [12]. In addition, the higher-quality channel made by a proper annealing process has demonstrated greater stability in TFTs [13]. Despite there being a significant amount of data on TFTs, intrinsic research on the degradation of oxide semiconductor-based TFTs is still lacking.

In fact, it may be impossible to generalize the essential characteristics of such a degradation as there are so many factors to be considered, including the channel material and composition, deposition method and condition, gate insulator, interface, annealing condition, and device structure. In addition to considering such parameters, the purpose of this paper is to investigate the effect of channel composition on the electrical stability of IGZO-TFTs. Electrical properties other than stability were previously explored by the following two groups. First, using a combinatorial method, Iwasaki and others extracted the electrical performance of an IGZO-TFT as a function of channel composition, where a greater amount of In_2O_3 existing in a channel leads to a higher mobility, and increasing the oxygen partial pressure during the formation of the IGZO channel moves the threshold voltage (V_{th}) toward the

Manuscript received May 25, 2012; revised Aug. 27, 2012; accepted Sept. 6, 2012.

Woo-Seok Cheong (phone: +82 42 860 5841, cws@etri.re.kr), Jonghyurk Park (eureka99@etri.re.kr), and Jae-Heon Shin (sjh@etri.re.kr) are with the Convergence Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea.

http://dx.doi.org/10.4218/etrij.12.0212.0232

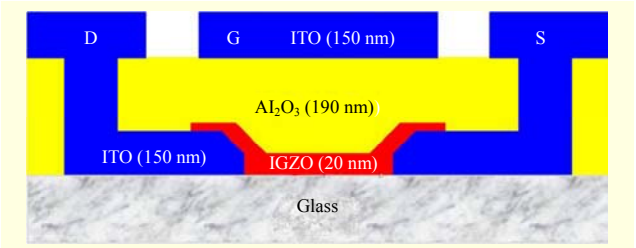

Fig. 1. Schematic description of top-gate IGZO-TFT with Al_2O_3 gate insulator and ITO electrodes (source/drain and gate).

Table 1. Electrical properties of three IGZO-TFTs.

TTFT / Property	A-type	B-type	C-type
Composition ratio (In:Ga:Zn, at%)	2:1:2	1:1:1	2:2:1
Post-annealing temperature (°C)	~ 200	~ 300	~ 400
V_{on} (V)	–1.26	0.21	0.42
V_{th} (V)	2.06	4.76	5.17
μ_{sat} (cm^2/Vs)	18.09	7.90	9.12
Subthreshold swing	0.20	0.26	0.29

positive direction [14]. Next, using several fixed-compositional IGZO targets, the effects of the processing parameters, such as the oxygen partial pressure, deposition pressure, target composition, thickness, and annealing temperature on the electrical properties of IGZO-TFTs, were reported by Barquinha and others, where a very high mobility of ~ 80 cm^2/Vs was achieved [15].

II. Experiment

For this study, three kinds of IGZO targets, In:Ga:Zn, at target ratios of 2:1:2, 1:1:1, and 2:2:1, respectively, are prepared by Advanced Nano Products, Ltd. To exclude both the absorption of O_2/H_2O gases in the atmosphere and damage caused by sputtering, a top-gate TFT structure (staggered type) is chosen. The source/drain and gate electrodes are made using ITO (In_2O_3:SnO_2 = 90:10, weight percent). After the channel deposition, an Al_2O_3 layer as a gate insulator is deposited using atomic layer deposition (ALD) at 150°C.

A schematic illustration of the device is shown in Fig. 1, in which the thicknesses of the IGZO channel, Al_2O_3 gate insulator, and electrode are 20 nm, 190 nm, and 150 nm, respectively. Positive bias stress (PBS) tests are carried out over time at conditions of V_g = 20 V and V_d = 0 V, and constant current stress (CCS) tests are conducted at I_d = 3 μA at room temperature and 60°C.

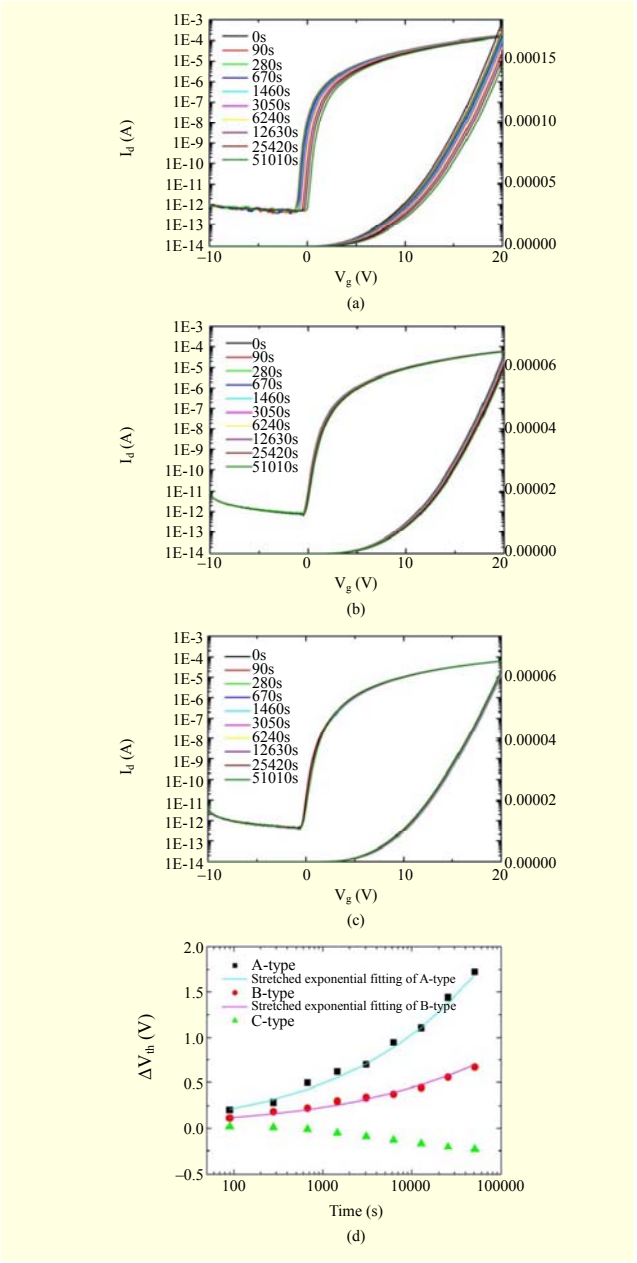

Fig. 2. Results of PBS tests (V_g = 20 V and V_d = 0 V) on three types of IGZO-TTFTs over time, where (a), (b), and (c) show A-type-IGZO (2:1:2), B-type-IGZO (1:1:1), and C-type-IGZO (2:2:1) TTFTs, respectively, and (d) summarizes all three in terms of numerical values, where A- and B-type TTFTs are well fitted with stretched exponential time-dependence model.

III. Results

The electrical properties of IGZO-TFTs are summarized in Table 1, in which the proper annealing temperature is chosen for each device to obtain a minimum hysteresis of below 0.05 V during the forward/backward sweep of the I_d-V_g transfer plot. The C-type device (with higher Ga content) has a little higher

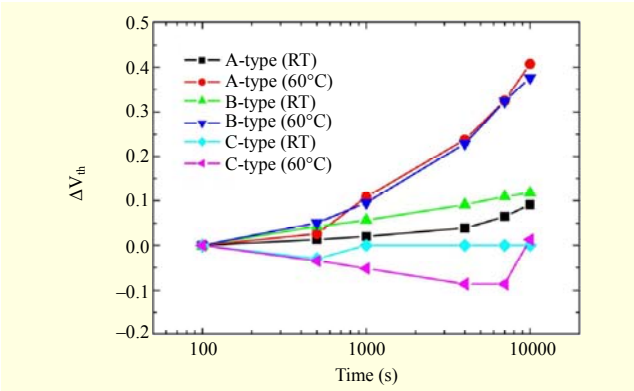

Fig. 3. Results of CCS tests (I_d = 3 μA) at room temperature (RT) and 60°C.

threshold voltage, and lower mobility, which is closely related with strong carrier suppressor, Ga, as reported earlier [17].

From the results of the PBS tests, Figs. 2(a) through 2(c) show a shift in the threshold voltage (V_{th}) of A-, B-, and C-type IGZO-TFTs for 51,010 seconds, which is summarized in Fig. 2(d). The V_{th} shifts of the A- and B-type TFTs are well fitted using a stretched-exponential equation on the instability of TFTs, which can be expressed as follows:

$$\Delta V_{th} = \Delta V_{tho}\left\{1-\exp\left[-\left(t/\tau\right)^{\beta}\right]\right\},$$

where ΔV_{tho} is the threshold voltage shift for infinity, τ represents the characteristic trapping time of the carriers, and β is the stretched-exponential exponent. The value of β for the A- and B-type TFTs is 0.355 and 0.29, respectively. However, for the C-type TFT, the model parameters cannot be extracted because of the negative shift in the threshold voltage. It is unclear why a negative shift occurs during PBS. Based on the ALD method, Jeon and others explained that the negative shift in the transfer plots in ZnO-TFTs is caused by the movement of the hydroxyl groups [16]. In our devices, the sputtering condition of the channels and the fabrication condition of the devices are the same in the A-, B-, and C-type TFTs, which means that the A- and B-types of TFTs have a common source causing a negative shift.

Figure 3 shows the results of CCS tests at both room temperature and 60°C. Similar results are obtained from the A- and B-type TFTs. However, considering that the A-type TFT has a higher mobility than the B-type TFT (thus, the biased voltage is much smaller), the former is stabler than the latter. Commonly, a shift in V_{th} increases with temperature, as the charge-trapping can be accelerated by an increase in the carrier concentration in the channel. The value of V_{th} in the C-type-TFT does not move at room temperature. However, at 60°C, the value shifts into a negative direction until 7,000 seconds, at which time the hydroxyl effect (or hydrogen effect) appears in the initial stage, but the charge-trapping effect then prevails.

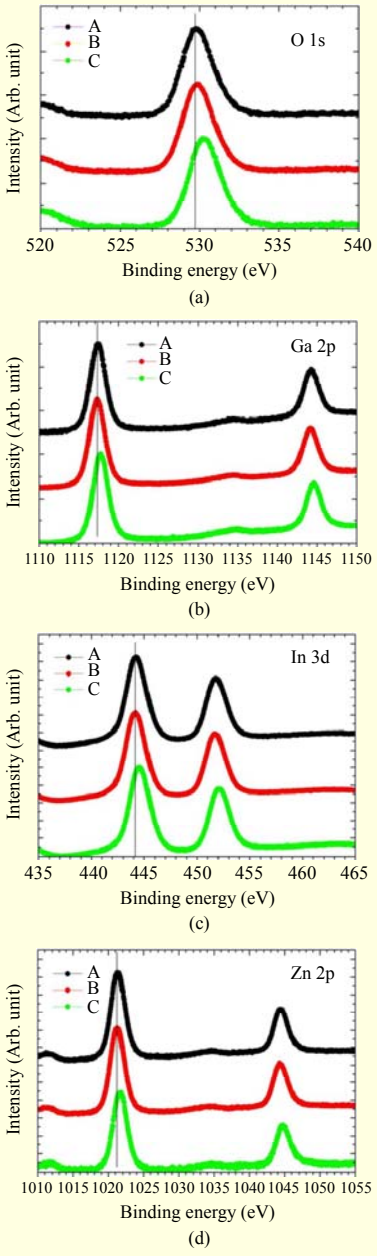

Fig. 4. Results from XPS analysis on A-, B-, and C-type IGZO films.

From both the PBS and CCS tests, the shift in the value of V_{th} decreases with an increase in the amount of Ga, namely, the electrical stability is improved. Nomura and others reported that an increase of Ga can suppress the formation of oxygen vacancies and thus reduce the carrier concentration, which is related to the strong binding between Ga and oxygen atoms [17]. Conversely, a weak bonding state will make it easy to form deep-state energy levels in the channel and/or charge trap sites in the interface between the channel and gate insulator, degrading the device.

To elucidate the change in the binding energy as a function of the channel composition, X-ray photoelectron spectroscopy (XPS) measurements are utilized. From Fig. 4, it is clear that In, Ga, and Zn atoms are rather insensitive to the local environment, but O atoms show a slight chemical shift, depending on the composition. Very recent work revealed that the local structure in amorphous IGZO should be a chained network of InO and (Zn,Ga)O [18]. They argued that the transport will be affected by not only the In s-like conduction band but also by the Zn and Ga localized states. In addition, they proposed that the (2217) phase should have a higher oxidation state in the (Zn,Ga)O cluster unlike the (1114) phase, which means a stronger bonding between the (Zn,Ga) and O atoms. This is also consistent with our stability results showing that Ga-rich samples are stabler than samples with less Ga.

IV. Conclusion

In this study, the electrical instability of top-gate IGZO-TFTs was evaluated as a function of the channel compositions. According to the PBS and CCS tests, the larger the amount of Ga in the channel, the more robust the TFT, which is consistent with the XPS analysis, namely, the strong binding of O atoms clearly appeared in the IGZO film with a larger amount of Ga.

References

[1] H. Yabuta et al., "High-Mobility Thin-Film Transistor with Amorphous $InGaZnO_4$ Channel Fabricated by Room Temperature rf-Magnetron Sputtering," *Appl. Phys. Lett*., vol. 89, no. 11, Sept. 2006, 112123.

[2] I. Song et al., "Short Channel Characteristics of Gallium–Indium–Zinc–Oxide Thin Film Transistors for Three-Dimensional Stacking Memory," *IEEE Electron Device Lett.*, vol. 29, no. 6, June 2008, pp. 549-552.

[3] J. Sun et al., "ZnO Thin-Film Transistor Ring Oscillators with 31-ns Propagation Delay," *IEEE Electron Device Lett.*, vol. 29, no. 7, July 2008, pp. 721-723.

[4] C. Chen et al., "Amorphous In–Ga–Zn–O Thin-Film Transistor Current-Scaling Pixel Electrode Circuit for Active-Matrix Organic Light-Emitting Displays," *Jpn. J. Appl. Phys.*, vol. 48, Mar. 2009, pp. 03B025-1-03B025-7.

[5] M. Shur and M. Hack, "Physics of Amorphous Silicon-Based Alloy Field-Effect Transistors," *J. Appl. Phys.*, vol. 55, no. 10, Jan. 1984, pp. 3831-3842.

[6] F.R. Libsch and J. Kanicki, "Bias-Stress-Induced Stretched-Exponential Time Dependence of Charge Injection and Trapping in Amorphous Thin-Film Transistors," *Appl. Phys. Lett.*, vol. 62, Mar. 1993, pp. 1286-1288.

[7] J.M. Lee et al., "Bias-Stress-Induced Stretched-Exponential Time Dependence of Threshold Voltage Shift in InGaZnO Thin Film Transistors," *Appl. Phys. Lett.*, vol. 93, Sept. 2008, 093504.

[8] P. Görrn et al., "Stability of Transparent Zinc Tin Oxide Transistors under Bias Stress," *Appl. Phys. Lett.,* vol. 90, Feb. 2007, 063502.

[9] J.K. Jeong et al., "Origin of Threshold Voltage Instability in Indium-Gallium-Zinc Oxide Thin Film Transistors," *Appl. Phys. Lett*., vol. 93, Sept. 2008, 123508.

[10] W.S. Cheong et al., "Process Development of ITO Source/Drain Electrode for the Top-Gate Indium-Gallium-Zinc Oxide Transparent Thin-Film Transistor," *Thin Solid Films*, vol. 517, May 2009, pp. 4094-4099.

[11] W.S. Cheong et al., "Effects of Interfacial Dielectric Layers on the Electrical Performance of Top-Gate In-Ga-Zn-Oxide Thin-Film Transistors," *ETRI J.*, vol. 31, no. 6, Dec. 2009, pp. 660-666.

[12] Y.K. Moon et al., "Improvement in the Bias Stability of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors Using an O_2 Plasma-Treated Insulator," *Appl. Phys. Lett*., vol. 95, July 2009, 013507.

[13] K. Nomura et al., "Origins of Threshold Voltage Shifts in Room-Temperature Deposited and Annealed a-In–Ga–Zn–O Thin-Film Transistors," *Appl. Phys. Lett.*, vol. 95, July 2009, 013502.

[14] T. Iwasaki et al., "Combinatorial Approach to Thin-Film Transistors Using Multicomponent Semiconductor Channels: An Application to Amorphous Oxide Semiconductors in In–Ga–Zn–O System," *Appl. Phys. Lett.*, vol. 90, June 2007, 242114.

[15] P. Barquinha et al., "Toward High-Performance Amorphous GIZO TFTs," *J. Electrochem. Soc.*, vol. 156, no. 3, Aug. 2009, pp. H161-H168.

[16] J.H. Jeon et al., "Effects of Gate Bias Stress on the Electrical Characteristics of ZnO Thin-Film Transistor," *J. Korean Phys. Soc.*, vol. 53, no. 1, July 2008, pp. 412-415.

[17] K. Nomura et al., "Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors," *Nature*, vol. 432, Nov. 2004, pp. 488-492.

[18] D.Y. Cho et al., "Local Structure and Conduction Mechanism in Amorphous In–Ga–Zn–O Films," *Appl. Phys. Lett.*, vol. 94, Mar. 2009, 112112.