

Novel Architecture for Efficient Implementation of Dimmable VPPM in VLC Lightings

Jin-Doo Jeong, Sang-Kyu Lim, Il-Soon Jang, Myung-Soon Kim, Tae-Gyu Kang, and Jong-wha Chong

In this paper, a new architecture is proposed to achieve complexity efficiency in implementing variable pulse position modulation (VPPM). VPPM, specified in IEEE 802.15.7, can support wireless communication and dimming control simultaneously using visible light. The proposed architecture is based on the VPPM signal property in which the transition point of the modulated output is obtained by counting the sample index and comparing it to both the assigned dimming factor and the transmitting data. Therefore, the proposed architecture can be composed of simple logics, including a counter, a comparator, and an inverter, all of which are insensitive to the dimming resolution in contrast to a conventional codeword-table method. This paper describes the verification of the proposed algorithm through a register-transfer level implementation of the codeword and proposed architectures. In comparison with the codeword-table method, the proposed method gains a nine-fold complexity reduction at a 1% dimming-step resolution.

Keywords: Dimming, VLC, VPPM, LED, RTL.

I. Introduction

Variable pulse position modulation (VPPM) is a modulation scheme proposed for visible light communication (VLC). VLC systems carry out data communication through a wireless optical channel using visible light modulated in LED luminaires capable of obtaining high-speed switching [1]–[5].

In general, many applications using LED luminaires require dimming controllability to adjust the illumination intensity for context awareness or to reduce the power consumption for energy saving, and dimming is an essential function of modern VLC systems [6]–[10].

VPPM is one of the modulation schemes internationally standardized to obtain both wireless communications and brightness control simultaneously through the LED luminaires described in [1] and [2]. Studies on VPPM have been performed in such fields as an analysis of modulation signals [3] and the presentation of a receiving method [7]–[8]. However, implementation issues considering hardware complexity have been little studied.

In this paper, a design architecture is proposed to achieve complexity efficiency in implementing the VPPM systems. From the existing study in [3], tabling the codewords can be considered as the design scheme. However, the codeword-table method can increase the complexity with an increase in dimming-control resolution. The proposed design can obtain implementation efficiency insensitive to the dimming resolution and is appropriate for VLC applications requiring highly resolvable dimming.

II. VPPM Modulation Based on Codeword Table

The VPPM modulation scheme basically makes use of the

Manuscript received Mar. 31, 2014; revised July 10, 2014; accepted July 17, 2014.

This work was supported by the MOTIE KEIT (10042947, System Lighting), the MSIP IITP (10040037, Intelligent IT Lighting), and the ICT Standardization Program of MSIP, Rep. of Korea.

Jin-Doo Jeong (corresponding author, jdjeong@etri.re.kr), Sang-Kyu Lim (sklim@etri.re.kr), Il-Soon Jang (isjang@etri.re.kr), Myung-Soon Kim (mskim75@etri.re.kr), and Tae-Gyu Kang (tgkang@etri.re.kr) are with the IT Convergence Technology Research Laboratory, ETRI, Daejeon, Rep. of Korea.

Jong-wha Chong (jchong@hanyang.ac.kr) is with the School of Electrical and Electronics Engineering, Hanyang University, Seoul, Rep. of Korea.

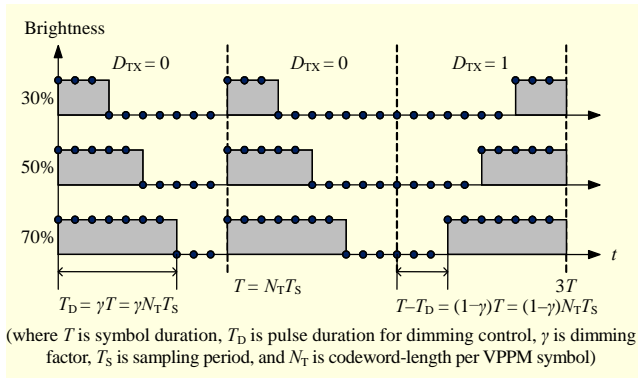


Fig. 1. Signal waveform of VPPM.

Table 1. Codewords for VPPM with 10% dimming step.

Dimming factor γ	Codeword for Bit 0	Codeword for Bit 1
0	0000000000	0000000000
0.1	1000000000	0000000001
0.2	1100000000	0000000011
0.3	1110000000	0000000111
0.4	1111000000	0000001111
0.5	1111100000	0000011111
0.6	1111110000	0000111111
0.7	1111111000	0001111111
0.8	1111111100	0011111111
0.9	1111111110	0111111111
1.0	1111111111	1111111111

main characteristics of 2-pulse-position modulation (2-PPM) for data transmission together with pulse-width modulation (PWM) for dimming control [1]–[3]. Figure 1 shows a signal waveform of VPPM based on a combination of 2-PPM and PWM. The VPPM signals can be expressed in the digital domain using a memorized mapping table, as shown in Table 1, where the codewords for the VPPM, with a 10% dimming resolution, are listed. In Table 1, γ indicates the dimming factor, which indicates the relative brightness level, within a range of zero and one. The VLC data are not transmitted when the dimming factor is zero or one because they represent cases in which the VLC luminaire is in a “fully off” or “fully on” state, respectively. Figure 1 also shows the signal waveforms, which illustrate the VPPM dimming mechanism (dependent upon the dimming factors listed in Table 1).

Table- or memory-based methods can be typically considered for implementation of a codeword table, such as Table 1. However, the aforementioned studies have presented methods based on a smaller table or discrete logic architecture

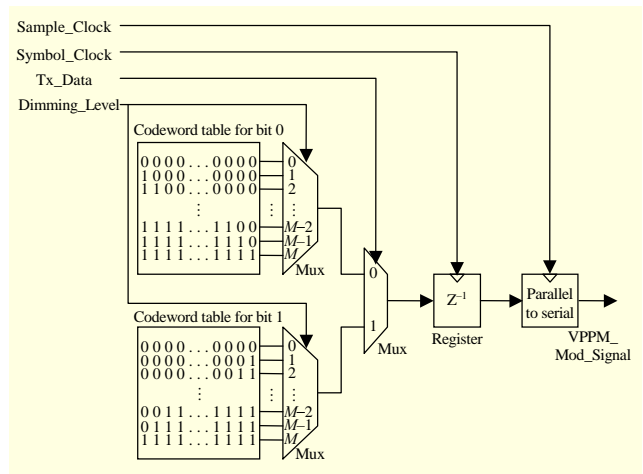


Fig. 2. Typical block diagram of table-based VPPM modulation.

to reduce the hardware complexity owing to a large codeword table [11]–[12]. No studies on the design or implementation of dimmable VPPM modulation based a codeword table such as Table 1 have been performed. This paper proposes a design method for VPPM modulation based on a discrete logic architecture to obtain a lower complexity than that of the typical table-based design.

Figure 2 shows a typical block diagram of table-based VPPM modulation by applying codewords in Table 1 to the codeword-table structure in [12]. In Fig. 2, Tx_Data, Dimming_Level, and VPPM_Mod_signal indicate the data to be delivered, the dimming index closely linked to the dimming factor (γ), and the synchronized (or synthesized) VPPM-modulated output signal, respectively. From Fig. 2, it can be supposed that the hardware complexity of the table-based VPPM modulator increases with an increase in the dimming resolution. Therefore, this paper proposes and describes a new architecture composed of only simple digital logics to avoid an increase in hardware complexity even when the dimming resolution increases.

III. Proposed Architecture for Complexity Efficiency

The architecture design for mitigating the hardware complexity of functional blocks for VPPM begins with the modeling on VPPM-modulated signals, as expressed in (1).

$$s(t) = A \sum_{n=0}^{\infty} p_{\text{VPPM}}(t - nT),$$

$$p_{\text{VPPM}}(t) \Big|_{0 \leq t < T} = \begin{cases} \int_0^T [\delta(t) - \delta(t - \gamma T)] dt & \text{for } D_{\text{TX}} = 0, \\ \int_0^T \delta(t - (1 - \gamma)T) dt & \text{for } D_{\text{TX}} = 1. \end{cases} \quad (1)$$

In (1), $s(t)$, A , $p_{\text{VPPM}}(t)$, $\delta(t)$, T , and D_{TX} represent a VPPM-modulated signal, amplitude, modulated signal per symbol,

delta function, symbol duration, and transmitting data, respectively. Equation (1) shows that a modulated signal can be characterized by D_{TX} and the transition point from low to high or high to low within the symbol duration.

$$p_{VPPM}(t) \Big|_{0 \leq t < T} = \begin{cases} 1 & \text{for } D_{TX} = 0 \text{ and } 0 \leq t < \gamma T, \\ 0 & \text{for } D_{TX} = 0 \text{ and } \gamma T \leq t < T, \\ 0 & \text{for } D_{TX} = 1 \text{ and } 0 \leq t < (1-\gamma)T, \\ 1 & \text{for } D_{TX} = 1 \text{ and } (1-\gamma)T \leq t < T, \end{cases} \quad (2)$$

$$= \begin{cases} \tilde{D}_{TX} & \text{for } D_{TX} = 0 \text{ and } 0 \leq t < \gamma T, \\ D_{TX} & \text{for } D_{TX} = 0 \text{ and } \gamma T \leq t < T, \\ \tilde{D}_{TX} & \text{for } D_{TX} = 1 \text{ and } 0 \leq t < (1-\gamma)T, \\ D_{TX} & \text{for } D_{TX} = 1 \text{ and } (1-\gamma)T \leq t < T, \end{cases}$$

where $\tilde{D}_{TX} = 1$ for $D_{TX} = 0$, and $\tilde{D}_{TX} = 0$ for $D_{TX} = 1$.

Equation (2) describes the signal value of the VPPM symbol derived from (1) and Fig. 1. From (2), a VPPM-modulated signal can be characterized with the transmitting data, D_{TX} , logically inverting operation, and inverting point in the time domain. This means that VPPM modulation can be based on simple digital logics and operations to make the complexity more efficient.

Figure 3 shows the architecture of the proposed VPPM, which is composed of discrete digital logics. Typically, digital circuits processing a digital signal in the discrete-time domain are operated using a clock trigger with a specific frequency. This means that a signal sampled at a specific frequency is processed through a digital circuit. The signal sampling should be considered to describe the operation of the proposed VPPM architecture.

In Fig. 1, T_D is the pulse duration varied by the dimming-control signal. In this case, the symbol rate or frequency is $1/T$ Hz. If the VPPM symbols are sampled on a clock with an N_T/T Hz frequency, then one VPPM symbol is composed of N_T samples. The number N_D of samples in a high-level pulse duration related with dimming factor γ is then rounded off to $(T_D/T) \times N_T$. If the dimming resolution is a sub-multiple of N_T , then N_D is $(T_D/T) \times N_T$ directly.

Setting the VPPM-modulated signal to S_{VPPM_TX} , when the transmitting data D_{TX} is equal to zero, S_{VPPM_TX} is logically a high state ('one') from the starting sample to N_D sample of the symbol, and S_{VPPM_TX} is logically a low state ('zero') in the other samples of the symbol from Fig. 1 and (2). When D_{TX} is equal to one, S_{VPPM_TX} is logically a low state ('zero') from the starting sample to the $(N_T - N_D)$ sample of the symbol, and S_{VPPM_TX} is a logically high state ('one') in the other samples of the symbol. Setting the level-transient point of S_{VPPM_TX} to N_{TP} , N_{TP} is equal to N_D for $D_{TX} = 0$, and N_{TP} is the same as $(N_T - N_D)$ for $D_{TX} = 1$. For $D_{TX} = 0$, from (2), S_{VPPM_TX} is the same as

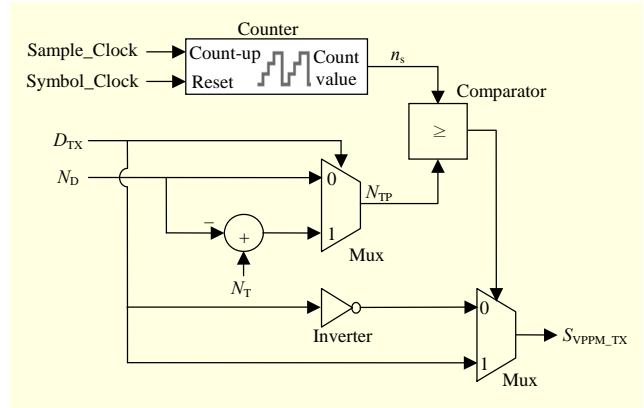


Fig. 3. Architecture of proposed VPPM modulation.

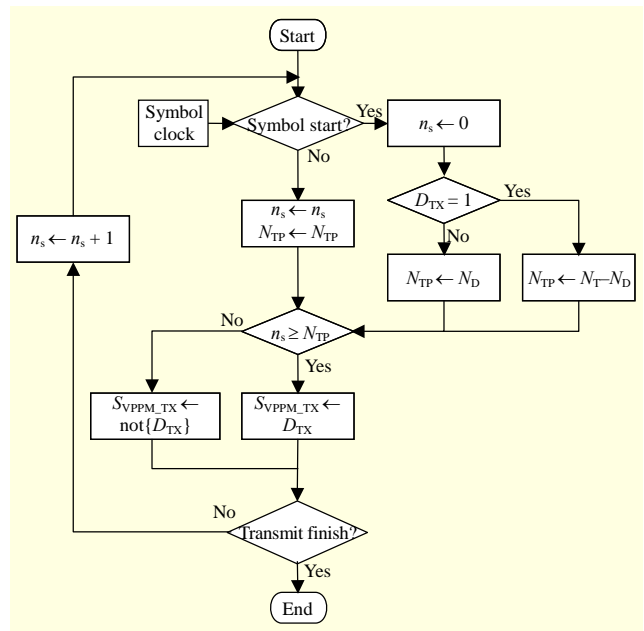


Fig. 4. Signal flow chart of proposed VPPM.

inverting D_{TX} (logically equivalent to “not(D_{TX})”) from the starting sample to the N_{TP} sample of the symbol. For the other samples in the symbol, S_{VPPM_TX} is equal to D_{TX} .

Figure 4 shows the signal flow chart for the proposed VPPM from the relation of the VPPM signal, S_{VPPM_TX} , the transmitting data, D_{TX} , and the transient point (N_{TP}). In Fig. 4, n_s is the sampling count value in the currently modulated symbol and can represent the sample index.

The proposed VPPM shown in Fig. 4 is processed as follows. First, determination of the starting point of the modulating symbol is required. This determination is operated with the symbol clock synchronized to the symbol rate. When the determination of the starting point of the symbol is finished, sample index n_s is reset to zero, and transient point N_{TP} is also reset to N_D or $N_T - N_D$ considering the value of D_{TX} . In the next step, the output for the modulated signal S_{VPPM_TX} is selected

through a comparison result between n_s and N_{TP} . Next, n_s is increased for each of the following sample indices; that is, $n_s + 1$.

The proposed architecture in Fig. 3 is composed of relatively simple logics including a counter, 2×1 comparator, subtracter, inverter, and two 2×1 muxes. Therefore, the complexity increase of the proposed modulator is slight compared with a table-based modulator. This means that the proposed method is more efficient in implementing a VPPM transmitter.

IV. Implementation and Experimentation Results

For a complexity comparison, the table-based method and the proposed method were designed at the register-transfer level (RTL) using a hardware description language. For the design verification, it was determined whether the input and output signals in the proposed method are the same as those in the codeword-table method. Figure 5 shows the timing simulation results in both the table-based and the proposed method with a 10% dimming-step resolution using the ModelSim tool [13]–[14]. This means that the waveforms of the proposed method are equal to those of the table-based method, and the required power and spectral efficiencies of both methods are equal to the results in [3]. In Fig. 5, the pulse width of the modulated signal is changed according to the dimming-level input, the full brightness of which is 10. The VPPM modulation was also verified by monitoring the detected data of the VPPM demodulator with a loopback input from the modulator, which was designed using the table-based method or the proposed method.

Table 2 shows the complexity comparison results between the codeword-table method and proposed method. The

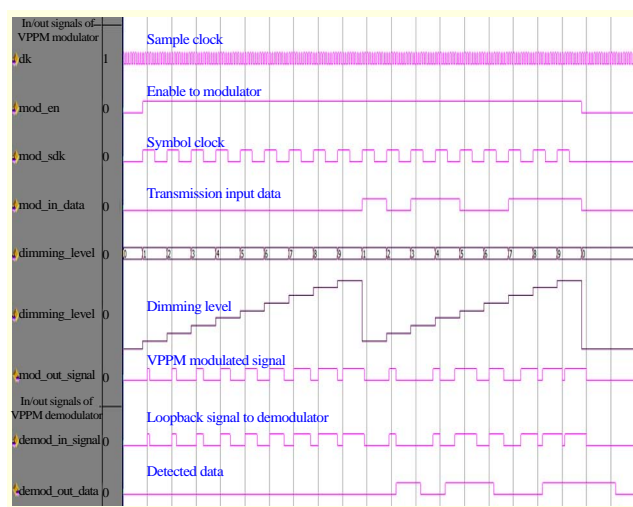


Fig. 5. Timing simulation results for both the table-based method and proposed method with a 10% dimming-step resolution.

Table 2. Complexity comparison results between the codeword-table method and proposed method.

Dimming step (%) (codeword length, resolution bits)	Cell usage in XC3S500e FPGA			
	Codeword-table method		Proposed method	
	BELS	FlipFlops /Latches	BELS	FlipFlops /Latches
33.33 (3, 2)	12	10	12	10
20 (5, 3)	17	12	15	12
10 (10, 4)	33	14	22	14
5 (20, 5)	76	16	26	16
3.33 (30, 5)	131	16	26	16
2.5 (40, 6)	142	18	29	18
2 (50, 6)	187	18	29	18
1.25 (80, 7)	274	20	35	20
1 (100, 7)	325	20	35	20
Dimming step (%) (codeword length, resolution bits)	Cell usage in CoolRunner2 CPLD			
	Codeword-table method		Proposed method	
	BELS	FlipFlops /Latches	BELS	FlipFlops /Latches
33.33 (3, 2)	36	10	23	10
20 (5, 3)	60	12	34	12
10 (10, 4)	105	14	55	14
5 (20, 5)	119	16	69	16
3.33 (30, 5)	198	16	67	16
2.5 (40, 6)	183	18	83	18
2 (50, 6)	487	18	82	18
1.25 (80, 7)	702	20	97	20
1 (100, 7)	851	20	96	20

(BELS represents basic elements in FPGA or CPLD)

comparison results were derived from the synthesis of the RTL designs of a Xilinx XC3S500e FPGA and CoolRunner2 CPLD using the ISE tool [13], [15], with a synthesis option for area optimization. In Table 2, a 33.33% dimming step represents the maximum step supporting dimmable VLC transmission. The complexity of the codeword-table method increases as the dimming resolution increases, as shown in Table 2. On the other hand, the complexity of the proposed method is only slightly increased. At a 1% dimming-step resolution, the proposed method gains a complexity reduction by about nine-fold compared with the table-based method. This means that the implementation efficiency is achieved using the proposed method, especially at a high dimming resolution.

Table 3 shows the estimated power consumption results of the codeword-table method and proposed method, which are obtained from a Xilinx XPower Analyzer with a 25 MHz

Table 3. Estimated power consumption results of the codeword-table method and proposed method.

Dimming step (%) (codeword length, resolution bits)	Estimated power consumption (mW)			
	Codeword-table method		Proposed method	
	FPGA	CPLD	FPGA	CPLD
33.33 (3, 2)	82.89	0.038	82.97	0.038
20 (5, 3)	82.96	0.038	83.11	0.038
10 (10, 4)	82.97	0.038	83.06	0.038
5 (20, 5)	82.83	0.038	83.06	0.038
3.33 (30, 5)	83.03	0.038	83.06	0.038
2.5 (40, 6)	82.88	0.038	83.10	0.038
2 (50, 6)	83.07	0.038	83.10	0.038
1.25 (80, 7)	83.31	0.038	83.13	0.038
1 (100, 7)	83.28	0.038	83.13	0.038

clock setting. From Table 3, the difference between power consumptions according to the dimming resolutions is slight in each platform of the FPGA and CPLD. However, in terms of power consumption and cost, it can be stated that the implementation of the VPPM modulation on CPLD is preferred over implementation on an FPGA.

Figure 6 shows the waveform measurement results of VLC lighting implemented using the proposed VPPM modulation to support a 10% dimming step. The measurement environment is shown in Fig. 6(a). The computer in Fig. 6(a) is used for generating the transmitting and dimming data through a graphic user interface. Waveforms at the output of the VPPM transmitter to LED luminaire have been measured using an oscilloscope. From Fig. 6(b), a modulator based on the proposed method can achieve pulse-width controllability for brightness control.

VLC lighting including the VPPM modulator is able to change the illuminance by controlling the dimming level. In other words, the specific illuminance of the VLC lighting including the VPPM modulator can be obtained by controlling the dimming level of the VPPM modulator. Figure 7 shows the illuminance measurement environment and the measurement results of 10 W VLC lighting implemented through the proposed VPPM modulation. In Fig. 7(a), the illuminance was measured using the average value from nine illuminometers placed 3×3 vertically from a 10 W LED luminaire using the proposed VPPM modulator. Figure 7(b) shows that the VLC luminaire with the proposed modulator can control the illuminance in a manner that is approximately proportional to the assigned dimming controlling level.

The dimming controllability of LED lighting can increase

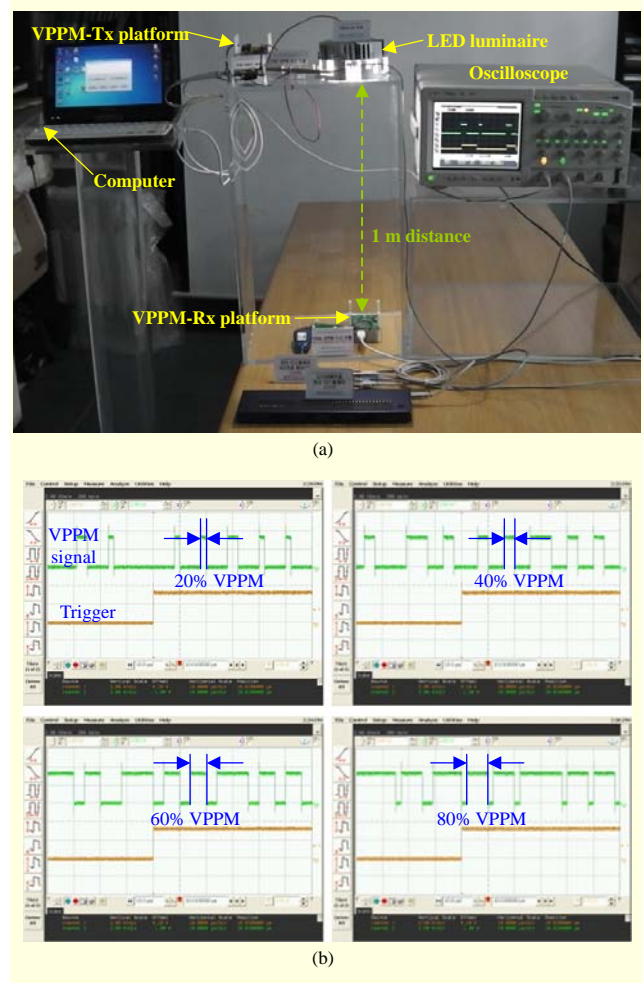


Fig. 6. Waveform measurement results of VLC lighting implemented using the proposed VPPM modulation: (a) waveform measurement environment and (b) waveform measurement results.

the value of commercial buildings by making them more comfortable and energy efficient [16]. The proposed method can achieve more efficient complexity in comparison with a typical table-based method and is suitable to implement in dimmable VPPM-VLC lighting systems. In particular, the proposed method is more appropriate for applications such as indoor audio-guiding and location-based services requiring fine brightness control and a low data rate, whereas it is difficult to be applied to multimedia transmission based on a high data rate. This is because the dimming resolution of the VPPM modulation is inversely proportional to the data rate when a clock frequency that is typically dependent on the switching speed of the LED module is specified. In terms of the evolution of VPPM-VLC lighting, VLC dimming control through cooperation with a backbone network to transfer scheduling-data processed by an optimization algorithm can offer precise location-based and enhanced context-aware services and

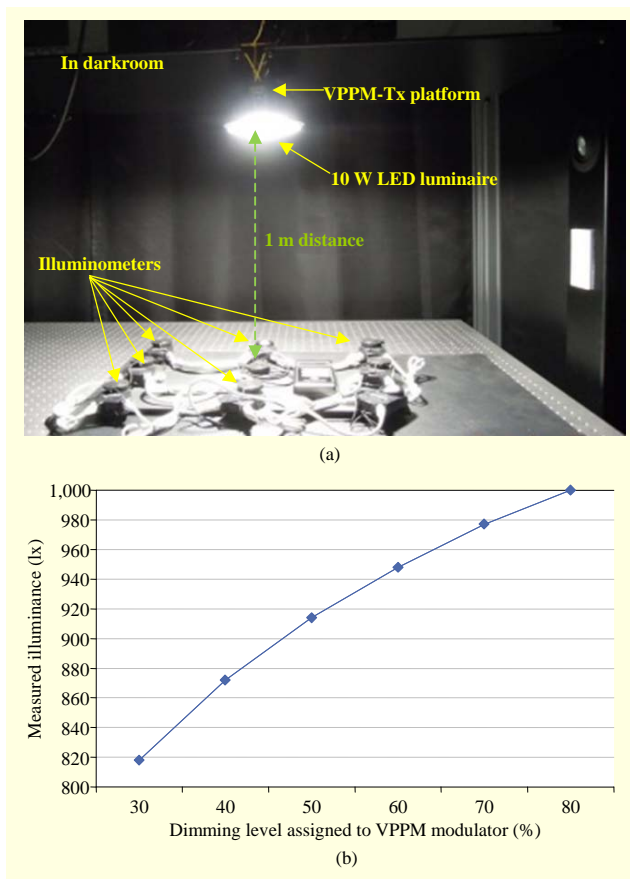


Fig. 7. Illuminance measurement results of 10 W VLC lighting implemented using the proposed VPPM modulation: (a) illuminance measurement environment and (b) illuminance measurement results.

energy savings in shopping malls or complex buildings [17]–[18]; and it may contribute to an early adoption of VLC lighting.

V. Conclusion

This paper proposed a complexity-efficient architecture for a VPPM design supporting simultaneous wireless data transmission and dimming control. The proposed architecture is based on sample counting, transition-point control, and two 2×1 muxes, which are composed of relatively simple logic, and its complexity is slightly sensitive to changes in the dimming resolution. The implementation efficiency can then be achieved using the proposed method, as compared with a conventional codeword-table method, particularly in applications requiring a high dimming-resolution controlled VLC. Finally, the additional researches on the communication performance analysis with respect to dimming level and the impact of interference in VPPM-VLC system for further studies will be continued.

References

- [1] IEEE Std. 802.15.7, *IEEE Standard for Local and Metropolitan Area Networks — Part 15.7: Short-Range Wireless Optical Communication Using Visible Light*, New York, NY, USA, 2011.
- [2] S. Rajagopal, R.D. Roberts, and S.-K. Lim, “IEEE 802.15.7 Visible Light Communication - Modulation Schemes and Dimming Support,” *IEEE Commun. Mag.*, vol. 50, no. 3, Mar. 2012, pp. 72–82.
- [3] K. Lee and H. Park, “Modulations for Visible Light Communications with Dimming Control,” *IEEE Photon. Technol. Lett.*, vol. 23, no. 16, Aug. 15, 2011, pp. 1136–1138.
- [4] M. Rouissat, R.A. Borsali, and M.E. Chikh-Bled, “A New Modified MPPM for High-Speed Wireless Optical Communication Systems,” *ETRI J.*, vol. 35, no. 2, Apr. 2013, pp. 188–192.
- [5] I.E. Lee, M.L. Sim, and F.W.L. Kung, “Performance Enhancement of Outdoor Visible-Light Communication System Using Selective Combining Receiver,” *IET Optoelectron.*, vol. 3, no. 1, Feb. 2009, pp. 30–39.
- [6] G. Ntogari et al., “Combining Illumination Dimming Based on Pulse-Width Modulation with Visible-Light Communications Based on Discrete Multitone,” *J. Opt. Commun. Netw.*, vol. 3, no. 1, Jan. 2011, pp. 56–65.
- [7] K. Choi et al., “Visible Light Communications with Color and Dimming Control by Employing VPPM Coding,” *Int. Conf. Ubiquitous Future Netw.*, Phuket, Thailand, July 4–6, 2012, pp. 10–12.
- [8] K. Choi et al., “Visible Light Communication with Color and Brightness Control of RGB LEDs,” *ETRI J.*, vol. 35, no. 5, Oct. 2013, pp. 927–930.
- [9] K.L. Sterckx and P. Saengudomlert, “Visible Light Communication via Dimmable LED Lamps Using Pulses of Equal Shape,” *European Conf. Netw. Opt. Commun.*, Newcastle upon Tyne, UK, July 20–22, 2011, pp. 48–51.
- [10] M. Anand and P. Mishra, “A Novel Modulation Scheme for Visible Light Communication,” *IEEE India Conf.*, Kolkata, India, Dec. 17–19, 2010, pp. 1–3.
- [11] P.-Y. Chen and Y.-M. Lin, “A Low-Cost VLC Implementation for MPEG-4,” *IEEE Trans. Circuits Syst.—II: Exp. Briefs*, vol. 54, no. 6, June 2007, pp. 507–511.
- [12] S.-C. Hsia, “Prototyping Implementation for Low-Complexity Real-Time MPEG-2 Variable Length Encoder,” *IEEE Int. Workshop System-on-Chip Real-Time Appl.*, Calgary, Canada, June 30–July 2, 2003, pp. 386–389.
- [13] V. Pedroni, *Circuit Design with VHDL*, Cambridge, MA, USA: MIT Press, 2004, pp. 515–535.
- [14] Mentor Graphics, *ModelSim – Leading Simulation and Debugging*, Mentor Graphics Corporation. Accessed Sept. 23, 2014. <http://www.mentor.com/products/fpga/model>

- [15] Xilinx, *FPGA Tutorials – ISE Design Suite Tutorials*, Xilinx Inc. Accessed Sept. 23, 2014. <http://www.xilinx.com/training/fpga-tutorials.htm>
- [16] J. Gancarz, H. Elgala, and T.D.C. Little, “Impact of Lighting Requirements on VLC Systems,” *IEEE Commun. Mag.*, vol. 51, no. 12, Dec. 2013, pp. 34–41.
- [17] H. Kim, S. Chang, and T-G Kang, “Enhancement of Particle Swarm Optimization by Stabilizing Particle Movement,” *ETRI J.*, vol. 35, no. 6, Dec. 2013, pp. 1168–1171.
- [18] S.-K. Lim et al., “Entertainment Lighting Control Network Standardization to Support VLC Services,” *IEEE Commun. Mag.*, vol. 51, no. 12, Dec. 2013, pp. 42–48.



Jin-Doo Jeong received his BS degree in electronic engineering in 1998 and his MS degree in electronic and communication engineering in 2000 from Hanyang University, Seoul, Rep. of Korea. In 2010, he joined the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, where

he has worked on wireless personal area communication systems using UWB and chirp signals. He is a senior member of the engineering staff in ETRI, and he is concentrating on the area of visible light communications.



Sang-Kyu Lim received his BS degree in physics in 1995 and his MS and PhD degrees in electronics engineering in 1997 and 2001, respectively, from Sogang University, Seoul, Rep. of Korea. Since he joined the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, in 2001, he

has worked on high-speed optical transmission systems and microwave/millimeter-wave circuit design. He is concentrating on the areas of visible light communication and lighting control networks. He is one of the major contributors in developing the IEEE 802.15.7 and ANSI E1.45 standards on VLC. He is a principal member of the engineering staff in ETRI and a senior member of the IEEE.



Il-Soon Jang is a principal member of the engineering staff at the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea. He received his BS degree in information and communication engineering in 1997 and his MS and PhD degrees in communication circuit and system engineering in 1999 and 2005, respectively, from Chungbuk National University, Cheongju, Rep. of Korea. In 2000, he joined ETRI, where he has worked on mobile communication systems. He is concentrating on the area of visible light communication. He is one of the major contributors in developing the IEEE 802.15.7 standard on VLC.



Myung-Soon Kim is a senior member of the engineering staff at the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea. She received her BS and MS degrees in information and communication engineering in 1999 and 2001, respectively, from Chonbuk National University, Jeonju, Rep. of Korea. In 2001, she joined ETRI, where she has worked on mobile communication systems. She is concentrating on the area of visible light communication

she has worked on mobile communication systems. She is concentrating on the area of visible light communication



Tae-Gyu Kang received his BS and PhD degrees in computer science in 1987 and 2002, respectively, from Kyonggi University, Gyeonggi, Rep. of Korea. He received his MS degree in computer science from Chung-Ang University, Gyeonggi, Rep. of Korea. He joined the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, in 2001 and worked on the CCS No.7 intelligent system and VoIP technologies. His current research interests are system lighting and visible light communication. He is one of the major contributors in developing the TTA standard and IEEE 802.15.7 standard on VLC. He is working as a director at the LED Communication Research Section in ETRI.



Jong-wha Chong received his BS and MS degrees in electronics engineering from Hanyang University, Seoul, Rep. of Korea, in 1975 and 1979, respectively and his PhD degree in electronics and communication engineering from Waseda University, Tokyo, Japan, in 1981. Since 1981, he has been a professor of the Department of Electronics Engineering at Hanyang University. From 1979 to 1980, he was a researcher at the C&C Research Center of Nippon Electronic Company, Tokyo, Japan. From 1983 to 1984, he was a visiting researcher at the Korean Institute of Electronics & Technology, Seongnam, Rep. of Korea. He was a visiting professor at

the University of California, Berkeley, USA, on two separate occasions — the first being from 1986 to 1987 and the second from 2006 to 2007. He was the chairman of the CAD & VLSI society of the Institute of Electronics and Information Engineers (IEIE) in 1993, the president of the IEIE in 2007, and the president of the KIEEE from 2009 to 2010. He is currently the chairman of the Fusion SoC Forum. His current research interests are SoC design methodology (including memory-centric design, and the physical design and automation of 3D ICs); indoor wireless communication SoC design for ranging and location; video systems; and power IT systems.