470-MHz–698-MHz IEEE 802.15.4m Compliant RF CMOS Transceiver

Youngho Seo, Seungsik Lee and Changwan Kim

This paper proposes an IEEE 802.15.4m compliant TV white-space orthogonal frequency-division multiplexing (TVWS)-(OFDM) radio frequency (RF) transceiver that can be adopted in advanced metering infrastructures, universal remote controllers, smart factories, consumer electronics, and other areas. The proposed TVWS-OFDM RF transceiver consists of a receiver, a transmitter, a 25% duty-cycle local oscillator generator, and a delta-sigma fractional-*N* phase-locked loop. In the TV band from 470 MHz to 698 MHz, the highly linear RF transmitter protects the occupied TV signals, and the high-Q filtering RF receiver is tolerable to in-band interferers as strong as −20 dBm at a 3-MHz offset. The proposed TVWS-OFDM RF transceiver is fabricated using a 0.13-μm CMOS process, and consumes 47 mA in the Tx mode and 35 mA in the Rx mode. The fabricated chip shows a Tx average power of 0 dBm with an error-vector-magnitude of < 3%, and a sensitivity level of −103 dBm with a packet-error-rate of < 3%. Using the implemented TVWS-OFDM modules, a public demonstration of electricity metering was successfully carried out.

Keywords: Advanced metering infrastructure, CMOS, IEEE 802.15.4m, OFDM, RF transceiver, Smart grid, TV white space, TV band devices.

I. Introduction

TV white space (TVWS) indicates the unused frequency spectrum within the TV UHF band at any given time in a particular geographic area [1], as shown in Fig. 1. In Fig. 1, because TVWS is also an unlicensed frequency band, it can be utilized in various wireless services, such as IEEE 802.11af, 802.15.4m, and 802.22b [1]–[4]. In addition, its superior propagation characteristics can enable better coverage using moderate transmission power. Therefore, in rural or undeveloped areas, wireless networks utilizing the TV band can be feasibly implemented. The presence of an advanced metering infrastructure (AMI) for gas, water, and electricity is a good example of how this may be realized, as shown in Fig. 2. In the figure, metering data obtained from houses that are far from each other are first sent to data collection units (DCUs) via TVWS wireless links. Then, for billing and data analysis, the data are gathered by utility providers over TVWS links or other backbone networks. In this manner, the time and human resources required for metering in suburban areas can be significantly reduced. In addition, supply shortages in certain areas can be prevented in advance with real-time metering. However, in order to feasibly construct wireless networks for

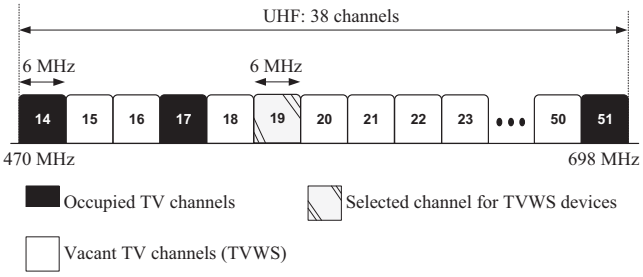

Fig. 1. Example of TV white space from 470 MHz to 698 MHz.

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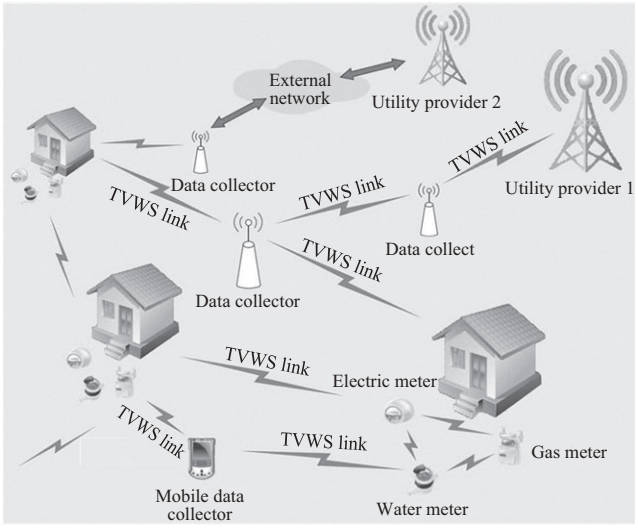

Fig. 2. Conceptual diagram of AMI utilizing TVWS wireless link.

incumbent users and their services, they should also be robust to nearby interferers in the TV band.

This paper describes an RF transceiver that operates in the 470-MHz–698-MHz TV band, and which is fabricated using a 0.13-μm CMOS process. The proposed RF transceiver is based on the IEEE 802.15.4m standard, which is also proposed by the authors' research group for AMI industries. To protect the TV signals, the proposed transmitter was designed to have superior linearity, thus satisfying the FCC regulations. The proposed receiver is tolerable to strong nearby interferers by using both RF and baseband filtering. Section II provides a brief overview of the IEEE 802.15.4m physical layers (PHY) and several design issues in the RF transceiver, while Section III provides extensive details about interference problems in the RF receiver operating in the TV band. The proposed RF transceiver architecture and detailed circuit designs are presented in Section IV and Section V, respectively. Measurement results of the fabricated RF transceiver are summarized in Section VI. In addition, a successful public demonstration of electricity metering using the fabricated RF transceiver is described in Section VII. Finally, Section VIII concludes this work.

II. System Overview and Design Issues

The IEEE 802.15.4 m standard was proposed for low-rate wireless personal area networks (WPANs) in 2013, and it supports the TVWS and describes three different physical layers (PHY) [1]: frequency-shift keying (FSK), orthogonal frequency-division multiple access (OFDMA), and narrowband (NB)-OFDM. In particular, TVWS-OFDM PHY supports a higher data rate of 1.56 Mbps compared with other PHYs; thus, it can be utilized to obtain services with higher quality. Accordingly, we designed the proposed RF transceiver to support the TVWS-OFDM PHY in the IEEE 802.15.4m standard.

Table 1. Summary of TVWS-OFDM PHY specification.

Parameters		Spec.
Nominal bandwidth (kHz)		1,064.5
Subcarrier spacing (kHz)		1,250/128
DFT size		128
Active tones		108
#Pilot tones		8
#Data tones		100
DC null tone		1
Data rate (kbps)	MCS0 (BPSK)	390.625
	MCS1 (QPSK)	781.250
	MCS2 (16-QAM)	1562.5
Sensitivity level (dBm)	MCS0 (BPSK)	−97
	MCS1 (QPSK)	−94
	MCS2 (16-QAM)	−88
Tx average power (dBm/100 kHz) (for personal/portable devices)		< 2.6
Tx PSD limit to adjacent channel (dBc)		55.4
Phase noise (dBc) @ 100-kHz/1-MHz offset		−100/−130

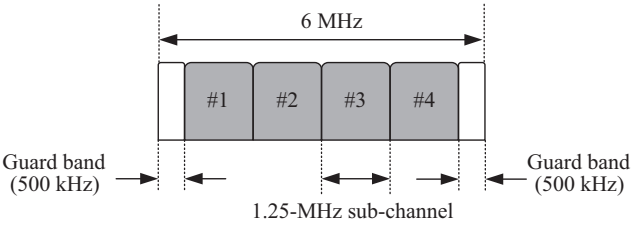

Fig. 3. TVWS-OFDM sub-channels in the 6-MHz TV channel.

The TVWS-OFDM PHY specifications are briefly summarized in Table 1 [1]. Here, the 6-MHz TV channel consists of four sub-channels with a bandwidth of 1.25 MHz, and two guard bands of 500 kHz, as shown in Fig. 3. In Table 1, one sub-channel consists of 128 tones, and has a subcarrier spacing of 9.76 kHz with a dc null-tone. Although four sub-channels are allocated, only one sub-channel may be used in noisy frequency environments. The TVWS-OFDM PHY supports data rates ranging from 390.625 kbps to 1562.5 kbps. To support different data rates, it uses three different modulation and coding schemes (MCSs), namely binary

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phase-shift keying (BPSK), quadrature PSK (QPSK), and 16-quadrature amplitude modulation (QAM). Because the required minimum sensitivity level in Table 1 is −97 dBm, the RF receiver should provide a low noise figure and high voltage gain. However, when the RF receiver operates in a high-gain mode to detect the input signal of −97 dBm, it needs to be able to tolerate strong interference in the TV band. The interference issues in RF receivers are discussed in detail in Section III.

To enable coexistence with existing TV services, the FCC strictly limits both the maximum transmission power level and the out-of-band emission of all TV band devices [4], [5]. For personal or portable devices, the transmitted power level must be less than +2.6 dBm/100-kHz, and the power spectral density (PSD) limit to adjacent channels is restricted by more than 55.4 dBc, as shown in Fig. 4. To satisfy this regulation, TVWS-OFDM PHY has allocated 500-kHz guard bands at both sides of the four sub-channels. These guard bands give extra space between the transmitted output signal and adjacent TV channels, which reduces the out-of-band emission of the transmitted power.

To adequately eliminate quantization noises from digital-to-analog-converters (DACs), a high-order low-pass filter (LPF) should be used in the transmitter. Considering the peak-to-average-power ratio (PAPR) of +10 dB in the MCS2 (16-QAM) mode, all RF and analog blocks in the transmitter should operate at a back-off of more than +10 dB from their output 1-dB compression point (OP1 dB).

There is also a strict phase noise requirement of the phase-locked loop (PLL), which should be more than −94 dBc and −124 dBc at 100-kHz and 1-MHz offsets, respectively, to satisfy the FCC's PSD limitation in the transmitter and the minimum sensitivity level in the receiver.

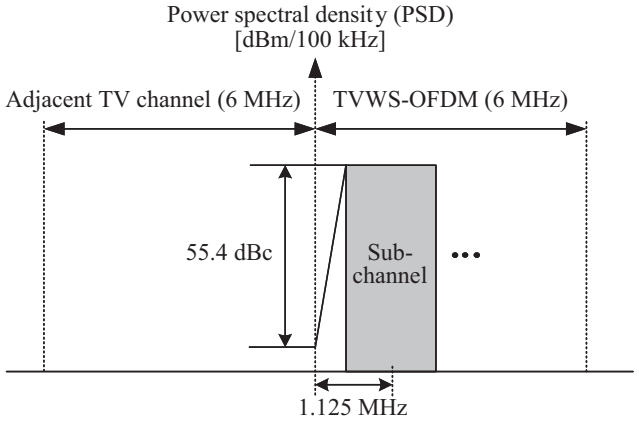

Fig. 4. FCC regulation for portable TVWS devices.

Fortunately, in the TV band from 470 MHz to 698 MHz, there are no harmonic mixing problems in the receiver or harmonic emissions in the transmitter because all odd-harmonic components of the local oscillator frequency are located out-of-band. These problems occur in TV tuners that operate in the entire TV band from 54 MHz to 698 MHz [2], [3], [6], [7].

III. Interference Problems

Because RF receivers select unused TV channels in the TV band, broadcast TV signals become unwanted interference sources. In addition, the signals transmitted by other TV band devices working for IEEE 802.11af, 802.22b, and so on can also pose an interference problem. Because they all use the same frequency band, and they are located close to the TVWS-OFDM channel, they function as *in-band* interferers to the TVWS-OFDM RF receiver. These in-band interferers cannot be easily attenuated by RF filtering, and they can saturate the RF front-end in a high-gain mode. If an RF receiver selects only the channels that are far away (more than two channels) from the interferers for ease of RF filtering, the receiver cannot secure many available channels in the TV band.

Accordingly, in order to determine the requirements of RF filtering for in-band interferers, and to secure many available channels in the TV band, we devised a worst-case scenario to describe the interference problem.

Figure 5 shows the devised worst-case scenario, where in-band interferers are close to the TVWS-OFDM channel. As seen in Fig. 5, assuming that two TV broadcasting signals occupy channels $n - 1$ and $n + 2$, the TVWS-OFDM device selects channel n. In this case, because blocker 1 is only at 500-kHz and 1.75-MHz offsets from sub-channels 1 and 2, respectively, in the TVWS-OFDM channel, it cannot be filtered out by any off-chip or on-chip RF filtering solution. Therefore, both sub-channels 1 and 2 are unavailable for communications. However, blockers 1 and 2 are located far away at 3-MHz

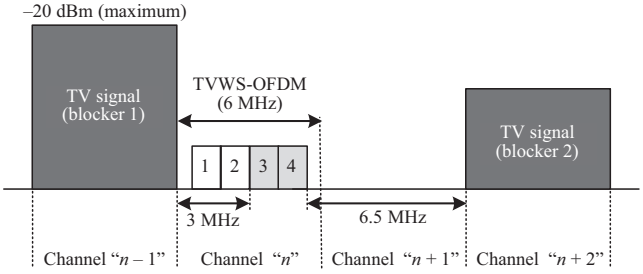

Fig. 5. Interference problems in a TVWS-OFDM receiver.

and 6.5-MHz offsets from sub-channels 3 and 4, respectively. Because these blockers can be attenuated with off-chip surface-acoustic-wave filters or on-chip RF filtering techniques in the receiver [8]–[14], sub-channels 3 and 4 can be utilized. The utilization of surface-acoustic wave filters in the multi-band RF receiver considerably increases the number of off-chip components and assembly costs, so it is not a favorable solution. On the other hand, the on-chip filtering solutions can support the multi-band RF band-passed filtering function with a few circuit blocks, where the center frequency of RF filtering is precisely controlled [8]–[14].

Finally, the TVWS-OFDM RF receiver is required to have an on-chip RF filtering function to ensure high immunity to the −20-dBm TV signals at an offset of more than 3 MHz, resulting in the presence of many available sub-channels in the TV band.

IV. RF Transceiver Architecture

For high silicon integration, two kinds of architectures can be used for the TVWS-OFDM RF transceiver: low-intermediate frequency (IF) architecture and zero-IF (direct-conversion) architecture. If a low-IF architecture is used, the IF may be one, two, or three times larger than the channel frequency of 1.25 MHz. The adoption of IF = 1.25 MHz (one channel frequency) cannot prevent wanted signals from dc-offset and low-frequency flicker noise. Alternatively, the use of IF = 2.5 MHz or 3.75 MHz can eliminate the dc-offset and flicker noise problems [15], but it leads to a high dc power consumption in the baseband circuits for a larger bandwidth. In addition, since the image signals have been located in the adjacent TV channels, a high image rejection ratio of more than 70 dB is required. It is very hard to implement on-chip image-rejection filters that satisfy this requirement.

Consequently, to avoid these complex problems in the low-IF architecture, we used a zero-IF architecture in the proposed RF transceiver, as shown in Fig. 6. Although the zero-IF transceivers suffer from dc-offset, flicker noise, local oscillator (LO) leakage, and so on [16], these problems are effectively solved with advanced design techniques, namely a 25% duty-cycle LO-driven mixing system [17]–[19] and the construction of a dc-offset cancellation loop [20].

In Fig. 6, the proposed zero-IF RF transceiver is composed of a receiver, a transmitter, a 25% duty-cycle LO generator (LOG), and a PLL. In the receiver, the RF input signal is amplified by the low-noise amplifier (LNA) and a trans-conductance amplifier (G_m), and it is then

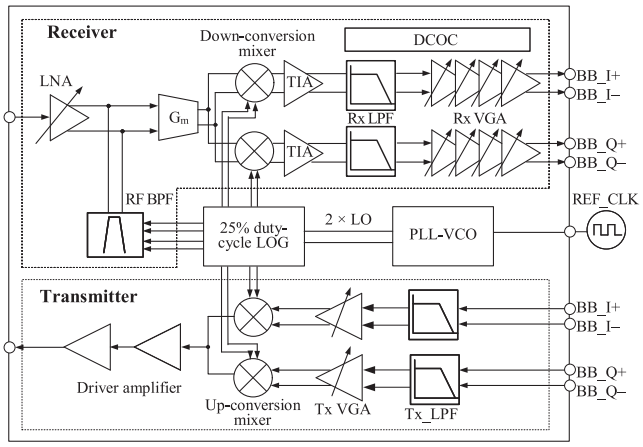

Fig. 6. Block diagram of the proposed zero-IF RF transceiver.

down-converted into a baseband signal by the down-conversion mixer. The trans-impedance amplifier (TIA) converts the input current signals into the output voltage signals for the following channel-selection LPFs and variable gain amplifiers (VGAs). To favorably solve the in-band interference problem, two high-Q RF band-pass filtering schemes are generated by the RF BPF (band-pass filter) and the down-conversion mixer, which are 25% duty-cycle LO-driven passive mixers [13], [14], [17]. Because a dc null-tone is allocated in the sub-channels, a dc-offset cancellation (DCOC) circuit is utilized to eliminate the dc-offset. In the transmitter, the baseband input signals are filtered at the Tx LPF, and their amplitudes are then adjusted by Tx VGA. The up-conversion mixer up-converts the baseband signals into an RF signal. Then, the DA amplifies the RF signal and propagates it into the air. For the RF BPF and up/down-conversion mixer, the LOG synthesizes the 25% duty-cycle quadrature LO clocks using the signal generated from the PLL.

V. Circuit Design

A. Receiver

To suppress the unwanted interferers in the RF domain, previously reported on-chip RF filtering receiver architectures can be classified into two types: blocker cancellation-based receivers [8], [9] and passive mixer-based receivers [10]–[12].

Blocker cancellation-based receivers [8], [9] cancel out the unwanted interferers using auxiliary feedback or feedforward paths. Although they have a low noise figure and high-Q RF filtering performance, they have a high dc-power consumption and a large chip area owing to the

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utilization of auxiliary signal paths. In addition, to prevent performance degradation due to process variations, extra calibration algorithms are required in the receiver. Passive mixer-based receivers [10]–[12] utilize 25% duty-cycle LO-driven passive mixers to achieve multi-band RF band-pass filtering [13], [14], where the passive mixer synthesizes a high-Q RF BPF by transforming baseband impedances to RF. They show superior high-Q RF filtering and high linearity, and their noise performance can be further improved by using an advanced CMOS process and by adoption of circuit techniques.

As discussed in Section III, the TVWS-OFDM receiver needs to tolerate in-band interferers as strong as −20 dBm at a 3-MHz offset. To achieve both high sensitivity and high immunity to the in-band interferers, the proposed RF front-end receiver is based not only on a conventional LNA-first architecture, but we also adopted two high-Q RF filters that use 25% duty-cycle LO-driven passive mixers, as shown in Fig. 7. In the proposed RF receiver in Fig. 7, the high RF gain from the LNA and G_m considerably suppresses the low-frequency flicker noise coming from the baseband circuits, which produces a high sensitivity level in the overall receiver chain. In addition, in contrast to the mixer-first architecture [11], [12], the LNA and G_m can mitigate a large LO feedthrough to the antenna. However, because the LNA and G_m amplify both the weak wanted signal and the strong in-band interferers by the same voltage gain, the following baseband circuits are saturated by the amplified in-band interferers. To effectively attenuate these interferers in the RF front-end, two high-Q RF BPFs Z_{RF1} and Z_{RF2} are utilized by adopting 25% duty-cycle LO passive mixers [13], [14].

In Fig. 7, the proposed LNA consists of a source inductive degeneration common-source amplifier (M_1 and M_2) and a common-source amplifier (M_3 and M_4). By connecting the input of M_3 to the output of M_1, a fully differential signal can be obtained at the LNA's output using a single-ended input signal. Therefore, this topology can remove an off-chip transformer and improve the noise figure by as much as 2 dB to 3 dB. For multiband operation, the input-matching circuit (L_G, C_{IN}, L_S, and M_1) and the resonant *RLC* load are respectively adjusted by C_{IN} and C_D with 4-bit control [21]. This multiband LNA topology provides a higher voltage gain, a higher selectivity, and a lower noise figure than conventional wideband LNAs [22], [23]. In the LNA, to reduce the chip area, with the exception of the source degeneration inductor L_S, all of the inductors are externally implemented. To accommodate the dynamic range of 80 dB in the receiver, the overall gain of the RF front-end can be adjusted to 48 dB, 28 dB, or 8 dB with 2-bit controls of the R_{IN} in the LNA.

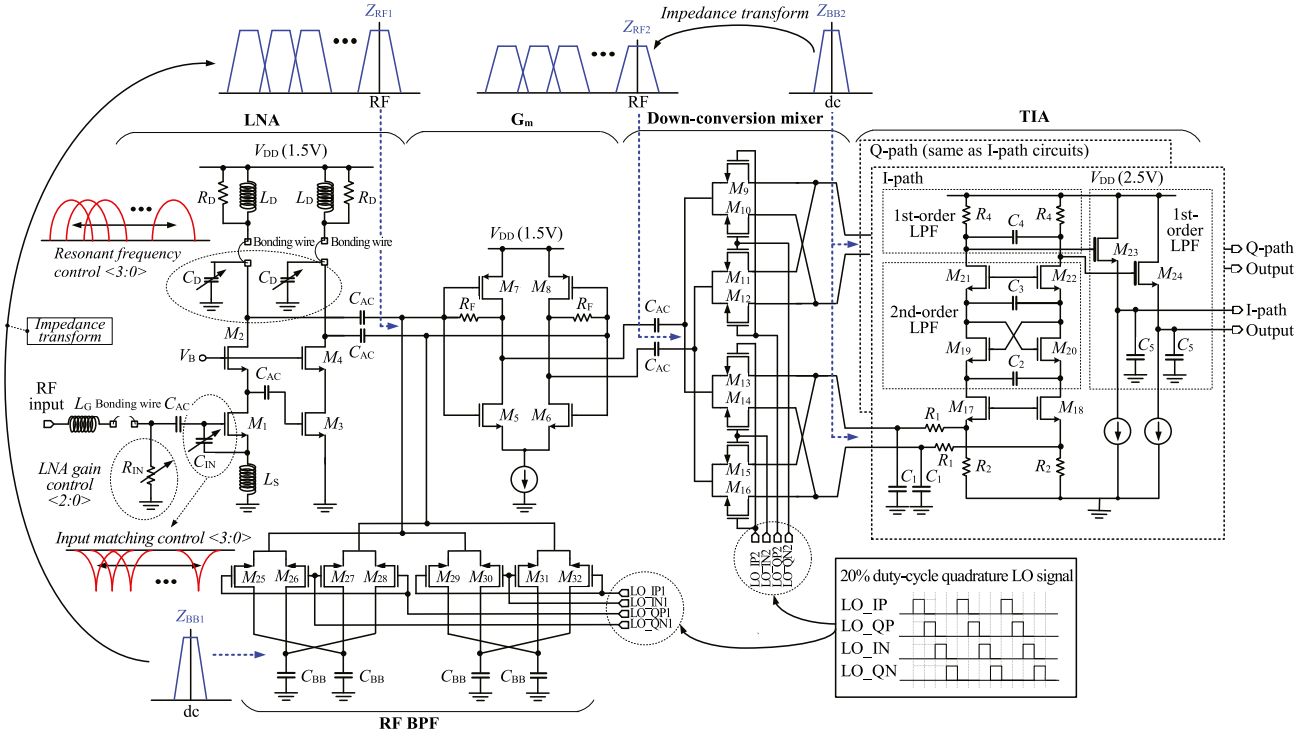

Fig. 7. Proposed RF front-end receiver with RF filtering.

The G_m is an inverter-type differential amplifier (M_5–M_8) with a resistive dc-feedback (R_F). The G_m further amplifies the input RF signal to suppress the flicker noise from the TIA, and isolates the two RF BPFs Z_{RF1} and Z_{RF2} from each other.

To achieve the first high-Q RF filtering Z_{RF1}, the RF BPF, which consists of a 25% duty-cycle LO-driven quadrature passive mixer (M_{25}–M_{32}) and four capacitors C_{BB}, is connected in parallel between the LNA and G_m. In the RF BPF, the passive mixer transforms the low-pass-shaped impedance Z_{BB1} centered at dc into the band-pass shaped impedance Z_{RF1} centered at LO frequency. The center frequency of the Z_{RF1} can be precisely controlled and moved to the wanted operating frequency by 25% duty-cycle LO clocks [13], [14], [17]. Note that in Fig. 7, the RF BPF is not connected at the LNA input or low-impedance nodes in the LNA, but is connected at the high-impedance nodes. This location of the RF BPF improves the stopband rejection ratio of the Z_{RF1}, and it also inhibits the LO feedthrough to the antenna. The source terminal biasing of the passive mixer in the RF BPF is defined by the input dc voltage of the G_m.

The second RF filtering Z_{RF2} occurs at the input of the down-conversion passive mixer, where the input impedance Z_{BB2} of the TIA is also transformed to the RF impedance Z_{RF2} with a band-pass frequency response. In Fig. 7, because the G_m has provides high isolation, the first and secondary RF filtering can simultaneously occur at the input and output nodes of G_m.

To obtain a high-quality-factor Z_{RF2}, we installed series resistor R_1 at the input of the TIA, which made the cut-off frequency of the $Z_{BB2} = 1/\{(R_1 + (R_2 \| 1/g_{m17}))C_1\}$. Although the use of R_1 causes a signal loss, it increases the voltage gain of the down-conversion mixer by increasing the mixer's output impedance. Therefore, the use of R_1 does not degrade the noise figure or linearity of the overall receiver.

Then, down-converted interferers are further suppressed by the proposed TIA with a fourth-order low-pass frequency response that is composed of a modified current-mode bi-quad ($M_{19–20}$ and $C_{2–3}$) [24], a first-order RC LPF (R_4 and C_4), and a first-order source follower-based LPF ($M_{23–24}$ and C_5) [25].

Figure 8 shows the simulated filtering characteristic of each block of the proposed RF front-end receiver. Considering the channel bandwidth of 1.25 MHz, the −1-dB bandwidth of the RF filters (Z_{RF1} and Z_{RF2}) and the TIA with fourth-order LPF are 2 MHz, 2.4 MHz, and 2 MHz, respectively; for each block, the corresponding attenuations at a 3-MHz offset frequency are 5.8 dB, 4.2 dB, and 27.5 dB, respectively. Since the current-mode bi-quad filter is embedded in the TIA, the transfer characteristic of the TIA has a peak in the passband, which compensates in-band signal losses caused by two RF filters Z_{RF1} and Z_{RF2}. Thus, the overall RF front-end receiver provides a flat passband within a 2-MHz −1-dB bandwidth and a 37.6-dB attenuation at 3-MHz offset, as shown in Fig. 8(d).

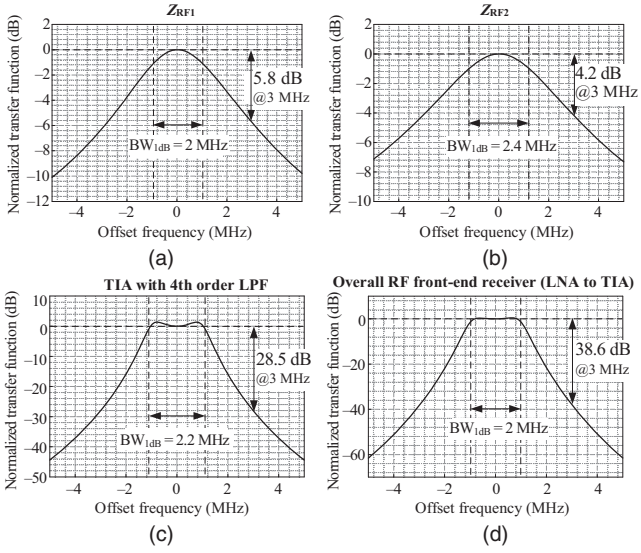

Fig. 8. Filtering characteristic of (a) Z_{RF1}, (b) Z_{RF2}, (c) the TIA with 4th-order LPF, and (d) the overall RF front-end receiver.

Consequently, from the LNA to the TIA, the simulated results show that the desired signal is amplified by 48 dB, but the 3-MHz offset interferer is only amplified by 9 dB by using two RF filters (Z_{RF1} and Z_{RF2}) and the fourth-order LPF.

Figure 9 shows the proposed receiver baseband circuit, which consists of a channel-selection LPF, four VGAs, a

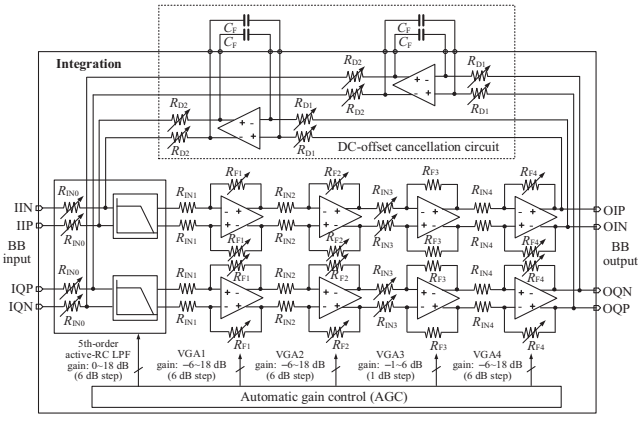

Fig. 9. Proposed receiver baseband circuit.

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DCOC circuit, and an automatic gain control (AGC). It provides a voltage gain of between −18 dB and +78 dB with a 1-dB fine step to support the dynamic range of the receiver. In Fig. 9, in order to fully remove the down-converted interferers and other unwanted signals, the channel-selection LPF is located at the front of the VGAs. It is designed with a fifth-order active-RC *Chebyshev* topology [26], [27], and has a −1-dB cutoff frequency of 650 kHz, considering both the channel bandwidth of 625 kHz and a frequency offset caused by the PLL. The four VGAs, which employ a resistive feedback amplifier topology to provide accurate voltage-gain levels with high linearity, gradationally amplify the output signal of the LPF. The AGC automatically adjusts each gain of the LPF and the VGAs according to a received signal strength indicator (RSSI) to deliver the baseband signal of a constant strength to an analog-to-digital converter (ADC). All of the VGAs and the LPF use a two-stage *RC* compensated operational amplifier (opamp) [28], which has a dc gain of 62 dB and a phase margin of 105° at a 66.5-MHz unit-gain bandwidth.

To mitigate the dc-offset problem in Fig. 9, the DCOC circuit using an integrator is adopted, and a DCOC loop based on voltage-current negative feedback [20] is applied from the VGAs to the LPF. Because the dc null tone in the TVWS-OFDM signal is located from 0 Hz to 4.88 kHz, the high-pass cutoff frequency in the DCOC loop is set to 1 kHz. Accordingly, a loss of the desired baseband signal can be avoided. To provide sufficient feedback current through R_{D2}, the opamp in the DCOC consumes about two times the dc current compared to the opamps in the VGAs and the LPF. The feedback capacitor C_F of the integrator is externally implemented owing to its large size.

B. Transmitter

The proposed I-Q direct-conversion transmitter consists of a Tx LPF, a Tx VGA, an up-conversion mixer, and a two-stage DA. To filter out the quantization noise of the quadrature baseband signal delivered from the DAC, the fifth-order active-RC *Chebyshev* LPF was also adopted and placed at the front in the transmitter. Following the LPF, to adjust the output power level of the transmitter, the Tx VGA provides a voltage attenuation from −6 dB to 0 dB with a 1-dB step.

To perform the frequency up-conversion with I-Q modulation in the transmitter, we used a single-balanced quadrature voltage-sampling passive mixer [18], [19] as shown in Fig. 10. Driven by a quadrature 25% duty-cycle LO signal, it produces no LO leakage or I-Q cross-talk

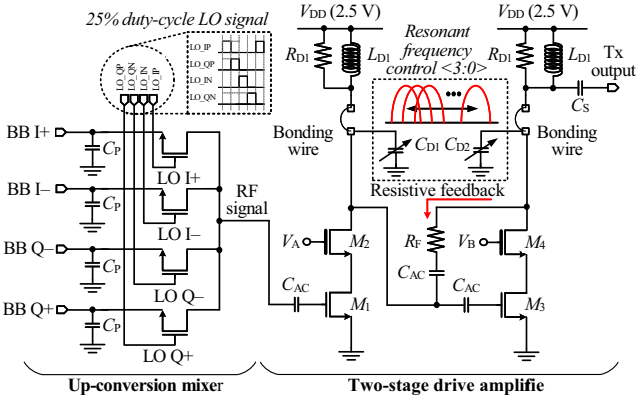

Fig. 10. Proposed up-conversion mixer and drive amplifier in the transmitter.

issues [18]. In addition, the single-ended output of the mixer permits the adoption of the single-ended drive amplifier, leading to a lower dc power consumption in the transmitter. In Fig. 10, C_P is used to remove unwanted spurious signals created at the mixer switches.

According to FCC regulations [5], the PSD of the adjacent channel should be at least 55.4 dB lower than the PSD of the main channel. To comply with this regulation, we propose a two-stage cascode driver amplifier (DA), as depicted in Fig. 10. The first DA is biased in class-A to achieve a large output signal for the following stage, and the second DA is biased in class-AB for better power efficiency. The voltage-current resistive feedback loop (R_F and C_{AC}) in the second DA further improves the linearity of the overall DA by reducing its nonlinear distortion [29]. The simulated results of the proposed DA show an OP1 dB of +15.5 dBm and an output third-order intercept point (OIP3) of +29 dBm from a 2.5-V supply. Consequently, an average output power level of more than 0 dBm can be achieved for the transmitter with a back-off of 10 dB. To support a wide frequency range of 470 MHz to 698 MHz, the proposed DA employs the resonant *RLC* loads (R_{D1}-L_{D1}-C_{D1}, and R_{D2}-L_{D2}-C_{D2}), which are varied by adjusting C_{D1} and C_{D2} with 4-bit control. The resistors (R_{D1} and R_{D2}) and inductors (L_{D1} and L_{D2}) in the loads are externally implemented to reduce the chip area. The cascode transistors (M_2 and M_3) of the DA are realized using thick-oxide metal-oxide semiconductor field-effect transistors (MOSFETs) to ensure that they withstand a high voltage swing.

C. 25% Duty-Cycle LO Generator and PLL

Figure 11(a) illustrates a simplified block diagram of the proposed quadrature 25% duty-cycle LOG, which consists

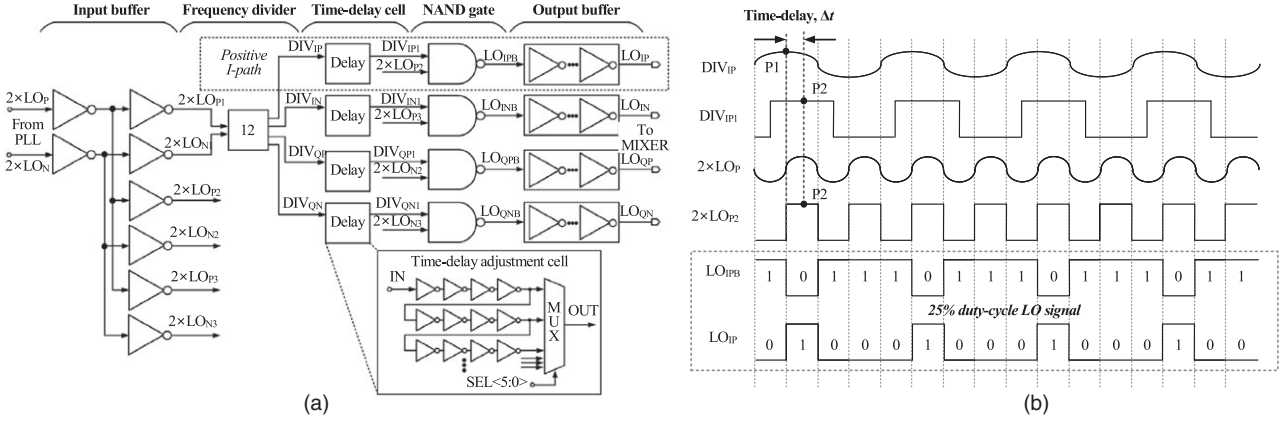

Fig. 11. Proposed 25% duty-cycle LO generator: (a) block diagram and (b) timing diagram (positive I-path only).

of input and output buffers, frequency dividers, time-delay cells, and NAND gates. Figure 11(b) shows a timing diagram of only the positive I-path signals in the 25% duty-cycle LOG.

In Fig. 11(a), the proposed LOG synthesizes a 25% duty-cycle LO signal by performing a logical NAND function for two input signals: one is a LO frequency signal of 470 MHz–698 MHz generated in the frequency divider, and the other is a 940-MHz–1,396-MHz signal, which is two times the LO frequency delivered from the PLL. The input sinusoidal signals ($2 \times LO_P$ and $2 \times LO_N$) are first reshaped into full-scaled square waves by the input buffer for the following frequency divider and NAND gates. The frequency divider generates the quadrature LO frequency signal by dividing the double LO frequency by two.

In Fig. 11(a), a propagation delay caused by the input buffer and the frequency divider are very frequency dependent. Therefore, when the LO frequency moves to the wanted frequency in the frequency band of 470 MHz–698 MHz, the two input signals of the NAND gate are out of synchronization and the 25% duty-cycle of the LO signal cannot be correctly synthesized. To overcome this problem, a time-delay cell, which consists of a six-to-one multiplexer and inverters, is used before the NAND gate to maintain the synchronization of the two signals of the NAND gate. In Fig. 11(b), the time-delay cell produces an adjustable time delay (Δt) between P1 and P2, where P1 is the peak point of DIV_{IP}, and P2 is the center point of $2 \times LO_{P2}$'s pulse interval. As a result, the 25% duty-cycle signal (LO_{IPB}) can be stably synthesized by the NAND function of two synchronized signals (DIV_{IP1} and $2 \times LO_{P2}$). Finally, using the output buffer comprised of an array of inverters, the synthesized 25% duty-cycle signals are inverted and delivered to the RF BPF and up/down-conversion mixers.

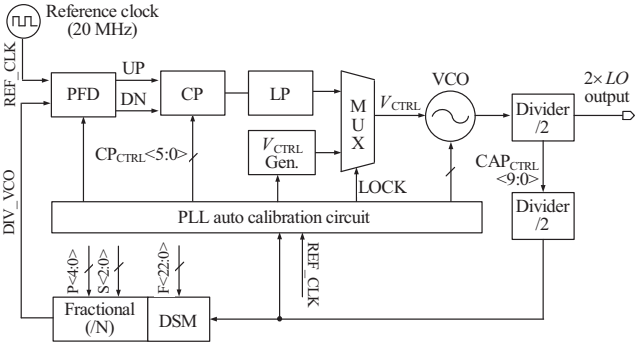

Fig. 12. Block diagram of the phase-locked loop (PLL).

Figure 12 shows the proposed delta-sigma fractional-N PLL with high-frequency resolution. It has a complementary differential voltage-controlled oscillator (VCO) that produces differential signal tone between 1,880 MHz and 2,792 MHz (that is, four times the LO frequency). The output signal of the VCO is converted into a quadrature 940-MHz-to-1,396-MHz signal by a divide-by-two circuit, and then delivered to the 25% duty-cycle LOG shown in Fig. 11(a). In the PLL, the bandwidth of the external loop filter is set to 100 kHz in order to favorably remove the phase noise of the VCO and quantization noise of the delta-signal modulator.

VI. Measurement Results and Summary

The proposed TVWS-OFDM RF transceiver was implemented using 0.13-μm CMOS technology, and it consumes 47 mA in the transmit mode and 35 mA in the receive mode. The dc power consumption for the sub-blocks of the transceiver is summarized in Table 2. Figure 13 shows the fabricated chip, which is composed of two main parts, that is, the RF transceiver and the digital part. Although the digital part is not described in this paper, some parts, such as

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the ADC/DAC, modem, and media access control, were designed and integrated into the system-on-chip (SoC) to fully support TVWS-OFDM systems. The fabricated SoC was 128-pin packaged and mounted on an FR-4 board to evaluate the chip performance, as shown in Fig. 14.

Figure 15 shows the measured phase noise when the proposed delta-sigma fractional-N PLL produces a 940-MHz carrier. The measured phase noise is about −92.3 dBc at a 100-kHz offset and −127.1 dBc at a 1-MHz offset, which almost satisfies the design requirements discussed in section II.

Table 2. Dc power consumption for sub-blocks.

Blocks		Power consumption
Receiver	LNA	7.9 mA @ 1.5 V
	G_m	4.1 mA @ 1.5 V
	TIA	3.8 mA @ 2.5 V
	Rx VGAs, Rx LPF, and DCOC	8.8 mA @ 1.5 V
Transmitter	DA	32 mA @ 2.5 V
	Tx VGA, Tx LPF	4.8 mA @ 1.5 V
	PLL and LOG	10.3 mA @ 1.2 V

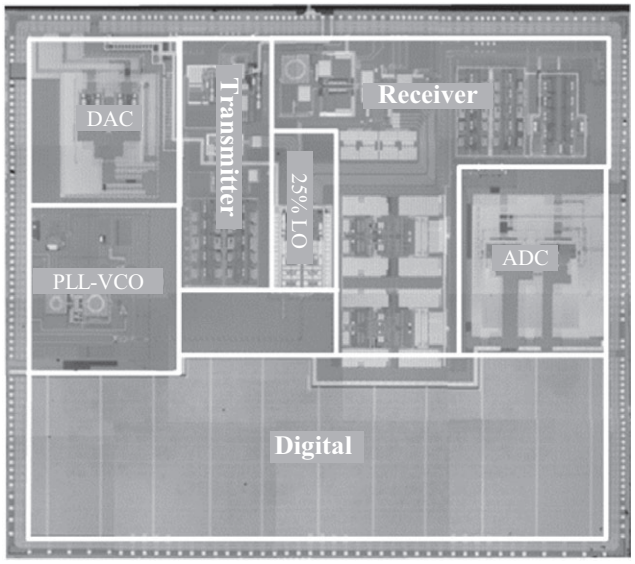


Fig. 13. Microphotograph of fabricated chip (6.8 mm × 6 mm).

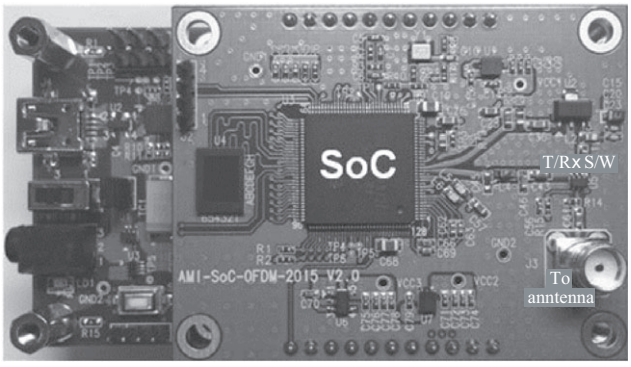


Fig. 14. Implemented TVWS-OFDM module (8 cm × 4.5 cm).

Figure 16 shows the transmitted output PSDs centered at 471.125 MHz, 575.625 MHz, and 681.125 MHz, respectively, which were QPSK-modulated. The measured output powers are greater than +1 dBm, and each PSD of the adjacent channel at a 1.125-MHz offset is at least 57-dB lower than the PSD of the main channel. These results are derived from the proposed DA with a sufficient back-off of 13 dB, and well satisfy the FCC regulation of 55.4 dBc.

Figure 17 shows a plot of the input return loss (S_{11}) of the receiver. By using the multiband function of the LNA, the value of S_{11} is less than −10 dB in the TV band spanning 470 MHz–698 MHz.

For the receiver, we evaluated the interference filtering performance, which was determined by RF band-pass filtering and low-pass filtering in the RF front-end, and channel filtering in the baseband circuits. An RF signal tone of −97 dBm and a 3-MHz offset blocker of −20 dBm were simultaneously applied to the receiver operating in a high-gain mode. At the receiver output, the strength of the blocker is 38-dB below that of the down-converted signal, as shown in Fig. 18. This interferer attenuation of 115 dB, (which resulted from an attenuation of 37 dB at the RF front-end and 78 dB at the baseband circuits), demonstrates the superior filtering performance of the proposed receiver.

We also evaluated the out-of-channel linearity performances of the receiver in high-gain mode. Figure 19 shows the measured out-of-channel IIP3 of −1.5 dBm using two tones at 3-MHz and 5.6-MHz, where the third-order intermodulation (IM3) tone is located at 400 kHz. The measured out-of-channel IIP2 for two blockers at 3-MHz and 3.4-MHz was +42 dBm.

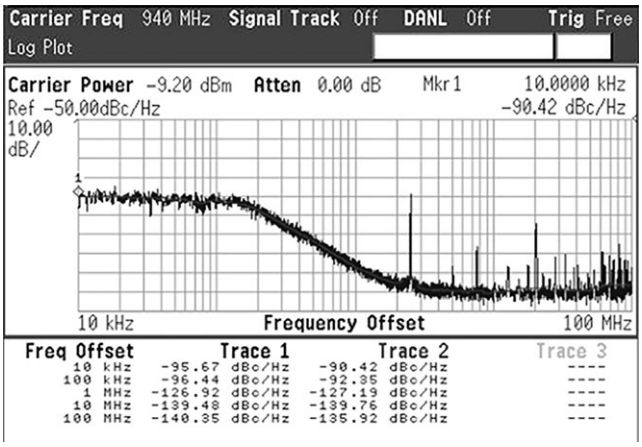
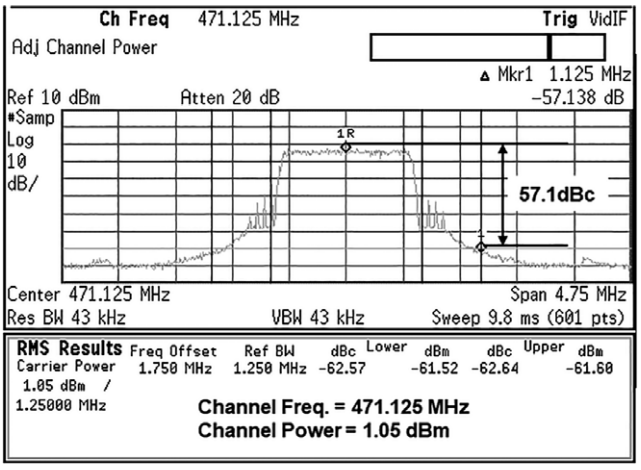
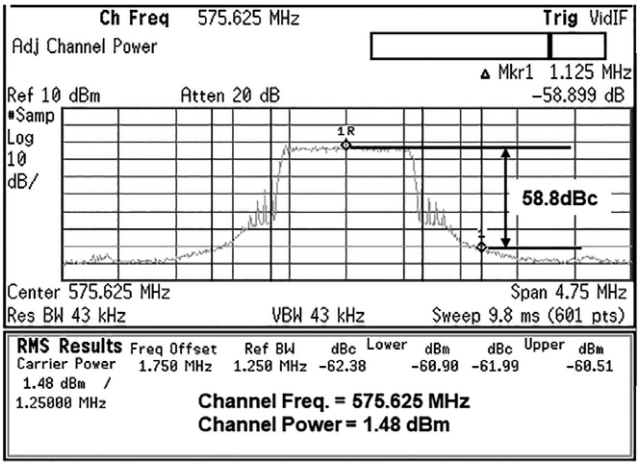


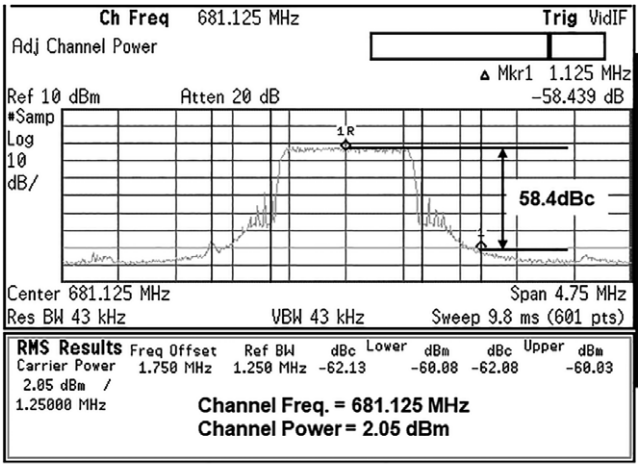
Fig. 15. Measured phase noise of the PLL.



(a)



(b)



(c)

Fig. 16. Transmitted output PSD centered at (a) 471.125 MHz, (b) 575.625 MHz, and (c) 681.125 MHz.

The fabricated SoC showed a minimum sensitivity level of −102 dBm with a packet-error-rate (PER) of 3% for the MCS0 mode. Table 3 summarizes the measured sensitivity levels for three MCS modes. The measured sensitivity levels all satisfied the IEEE 802.15.4m TVWS-OFDM PHY. The

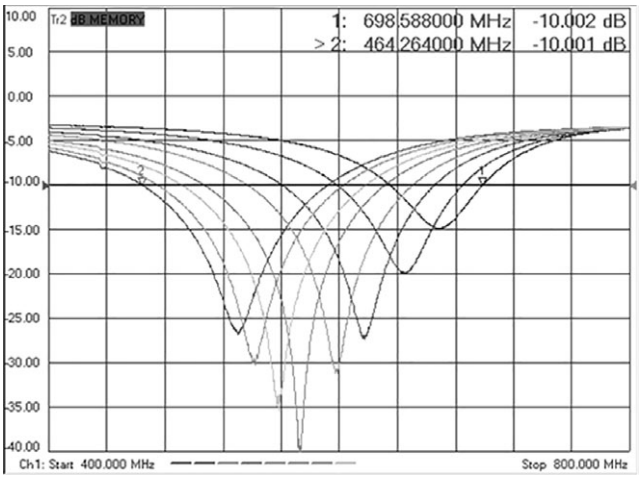


Fig. 17. Input return loss (S_{11}) of the receiver.

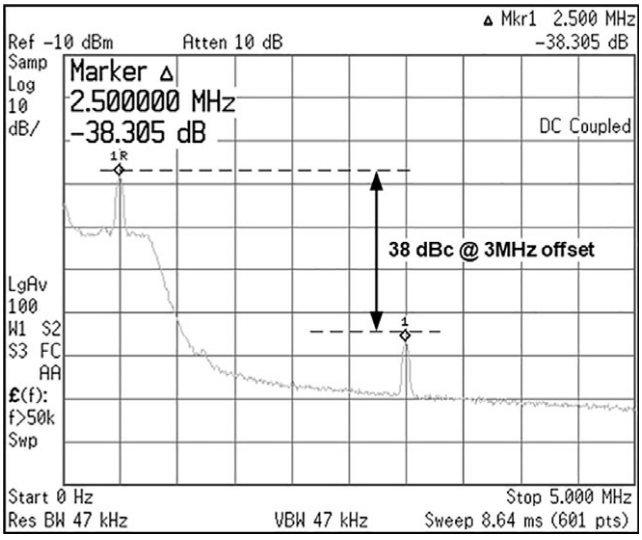


Fig. 18. Measured output spectrum of the receiver.

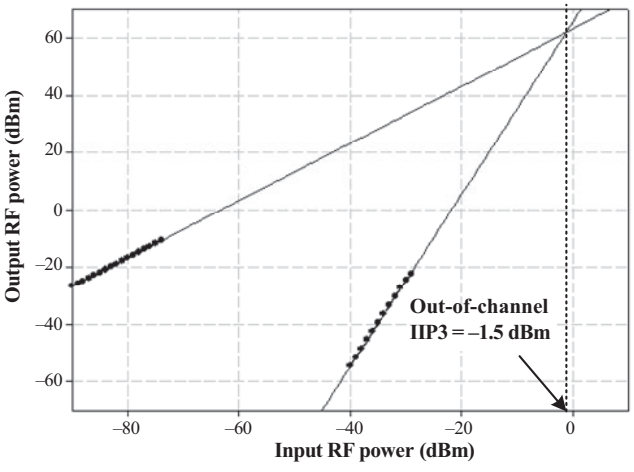


Fig. 19. Measured out-of-channel IIP3.

blocking sensitivity level for the MCS0 mode was also measured, as shown in Fig. 20. In the presence of a −20-dBm blocker at a 3-MHz offset, the sensitivity level was slightly degraded by 4 dB from −102 dBm to −98 dBm. Table 4 shows a comparison of the performances of the proposed receiver and the previously reported receivers.

VII. Public Demonstration

The conceptual diagram of smart metering using the TVWS link has been already shown in Fig. 2. Metering data can be sent to the utility providers via the TVWS link for billing and real-time monitoring. Figure 21 shows the implemented TVWS-OFDM modules, which were connected to water, electricity, and gas meters for AMI applications.

We performed a public demonstration of smart electricity-metering using 100 TVWS-OFDM modules in a rural district in the Republic of Korea. For simplicity, two data collection units (DCUs) and 20 houses are shown in Fig. 22. Once a day, electricity-metering data from the houses were transmitted to the DCUs via the TVWS link. Then, they were gathered via other backbone networks employed by the power provider. During a 30-day period,

Table 3. Performance summary.

Parameters	Measured results
RF frequency	470 MHz–698 MHz
Sensitivity level (PER < 3%)	
@ 390 kbps (MCS0, BPSK)	−102 dBm
@ 780 kbps (MCS1, QPSK)	−99 dBm
@ 1.56 Mbps (MCS2, 16-QAM)	−93 dBm
Blocking sensitivity level (MCS0)*	−98 dBm
Out-of-channel IIP3	−1.5 dBm
Out-of-channel IIP2	+42 dBm
Tx average power	1 dBm
Tx PSD to adjacent channel	<−57 dBc
Tx output $CP_{1\ dB}$**	+15 dBm
Phase noise PLL	−127.1 dBc/Hz @1 MHz
Rx mode current	35 mA
Tx mode current	47 mA
Supply voltage	1.2 V/1.5 V/2.5 V
CMOS technology	0.13 μm

*In the presence of a -20-dBm blocker at 3-MHz offset.
**1-dB compression point.

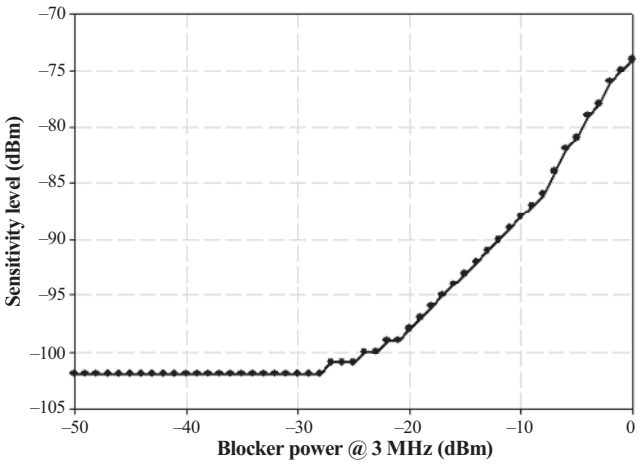


Fig. 20. Measured blocking sensitivity level (PER < 3%) for MCS0 mode.

Table 4. Performance comparison with previously reported receivers.

Parameters	Proposed	[10]	[11]	[12]
Technology	130 nm	65 nm	65 nm	40 nm
Architecture	LNA-first	LNA-first	Mixer-first	Mixer-first
RF frequency (GHz)	0.47–0.7	0.4–0.9	0.1–2.4	0.4–6
Location of targeted interferers	In-band	Out-of-band	Out-of-band	Out-of-band
Sensitivity level (dBm)	−102	N/A	N/A	N/A
Gain (dB)	105	34	70	70
Noise figure (dB)	4.8	4	4 ± 1	3
Out-of-band IIP3 (dBm)	−1.5*	+16	+25	+10
Out-of-band IIP2 (dBm)	+42*	+56	+56	N/A
Power consumption (mW)	42–88	60**	37–70	64–100
Supply voltage (V)	1.2/1.5/2.5	1.2	1.2/2.5	1.2/2.5

*Out-of-channel IIP3, Out-of-channel IIP2.
**Does not include a synthesizer.

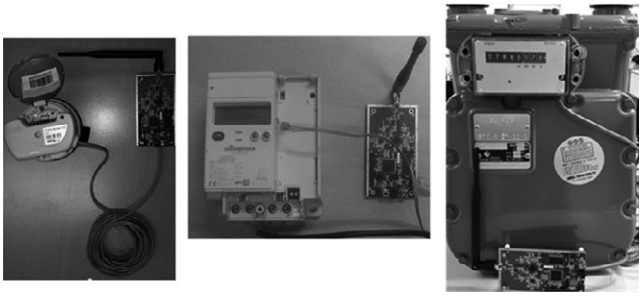


Fig. 21. TVWS-OFDM modules connected to water, electricity, and gas meters.

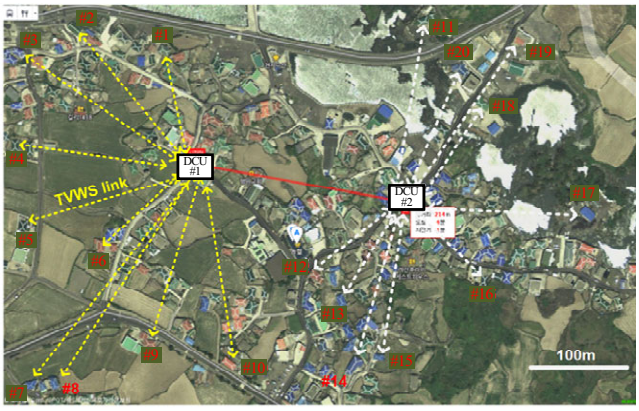


Fig. 22. Public demonstration in a rural area in the Republic of Korea. For simplicity, only two DCUs and 20 houses are shown.

all electricity-metering data for the 100 houses were successfully received by the power supplier.

VIII. Conclusion

This paper presented an IEEE 802.15.4m-compliant TVWS-OFDM RF transceiver, which was implemented using 0.13-μm CMOS technology. Because the proposed receiver adopted high-Q band-pass filtering using an RF front-end and high-order LPF in the baseband, it can tolerate interference as high as −20 dBm at a 3-MHz offset, while detecting a minimum input signal of −97 dBm. The proposed transmitter well satisfies the FCC regulation with highly linear characteristics. The overall measurement results show that the fabricated SoC favorably supports the IEEE 802.15.4m standard. We successfully carried out a public demonstration of smart electricity metering using the implemented TVWS-OFDM modules.

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