

## Article

# Graphene Oxide/Polystyrene Bilayer Gate Dielectrics for Low-Voltage Organic Field-Effect Transistors

Sooji Nam <sup>1,\*</sup> , Yong Jin Jeong <sup>2</sup>, Joo Yeon Kim <sup>1</sup>, Hansol Yang <sup>2</sup> and Jaeyoung Jang <sup>2,\*</sup> 

<sup>1</sup> Realistic Display Research Group, Electronics and Telecommunications Research Institute, Daejeon 34129, Korea; jooyeon.kim@etri.re.kr

<sup>2</sup> Department of Energy Engineering, Hanyang University, Seoul 04763, Korea; il5range@gmail.com (Y.J.J.); yhsyhs2@hanyang.ac.kr (H.Y.)

\* Correspondence: sjnam15@etri.re.kr (S.N.); jyjang15@hanyang.ac.kr (J.J.);  
Tel.: +82-2-2220-2334 (S.N.); +82-42-860-1479 (J.J.)

Received: 3 December 2018; Accepted: 17 December 2018; Published: 20 December 2018



**Abstract:** Here, we report on the use of a graphene oxide (GO)/polystyrene (PS) bilayer as a gate dielectric for low-voltage organic field-effect transistors (OFETs). The hydrophilic functional groups of GO cause surface trapping and high gate leakage, which can be overcome by introducing a layer of PS—a hydrophobic polymer—onto the top surface of GO. The GO/PS gate dielectric shows reduced surface roughness and gate leakage while maintaining a high capacitance of 37.8 nF cm<sup>−2</sup>. The resulting OFETs show high-performance operation with a high mobility of 1.05 cm<sup>2</sup> V<sup>−1</sup> s<sup>−1</sup> within a low operating voltage of −5 V.

**Keywords:** graphene oxide; polystyrene; gate dielectric; low voltage; organic field-effect transistor

## 1. Introduction

Organic field-effect transistors (OFETs) have attracted great attention because of their potential applications in flexible and bendable displays with high field-effect mobility, low-temperature processability, and flexibility [1,2]. Although high-performance OFETs have been consistently reported in the past decade, most of the studies have focused on devices employing rigid inorganic dielectrics, such as silicon dioxide (SiO<sub>2</sub>) and aluminum oxide [3–5]. Therefore, polymer dielectrics, such as poly(methyl methacrylate), poly(vinyl alcohol), polyimide, and poly(4-vinylphenol), have been extensively studied as alternatives to inorganic dielectric layers in OFETs because the former offer the advantages of solution processes and the need for flexible device applications [6–9]. However, single layers of such polymer dielectrics have some limitations with regard to working in low-voltage driving OFETs. Realization of low-voltage OFETs necessitates the use of high-capacitance ( $C_i$ ) gate dielectrics. In general,  $C_i$  can be expressed as  $C_i = k \cdot \epsilon_0 \cdot d^{-1}$ , where  $k$  is the dielectric constant,  $\epsilon_0$  is the permittivity of the dielectric material, and  $d$  is the dielectric thickness. From this equation, it is clear that the use of a high- $k$  gate dielectric film or a reduction of the thickness of the dielectric layer is necessary for increasing  $C_i$ . With only a few exceptions, polymer dielectrics generally have low  $k$ ; thus, the thickness of the polymer layer must be reduced to a scale of at least a few nanometers to increase  $C_i$ . However, the insulating properties of polymer dielectrics degrade severely with a reduction in film thickness [10]. Therefore, it is highly challenging to develop novel gate dielectric materials that simultaneously are thin and exhibit good dielectric properties with high  $k$  for application to low-voltage OFETs.

On account of its outstanding electrical, mechanical, and chemical properties, graphene has been intensively studied for application as a semiconductor, electrode, and encapsulation layer in OFETs [4,11–14]. In particular, graphene derived from graphene oxide (GO), which is referred to as reduced GO (rGO), has attracted much attention for application to flexible devices because of its

thinness, excellent electrical properties, and mechanical flexibility [15–17]. Most researchers have focused on achieving good electrical properties of rGO; however, it is notable that GO has potential to be used as a gate dielectric layer of OFETs since it possesses insulating properties and a very high  $k$  [18–20]. Nevertheless, neither the dielectric properties of GO-based materials nor their application as dielectric layers of OFETs has been studied satisfactorily. To enable the use of GO as a dielectric layer of OFETs, its surface properties need to be modified because the hydrophilic hydroxyl and epoxide functional groups on the GO surface can function as trap sites and reduce the device characteristics. Several studies have attempted to passivate the hydrophilic surface of gate dielectrics with hydrophobic polymers to realize high-performance and reliable OFETs [21,22].

Here, we report on the feasibility of using GO as the gate dielectric layer of low-voltage OFETs. We attempted to modify the surface of GO by overlaying it with the hydrophobic polymer polystyrene (PS). Through atomic force microscopy (AFM), X-ray diffraction (XRD), and two-dimensional grazing incidence X-ray diffraction (2D-GIXD) analysis, we confirmed that the GO/PS bilayer gate dielectric reduced the surface roughness and increased the crystallinity of the organic semiconductor. We also found that the GO/PS bilayer gate dielectric resulted in a reduced gate leakage current, which, in turn, drastically enhanced the electrical properties of OFETs within a low operating voltage of  $-5$  V.

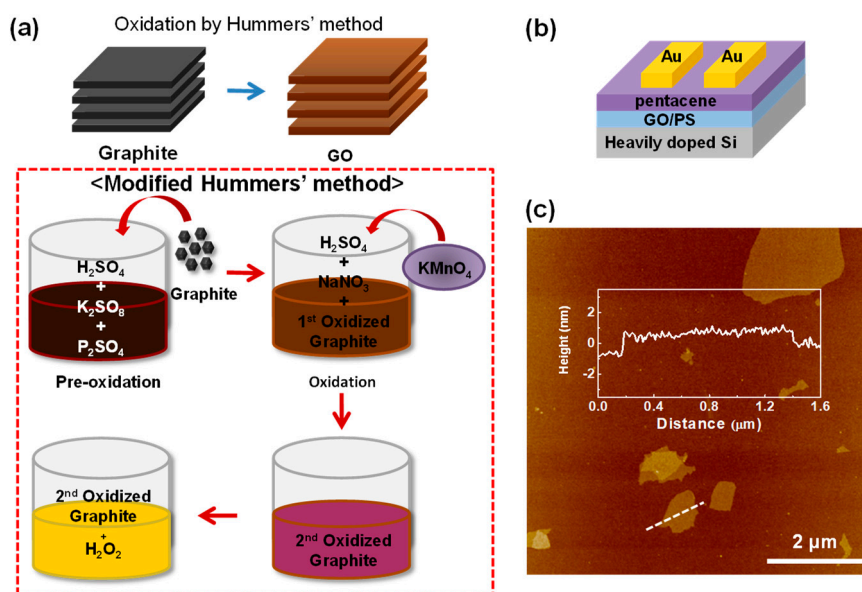
## 2. Materials and Methods

### 2.1. Film Characterization

GO was synthesized using the modified Hummers' method, as shown in Figure 1; further details of this synthesis have been reported in a previous paper [16]. Final dried GO flakes were dispersed in a deionized water/methanol (2:1) mixed solvent (1.5 wt %) by using a sonicator. For film characterization, GO solutions were spin-coated onto Si substrates at 1200 rpm for 60 s and cured at  $120$  °C for 30 min. To form the GO/PS bilayer, 0.7 wt % PS solution in toluene was spin-coated onto the GO films at 4000 rpm for 45 s, and then cured at  $90$  °C for 20 min. The GO and PS solutions were spin-coated in air. The film thickness was measured by ellipsometry (J.A. Woollam). The surface morphologies and  $C_i$  were characterized using an atomic force microscope (MultiMode SPM, Digital Instruments Inc., Santa Barbara, CA, USA) and the HP 4284A precision LCR meter (Agilent, Santa Clara, CA, USA), respectively. To investigate the crystallinity of the organic semiconductor films, a 50 nm-thick pentacene film was deposited onto various dielectric layers (GO, GO/PS, and PS). The pentacene films were investigated via XRD and 2D-GIXD experiments, which were performed at the 10C1 and 4C2 beamlines (wavelength =  $1.38$  Å), respectively, at the Pohang Accelerator Laboratory in Korea. The measurements of  $C_i$  and leakage current were performed using a metal–insulator–metal structure.

### 2.2. Device Fabrication

For the fabrication of OFETs, highly  $p$ -doped Si wafers were used as gate electrodes and substrates. After piranha cleaning and consecutive DI water washing of the substrates, the GO solutions were spin-coated onto them at 1200 rpm for 60 s and cured at  $120$  °C for 30 min. Then, 0.7 wt % PS solution in toluene was spin-coated onto the GO films at 4000 rpm for 45 s, and cured at  $90$  °C for 20 min. A 50 nm-thick pentacene film, serving as the active layer, was deposited onto the GO/PS dielectric at a rate of  $0.2$  Å  $s^{-1}$  by means of an organic molecular beam deposition system. The film deposition conditions were kept identical for the film analysis and the device. Finally, Au source/drain electrodes with a thickness of 100 nm each were deposited using a thermal evaporator (Figure 1b). Electrical measurements were conducted using Keithley 2400 and 236 source/measure units. The electrical properties were evaluated in the dark under ambient conditions. The device parameters were calculated on the basis of the transfer curves in the saturation regime by using the equation  $I_d = (W/2L) \cdot \mu \cdot C_i \cdot (V_g - V_{th})^2$ ; here,  $I_d$ ,  $\mu$ ,  $V_g$ , and  $V_{th}$  are the drain current, field-effect mobility, gate voltage, and threshold voltage, respectively;  $W$  and  $L$  are the channel width and length, respectively; and  $C_i$  is the capacitance per unit area of the GO/PS gate insulator.

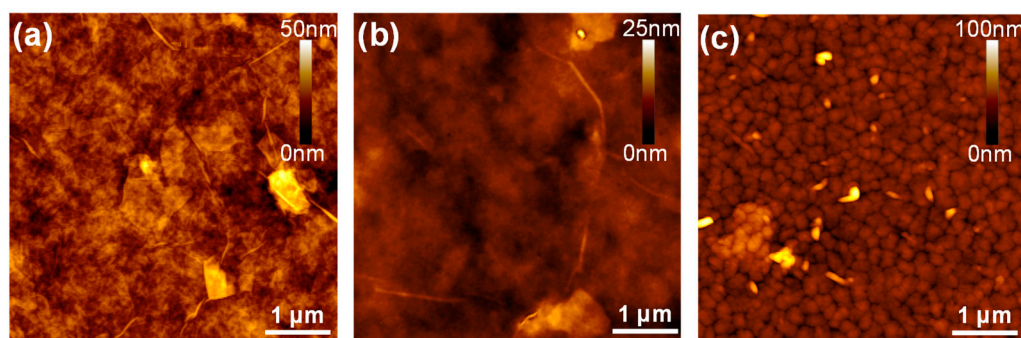


**Figure 1.** (a) Schematic illustration of procedure for synthesizing graphene oxide (GO) by modified Hummers' method. (b) Schematic device structure of organic field-effect transistor (OFET) used in this study. (c) Height-mode atomic force microscopy (AFM) topographs of GO pieces obtained from highly diluted solution (the inset shows the height profile of a GO slice).

### 3. Results

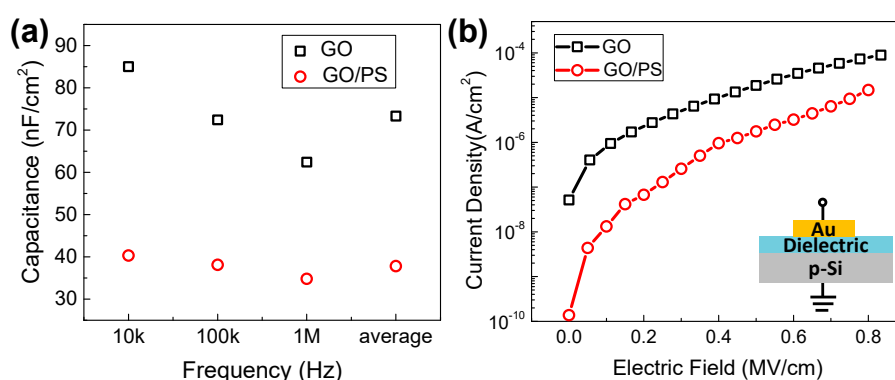
#### 3.1. Film Characterization

The surface morphologies of the synthesized GO, GO/PS bilayer, and pentacene deposited on the GO/PS bilayer were studied by AFM. Figure 1c shows the synthesized GO pieces obtained from a highly diluted solution; the pieces are in the form of flat sheet-type structures with an average sheet size of about 600 nm (with some size deviation from sheet to sheet). The inset of Figure 1c shows the height profile of a 1.5–2.0 nm GO slice, which reveals that the GO flakes are well separated by a single layer. Figure 2a,b, respectively, show the surface morphologies of the GO film (thickness of 70 nm) and PS-coated GO (GO/PS bilayer, total thickness of 75 nm) film used in this system. As can be seen in the AFM images, coating the PS layer on the GO surface can significantly reduce the surface root-mean-square ( $R_q$ ) of the GO film, from 4.91 nm to 2.17 nm, and improve the uniformity. Figure 2c shows the morphology of the pentacene film deposited on the GO/PS film; the average grain size is approximately 250 nm, and  $R_q$  roughness is 7.8 nm.



**Figure 2.** Height-mode AFM topographs of (a) GO film, (b) polystyrene (PS)-coated GO (GO/PS) film, and (c) pentacene film deposited on GO/PS bilayer dielectric.

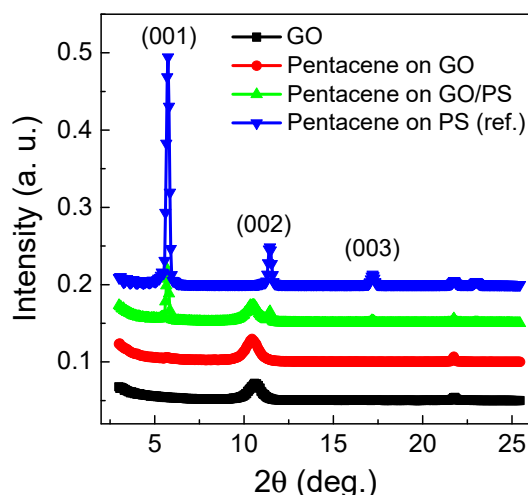
To measure the gate dielectric properties of the GO and GO/PS bilayer films, metal–insulator–metal capacitors (herein, Au–GO–heavily p-doped Si wafer or Au–GO/PS–heavily p-doped Si wafer) were fabricated. Figure 3 shows the measured  $C_i$  and electric-field-dependent gate leakage current density. The  $C_i$  value of GO decreases from 85 to 62.4 nF cm<sup>−2</sup> (average: 73.3 nF cm<sup>−2</sup>) and that of GO/PS decreases from 40.3 to 34.8 nF cm<sup>−2</sup> (average: 37.8 nF cm<sup>−2</sup>), as the frequency increases from 10 kHz to 1 MHz, which agrees well with the reported  $C_i$  value of a GO film with a similar thickness [13]. Although the  $C_i$  value of the GO/PS bilayer is smaller than that of the GO film because of the low dielectric constant of PS, the former  $C_i$  is high enough for GO/PS to serve as a dielectric layer for low-voltage operation of OFETs. As can be observed from the data in Figure 3a, the  $C_i$  values of the GO film and the GO/PS bilayer decrease by about 27% and 14%, respectively, with an increase in the frequency to up to 1 MHz; this indicates that the GO/PS bilayer has fewer mobile impurities on the dielectric surface than does the GO single layer. Figure 3b shows the electric-field-dependent gate leakage current. The GO single layer shows a high leakage current (10<sup>−4</sup>–10<sup>−7</sup> A cm<sup>−2</sup>), whereas the gate leakage current of GO/PS bilayer is one order or more less than that of the GO film; this indicates the excellent electrical strength of the GO/PS bilayer. As mentioned in the introduction part, since the hydrophilic hydroxyl and/or epoxide functional groups on the GO surface can function as trap sites and reduce the device characteristics, it is necessary to modify the GO surface with the hydrophobic layer. The leakage current reduction can be attributed to the surface passivation of the hydrophilic GO with the hydrophobic PS, which could facilitate the use of GO as a dielectric of the OFETs.



**Figure 3.** Analysis of dielectric properties of GO and GO/PS films: (a) frequency dependence of capacitance of GO and GO/PS films and (b) current density–electric field characteristics of GO and GO/PS films. The inset shows a schematic diagram of the metal–insulator–metal structure that induces the current density–electric field characteristics.

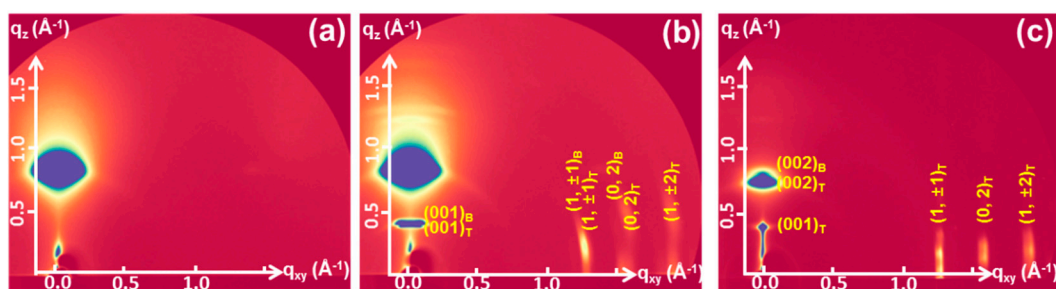
### 3.2. Molecular Ordering and Crystallinity

The molecular ordering and crystallinity of the pentacene layers on various dielectrics (GO, GO/PS, and PS) were investigated by out-of-plane XRD and 2D-GIXD analysis. Figure 4 shows the XRD patterns of the GO film and pentacene films on the various dielectrics. As can be seen from the black and blue graphs in Figure 4, the diffraction peaks of the GO film correspond to (001) and (002) planes, and an interlayer spacing ( $d_{001}$ ) of  $8.3 \pm 0.1$  Å, and the diffraction peaks of the pentacene layer on the PS substrate correspond to (001), (002), and (003) planes with  $d_{001}$  of  $15.5 \pm 0.1$  Å; these results are in good agreement with literature values [23,24]. Diffraction peaks of only GO are observed in the XRD patterns of pentacene on the GO film; on the other hand, in the XRD patterns of pentacene on the GO/PS bilayer film, thin-film-phase diffraction peaks of pentacene are observed, as seen in Figure 4. This indicates that the pentacene film is more ordered and has more aligned crystalline on the GO/PS bilayer film than on the GO film.



**Figure 4.** X-ray diffraction (XRD) patterns of GO film and pentacene films deposited on various dielectrics (GO, GO/PS, and PS).

Since the crystal structure of organic semiconductors affects the carrier transport properties, analysis of the crystal structures of thin-film organic semiconductors is crucial for understanding the electrical and physical properties of OFETs. Figure 5 shows 2D-GIXD scan images of the GO film and pentacene films deposited on the various dielectrics. In Figure 5a, a broad (001) plane of GO is observed in the  $q_z$  direction (direction parallel to the substrate), which corresponds to the XRD result of GO in Figure 4. The 2D-GIXD patterns of pentacene in Figure 5b,c reveal that the pentacene film on the GO dielectric contains both a “thin-film phase” and a “bulk phase” in the  $q_z$  and  $q_{xy}$  directions, whereas the pentacene film on the GO/PS bilayer shows a relatively highly oriented “thin-film phase” in the  $q_z$  and  $q_{xy}$  directions. In the case of carrier transport in pentacene, the  $\pi$ - $\pi$  overlap depends largely on the molecular alignment along the in-plane direction,  $q_{xy}$ , and not the out-of-plane direction,  $q_z$ . It has been reported that the bulk phase corresponds to a tilted molecular orientation and the poorest degree of  $\pi$ - $\pi$  overlap [25]. Therefore, the 2D-GIXD results indicate that the pentacene grains are well-stacked with fewer mismatched and tilted crystalline domains on the GO/PS bilayer than on the GO film.



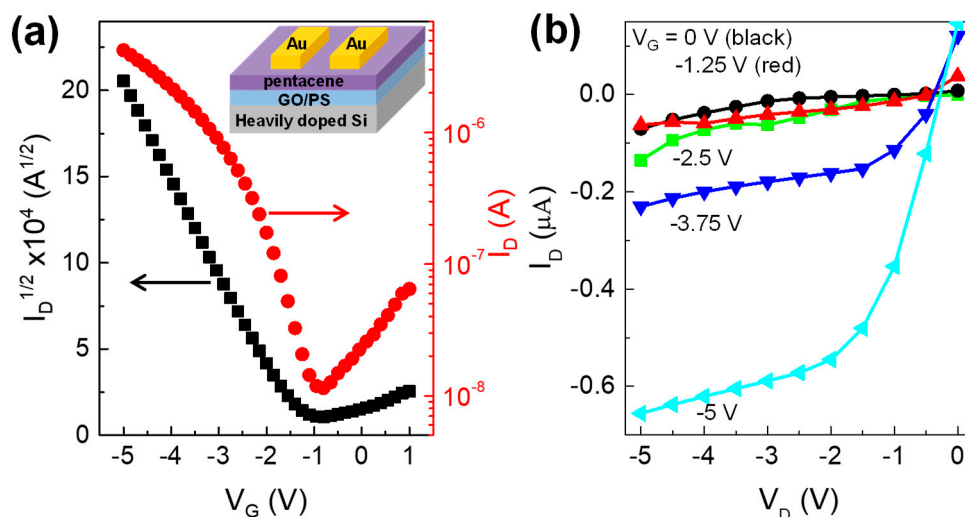
**Figure 5.** Two-dimensional grazing incidence X-ray diffraction (2D-GIXD) scan images of (a) GO film, (b) pentacene films deposited on GO, and (c) GO/PS dielectric. Subscripts “T” and “B” represent “thin-film phase” and “bulk phase,” respectively.

### 3.3. Device Characterization

Figure 6a shows the transfer characteristics in the saturation regime ( $V_D = -5$  V) for a pentacene-based OFET with a GO/PS bilayer dielectric ( $W/L = 1000/100$   $\mu\text{m}$ ). In the case of OFET device, using GO as a dielectric layer, the transistor characteristics were not shown despite the high  $C_i$  value of GO film, which is due to the high surface roughness and high leakage of GO film, and the poor crystallinity of pentacene on the GO dielectric. By contrast, the OFET with the GO/PS bilayer



dielectric exhibits a high  $\mu$  of  $1.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , an on/off ratio exceeding  $10^2$ , and  $V_{\text{th}}$  of  $-1.4 \text{ V}$  with  $C_i$  of  $37.8 \text{ nF cm}^{-2}$ . Figure 6b shows the output characteristics ( $I_D$  vs.  $V_D$  curves at  $V_G = 0, -1.25, -2.5, -3.75$ , and  $-5 \text{ V}$ ) of the OFET with the GO/PS bilayer dielectric. Although the OFET shows some leakage current at  $V_G = 0 \text{ V}$ , the device can be operated within  $-5 \text{ V}$  with clear saturation behavior. It is not easy to fabricate reproducible OFET devices (yield less than 50 %), however, this study successfully enabled the use of GO as a dielectric layer of low-voltage OFET with a high mobility.



**Figure 6.** (a) Transfer and (b) output characteristics of OFET with GO/PS bilayer dielectric under a single sweep mode ( $V_G = 0, -1.25, -2.5, -3.75$ , and  $-5 \text{ V}$  from black circles to cyan triangles). The inset in (a) shows a schematic of the device structure used in this study.

#### 4. Conclusions

In summary, we have successfully demonstrated a high-performance OFET with a GO/PS bilayer gate dielectric, which shows  $\mu$  of  $1.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and operates within a low voltage of  $-5 \text{ V}$ . The high performance of the device is attributed to the significant reduction in the surface roughness and gate leakage current through overlaying of the hydrophilic GO surface with hydrophobic PS, as well as to a significant increase in the crystallinity of the pentacene film on the GO/PS bilayer surface. We believe that this work provides a facile route for fabricating low-power-consumption electronic devices by taking advantage of the thinness and excellent insulating properties of GO, which have not been satisfactorily studied in the past.

**Author Contributions:** S.N. and J.J. conceived and designed the experiments; S.N. and Y.J.J. performed the experiments; all authors analyzed the data, discussed the results and wrote the manuscript.

**Funding:** This work was supported by the Institute for Information & Communications Technology Promotion (IITP) grant funded by the Korea government (MSIT) (2018-0-00202, Development of Core Technologies for Transparent Flexible Display Integrated Biometric Recognition Device) and also by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2018R1D1A1A02050420).

**Conflicts of Interest:** The authors declare no conflict of interest.

#### References

1. Heremans, P.; Tripathi, A.K.; Meux, A.J.; Smits, E.C.P.; Hou, B.; Pourtois, G.; Gelinck, G.H. Mechanical and Electronic Properties of Thin-Film Transistors on Plastic, and Their Integration in Flexible Electronic Applications. *Adv. Mater.* **2016**, *28*, 4266–4282. [[CrossRef](#)] [[PubMed](#)]

2. Jang, J.; Nam, S.; Im, K.; Hur, J.; Cha, S.N.; Kim, J.; Son, H.B.; Suh, H.; Loth, M.A.; Anthony, J.E.; et al. Highly Crystalline Soluble Acene Crystal Arrays for Organic Transistors: Mechanism of Crystal Growth During Dip-Coating. *Adv. Funct. Mater.* **2012**, *22*, 1005–1014. [[CrossRef](#)]
3. Kang, I.; An, T.K.; Hong, J.A.; Yun, H.J.; Kim, R.; Chung, D.S.; Park, C.E.; Kim, Y.H.; Kwon, S.K. Effect of Selenophene in a DPP Copolymer Incorporating a Vinyl Group for High-Performance Organic Field-Effect Transistors. *Adv. Mater.* **2013**, *25*, 524–528. [[CrossRef](#)] [[PubMed](#)]
4. He, D.; Zhang, Y.; Wu, Q.; Xu, R.; Nan, H.; Liu, J.; Yao, J.; Wang, Z.; Yuan, S.; Li, Y.; et al. Two-dimensional quasi-freestanding molecular crystals for high-performance organic field-effect transistors. *Nat. Commun.* **2014**, *5*, 5162. [[CrossRef](#)] [[PubMed](#)]
5. Nam, S.; Jang, J.; Park, J.J.; Kim, S.W.; Park, C.E.; Kim, J.M. High-Performance Low-Voltage Organic Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2012**, *4*, 6–10. [[CrossRef](#)] [[PubMed](#)]
6. Noh, Y.H.; Park, Y.; Seo, S.M.; Lee, H.H. Root cause of hysteresis in organic thin film transistor with polymer dielectric. *Org. Electron.* **2006**, *7*, 271–275. [[CrossRef](#)]
7. Subbarao, N.V.V.; Gedda, M.; Iyer, P.K.; Goswami, D.K. Enhanced environmental stability induced by effective polarization of a polar dielectric layer in a trilayer dielectric system of organic field-effect transistors: A quantitative study. *ACS Appl. Mater. Interfaces* **2015**, *7*, 1915–1924. [[CrossRef](#)]
8. Nketia-Yawson, B.; Lee, H.S.; Seo, D.; Yoon, Y.; Park, W.T.; Kwak, K.; Son, H.J.; Kim, B.S.; Noh, Y.Y. A Highly Planar Fluorinated Benzothiadiazole-Based Conjugated Polymer for High-Performance Organic Thin-Film Transistors. *Adv. Mater.* **2015**, *27*, 3045–3052. [[CrossRef](#)] [[PubMed](#)]
9. Yang, S.Y.; Shin, K.; Park, C.E. The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics. *Adv. Funct. Mater.* **2005**, *15*, 1806–1814. [[CrossRef](#)]
10. Jang, J.; Kim, S.H.; Hwang, J.; Nam, S.; Yang, C.; Chung, D.S.; Park, C.E. Photopatternable ultrathin gate dielectrics for low-voltage-operating organic circuits. *Appl. Phys. Lett.* **2009**, *95*, 073302. [[CrossRef](#)]
11. Nath, A.; Kong, B.D.; Koehler, A.D.; Anderson, V.R.; Wheeler, V.D.; Daniels, K.M.; Boyd, A.K.; Cleveland, E.R.; Myers-Ward, R.L.; Gaskill, D.K.; et al. Universal conformal ultrathin dielectrics on epitaxial graphene enabled by a graphene oxide seed layer. *Appl. Phys. Lett.* **2017**, *110*, 013106. [[CrossRef](#)]
12. Jang, J.; Park, J.; Nam, S.; Anthony, J.E.; Kim, Y.; Kim, K.S.; Kim, K.S.; Hong, B.H.; Park, C.E. Self-organizing properties of triethylsilylethynyl-anthradithiophene on monolayer graphene electrodes in solution-processed transistors. *Nanoscale* **2013**, *5*, 11094–11101. [[CrossRef](#)] [[PubMed](#)]
13. Ho, K.I.; Huang, C.H.; Liao, J.H.; Zhang, W.; Li, L.J.; Lai, C.S.; Su, C.Y. Fluorinated Graphene as High Performance Dielectric Materials and the Applications for Graphene Nanoelectronics. *Sci. Rep.* **2014**, *4*, 5893. [[CrossRef](#)] [[PubMed](#)]
14. Choi, K.; Nam, S.; Lee, Y.; Lee, M.; Jang, J.; Kim, S.J.; Jeong, Y.J.; Kim, H.; Bae, S.; Yoo, J.B.; et al. Reduced Water Vapor Transmission Rate of Graphene Gas Barrier Films for Flexible Organic Field-Effect Transistors. *ACS Nano* **2015**, *9*, 5818–5824. [[CrossRef](#)] [[PubMed](#)]
15. Han, S.T.; Zhou, Y.; Wang, C.; He, L.; Zhang, W.; Roy, V.A.L. Layer-by-Layer-Assembled Reduced Graphene Oxide/Gold Nanoparticle Hybrid Double-Floating-Gate Structure for Low-Voltage Flexible Flash Memory. *Adv. Mater.* **2013**, *25*, 872–877. [[CrossRef](#)] [[PubMed](#)]
16. Nam, S.; Jeong, Y.J.; Park, C.E.; Jang, J. Enhanced gas barrier properties of graphene-TiO<sub>2</sub> nanocomposites on plastic substrates assisted by UV photoreduction of graphene oxide. *Org. Electron.* **2017**, *48*, 323–329. [[CrossRef](#)]
17. Kim, Y.; An, T.K.; Kim, J.; Hwang, J.; Park, S.; Nam, S.; Cha, H.; Park, W.J.; Baik, J.M.; Park, C.E. A composite of a graphene oxide derivative as a novel sensing layer in an organic field-effect transistor. *J. Mater. Chem. C* **2014**, *2*, 4539. [[CrossRef](#)]
18. Eda, G.; Nathan, A.; Wöbkenberg, P.; Colleaux, F.; Ghaffarzadeh, K.; Anthopoulos, T.D.; Chhowalla, M. Graphene oxide gate dielectric for graphene-based monolithic field effect transistors. *Appl. Phys. Lett.* **2013**, *102*, 133108. [[CrossRef](#)]
19. Kumar, K.S.; Pittala, S.; Sanyadanam, S.; Paik, P. A new single/few-layered graphene oxide with a high dielectric constant of 10<sup>6</sup>: Contribution of defects and functional groups. *RSC Adv.* **2015**, *5*, 14768. [[CrossRef](#)]
20. Fu, W.Y.; Liu, L.; Wang, W.L.; Wu, M.H.; Xu, Z.; Bai, X.D.; Wang, E.G. Carbon nanotube transistors with graphene oxide films as gate dielectrics. *Sci. China Phys. Mech. Astron.* **2010**, *53*, 828–833. [[CrossRef](#)]

21. Chua, L.L.; Zaumseil, J.; Chang, J.F.; Ou, E.C.-W.; Ho, P.K.-H.; Sirringhaus, H.; Friend, R.H. General observation of n-type field-effect behaviour in organic semiconductors. *Nature* **2005**, *434*, 194–199. [[CrossRef](#)] [[PubMed](#)]
22. Jang, J.; Nam, S.; Yun, W.M.; Yang, C.; Hwang, J.; An, T.K.; Chung, D.S.; Park, C.E. High  $T_g$  cyclic olefin copolymer/ $Al_2O_3$  bilayer gate dielectrics for flexible organic complementary circuits with low-voltage and air-stable operation. *J. Mater. Chem.* **2011**, *21*, 12542. [[CrossRef](#)]
23. Johra, F.T.; Lee, J.W.; Jung, W.G. Facile and safe graphene preparation on solution based platform. *J. Ind. Eng. Chem.* **2014**, *20*, 2883–2887. [[CrossRef](#)]
24. Nam, S.; Jeon, H.; Kim, S.H.; Jang, J.; Yang, C.; Park, C.E. An inkjet-printed passivation layer based on a photocrosslinkable polymer for long-term stable pentacene field-effect transistors. *Org. Electron.* **2009**, *10*, 67–72. [[CrossRef](#)]
25. Kim, S.H.; Jang, M.; Yang, H.; Park, C.E. Effect of pentacene–dielectric affinity on pentacene thin film growth morphology in organic field-effect transistors. *J. Mater. Chem.* **2010**, *20*, 5612–5620. [[CrossRef](#)]



© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).