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Delta-Sigma Modulator-Based Step-Up DC–DC Converter with Dynamic Output Voltage Scaling

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Abstract: The switching noise and conversion efficiency of step-up DC-DC converters need to be improved to meet increasing demand. The delta-sigma modulation (DSM) technique is typically used to improve the performance of buck converters; however, this control scheme is not directly applicable for boost converters. This paper presents a boost DC–DC converter using a continuous-time delta-sigma modulator (DSM) controller for battery-powered and noise-sensitive applications. The proposed converter can adjust a wide range of output voltages dynamically by clamping the maximum duty cycle of the DSM, thus enabling stable and robust transient responses of the converter. The switching harmonics in the converter output are reduced effectively by the noise shaping property of the modulator. Moreover, the converter does not suffer from instability of mode switching due to the use of a fixed third-order DSM. Fabricated in a 180 nm CMOS, the converter occupies an active area of 0.76 mm^2. It produced an output voltage ranging from 2.5 V to 5.0 V at an input voltage of 2.0 V and achieved a peak conversion efficiency of 95.5%. The output voltage ripples were maintained under 25 mV for all load conditions. A low noise output spectrum with a first spurious peak located −91 dBc from the signal was achieved.

Keywords: boost converter; maximum on-time duty cycle; delta-sigma modulator; switching noise; conversion efficiency

1. Introduction

Portable electronic devices are typically equipped with a rechargeable lithium-ion battery with an output voltage range from 4.2 V to 2.7 V [1]. However, traditional analog mixed-signal systems may require the supply voltage to be regulated at a higher level than the battery voltage [2,3]. Therefore, integrated boost DC–DC converters, which can serve as a power interface to step up the input voltage, have become increasingly popular [4–10]. These converters must exhibit a high conversion efficiency to extend the battery life and minimize the chip area to be cost effective. Moreover, low noise characteristics should accompany this in order to achieve high performance in precision analog blocks.

In recent years, an approach to reduce the switching noise in DC–DC converters using a delta-sigma modulator (DSM) controller has received increasing attention [11,12]. Replacing the conventional pulse-width modulation (PWM) controller with a DSM can reduce the output harmonics and electromagnetic interference and yield high efficiency. This control scheme is directly applicable for boosting converters [6,13,14]; however, the most practical limitation on the step-up conversion is that the maximum duty ratio (D_{MAX}) of the DSM controller cannot be adjusted as in conventional PWM controllers [15]. Because the digitalized output bitstream of the DSM is determined by the difference between the reference voltage of the compensator (V_{REF}) and output voltage of the converter (V_{OUT}), a duty condition exceeding D_{MAX} may occur under dynamic output voltage scaling where V_{REF} is significantly higher than V_{OUT}. Beyond D_{MAX}, the output voltage can decrease below the targeted

value, and the feedback loop may become unstable [16]. In an extreme scenario, a 100% duty condition with the low-side N-type transistor turned on can be produced, in which case the stored energy of the inductor is not transferred to the load and causes an excessive inductor current, resulting in damage to the bottom switch. An earlier study did not address this issue because the output voltage scaling condition was not considered [6]. Therefore, it is necessary to produce a duty ratio limitation in the DSM controller to ensure the reliable operation of the boost converter.

This paper presents a low-switching-noise boost converter that uses a DSM controller with limited on-time duty ratio. The proposed converter produces a wide range of scalable output voltages by adjusting the maximum duty cycle of the controller, thus enabling robust and reliable operation of the converter. Moreover, the boost converter achieves a low output switching noise by using a noise-shaped third-order DSM controller. The remainder of this paper is organized as follows. Section 2 introduces the proposed boost converter architecture; Section 3 describes the detailed circuit of the duty cycle limiter, DSM controller, and compensator; Section 4 provides the experimental results of the prototype converter; and Section 5 presents the conclusions.

2. Proposed DSM-Based Boost Converter Architecture

The block diagram of the proposed boost converter is shown in Figure 1. The converter is composed of power stages (two switches of M_N and M_P, an external inductor L, and an output capacitor C), feedback networks (a resistor divider comprising R_1 and R_2 and a compensator), and control blocks (a third-order DSM, a duty controller, and a dead-time controller). The external inductor and capacitor are 2.8 µH and 20 µF, respectively. The signal difference between the scaled output voltage V_{FB} and reference voltage V_{REF} is processed by the compensator and fed to the DSM input. The switching noise of the converter can be reduced by the noise shaping capability of the DSM. The DSM outputs noise-shaped, digitized single-bit, and multiple delayed signals of V_{D1} to V_{D5} to control the on-time duty ratio. The duty controller produces a modified output bitstream V_M with this limited on-time duty ratio. V_M drives the power stage through a deadtime controller. The clock signal f_S is applied externally with a 12 MHz source. The converter has a single operating mode because it operates only in the continuous conduction mode (CCM) condition under the targeted output load of 50–450 mA. A zero-current detector (ZCD) was included for stable operation under light load conditions below 50 mA. A bandgap reference (BGR), soft start, and supply selector were also designed for a more robust operation.

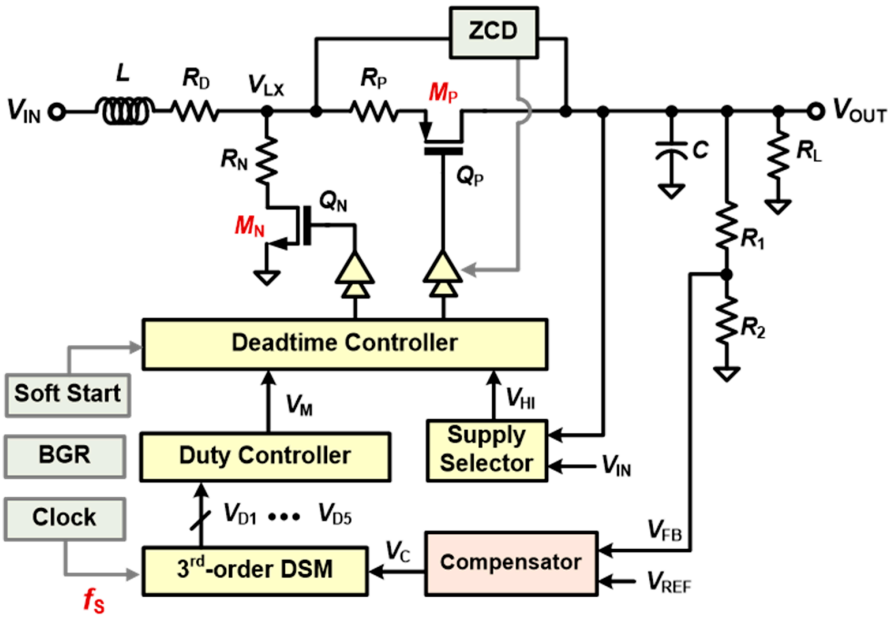

Figure 1. Block diagram of the proposed step-up converter.

3. Circuit Implementations

The proposed boost converter was designed for a supply of 2.0–4.5 V, output voltage of 2.5–5.0 V, and output current of 1–450 mA. It uses a switching frequency of 12 MHz.

3.1. Duty Cycle Controller

The voltage conversion ratio M for an ideal boost converter (in Figure 1, R_D, R_N, and R_P are 0 where R_D is the parasitic resistance of inductor L, R_N is the on-resistance of low-side transistor M_N, and R_P is the on-resistance of high-side transistor M_P) is determined by 1/(1–D), which is a function of duty cycle D [16]. A larger output voltage can be achieved as D approaches 1. In the practical case where the resistances of the inductor and switches are present (in Figure 1, R_D, R_N, and R_P are not 0), M can be calculated as [17]

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{R_L \cdot (1 - D)}{R_L \cdot D^2 - (2R_L + R_P - R_N)D + R_L + R_P + R_D} \quad (1)$$

The reduction in M is demonstrated for various on-resistances of transistors in Figure 2. As shown in Figure 2, the parasitic resistance and on-resistances in Equation (1) limit the maximum M and determine the upper limit of D (D_{MAX}) that can produce normal operation with a positive gain. It is noteworthy that although M is not a function of V_{IN}, R_N and R_P are proportional to V_{IN}; therefore, the maximum output voltage can vary with V_{IN}. In the targeted system, the worst-case D_{MAX} at which M begins to decrease is about 0.8, which occurs at the maximum load current and highest R_N condition. The duty cycle of the DSM controller should be clamped to a fixed D_{MAX} to prevent control loop instability.

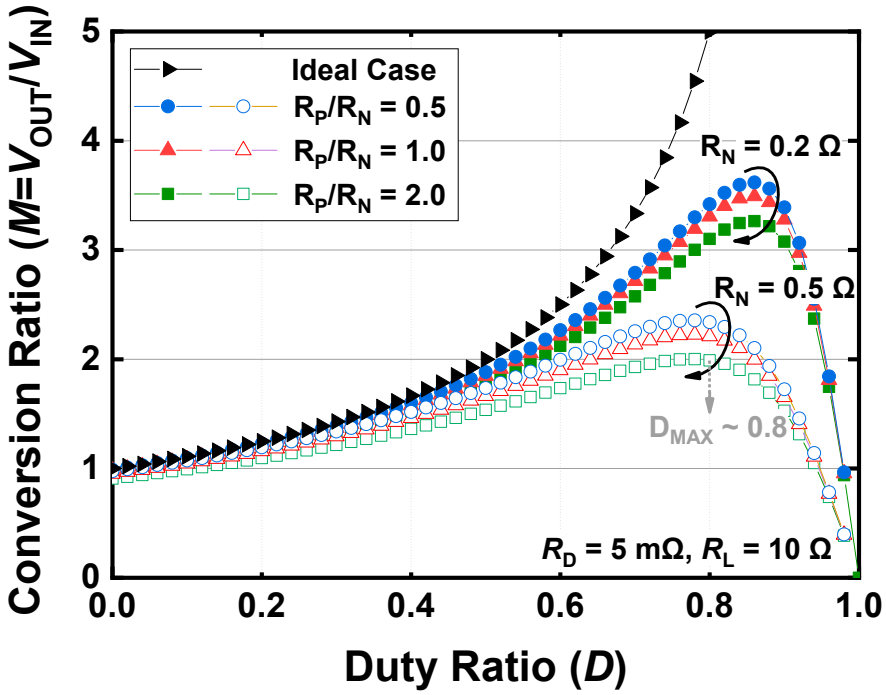

Figure 2. Voltage conversion ratio with respect to the duty ratio.

The proposed duty cycle limiter (DCL) is shown in Figure 3. Multiple delayed signals (V_{D1} to V_{D5}) connected to the DSM output (DSMO) and a modified counter with an AND gate are used to clamp the duty cycle of the controller. By connecting the inverting output of the D-type flip-flop (DFF) back to the "D" input through the AND gate and creating a feedback loop, the signal period applied to V_{SUM} can be counted using the clock signal f_S. V_{SUM} outputs high only when V_{D1} to V_{D5} produce low

simultaneously. Therefore, if the DSM outputs a low signal for five or more periods, V_{SUM} activates the DFF to form a new pulse V_{SHOT}. This signal is combined with the original DSM output V_{D1} and limits the on-time duty of the proposed boost converter. Figure 4 shows the simulation results of the proposed duty cycle control. V_{SHOT} is generated when the output of the DSM maintains low for more than five cycles, as explained earlier. The modified control signal of the controller V_M effectively limits the D_{MAX} of the converter by adding new pulses through V_{SHOT}. The clamped D_{MAX} is approximately 83%, which corresponds to the system simulation results.

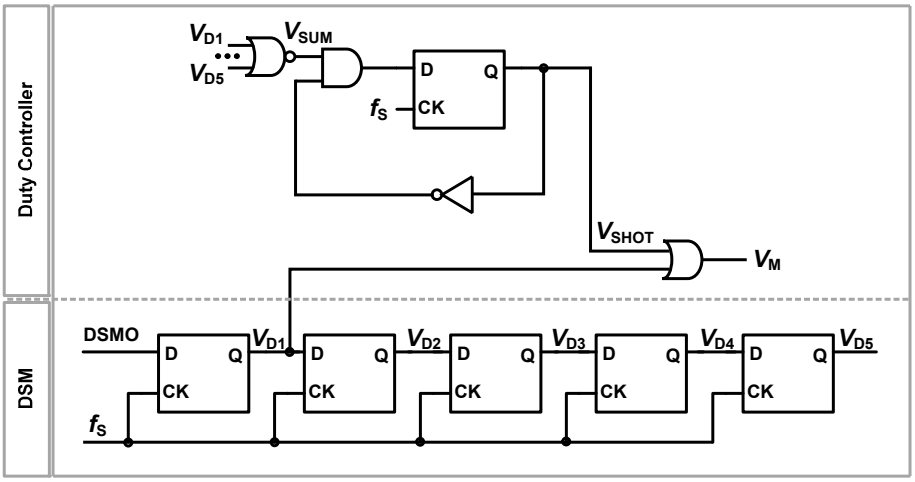

Figure 3. Proposed duty cycle limiter.

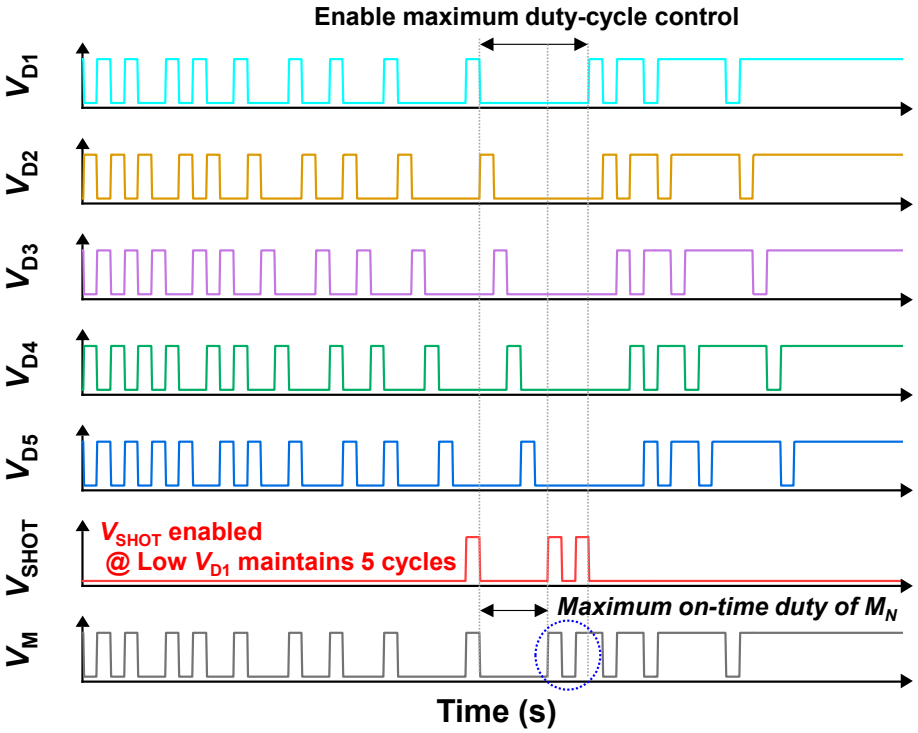

Figure 4. Simulation results of the proposed duty cycle control.

The simulation result of the dynamic output voltage scaling according to the DCL scheme is shown in Figure 5. Without the DCL, because a V_{SHOT} signal is not produced and a 100% duty condition in which M_N is solely turned on has occurred, the stored energy of the inductor causes an excessive current; hence, the output voltage decreases below the targeted value and the feedback loop

becomes unstable. Meanwhile, with the DCL, D_{MAX} is limited by V_{SHOT}, resulting in stable operation of the converter. The stability of the control loop is maintained despite the forced V_M because the compensator and DSM can sufficiently cope with the variation in the output voltage from the changed switching operation. Therefore, the proposed step-up converter enables a wide range of scalable output voltages with stable transient responses, as shown in Figure 5. Moreover, because the proposed technique controls the duty cycle in the digital domain rather than in the analog domain, it is more immune to process and temperature variations [17].

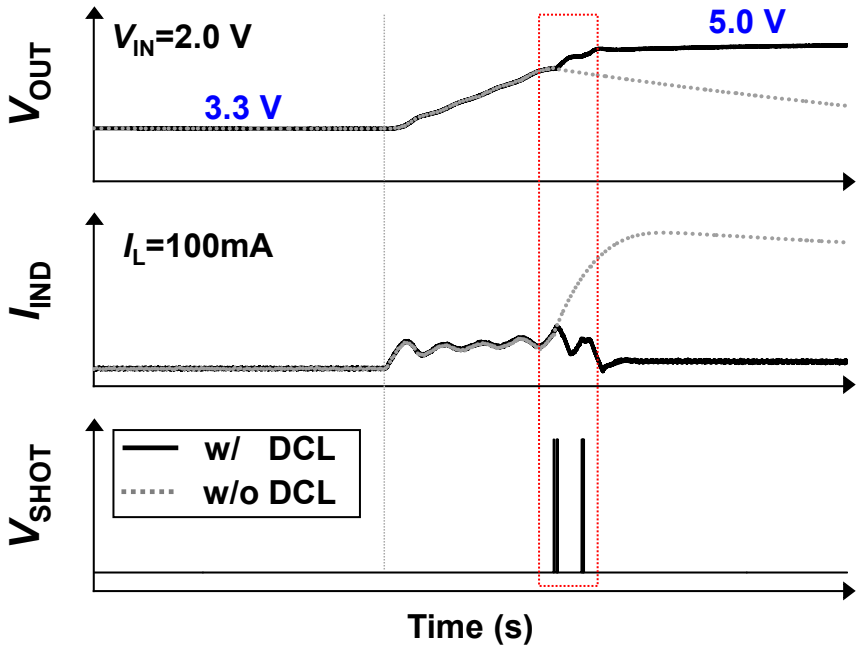

Figure 5. Dynamic output voltage scaling according to the duty cycle limiter (DCL) scheme.

3.2. Third-Order Single Op-Amp DSM

The DSM controller in Figure 6 adopts a continuous-time (CT) architecture with a third-order single op-amp loop filter because of its simple and nondelaying nature. A CT DSM is less sensitive to loop filter delays compared with discrete-time DSMs, and the single op-amp loop filter merges multiple integrators into a single op-amp; hence, the proposed controller exhibits the advantages of high-order and -frequency operations with improved power and area efficiency. The proposed third-order loop filter (LF) consists of a single op-amp with an input resistor (R_1), three series-connected capacitors (C_1, C_2, C_3), and two T-shape resistors ($R_2||R_4||R_6$, $R_3||R_5||R_7$). The input signal and the output signal are applied to R_6 and R_5, respectively, through the cross-coupled connection of the differential signal, which is illustrated as -1. These signals adjust the numerator and denominator coefficients of the transfer function. The transfer function of proposed LF is given by

$$G_D(s) = \frac{V_O}{V_I} = \frac{s^2 \cdot \frac{1}{C}\left(\frac{4}{R_1} + \frac{1}{R_7} - \frac{3}{R_6}\right) + s \cdot \frac{1}{C^2}\left[\frac{3}{R_1}\left(\frac{1}{R_X} + \frac{1}{R_Y}\right) - \frac{2}{R_6 R_Y}\right] + \frac{2}{C^3 R_1}\left(\frac{1}{R_X} \cdot \frac{1}{R_Y}\right)}{s \cdot \left[s^2 + \frac{2/3}{C^2 R_5 R_Y}\right]} \quad (2)$$

where $R_X = R_2||R_4||R_6$, $R_Y = R_3||R_5||R_7$, and $C = C_1 = 2 \cdot C_2 = C_3$. The positive feedback produced by R_5 makes a resonating condition when $R_4 = 3 \cdot R_5$. The resonating condition is used to implement a zero-optimized noise transfer function (NTF). The DSM can maximize the signal-to-noise ratio by optimizing the NTF zeros. The simulation results of the signal transfer function and NTF of the DSM are illustrated in Figure 7 using a Matlab/Simulink simulation platform. This noise shaping characteristic of the DSM controller can effectively suppress the switching noise of the boost converter.

The corresponding sampling frequency (f_S) and signal bandwidth (f_{BW}) are 12 MHz and 150 kHz, respectively. The performance of the DSM was described in greater detail in [18]. The primary difference of the DSM compared with [11] is that it adopts only the third-order loop filter structure. This is because the proposed converter has a small output load range and operates only in the CCM. Thus, the converter does not suffer from instability of the mode switching and alleviates the design complexity of the compensator. Moreover, the third-order structure exhibits a signal-to-noise ratio more than 20 dB higher when compared with its second-order counterpart [19], which can improve the switching noise rejection.

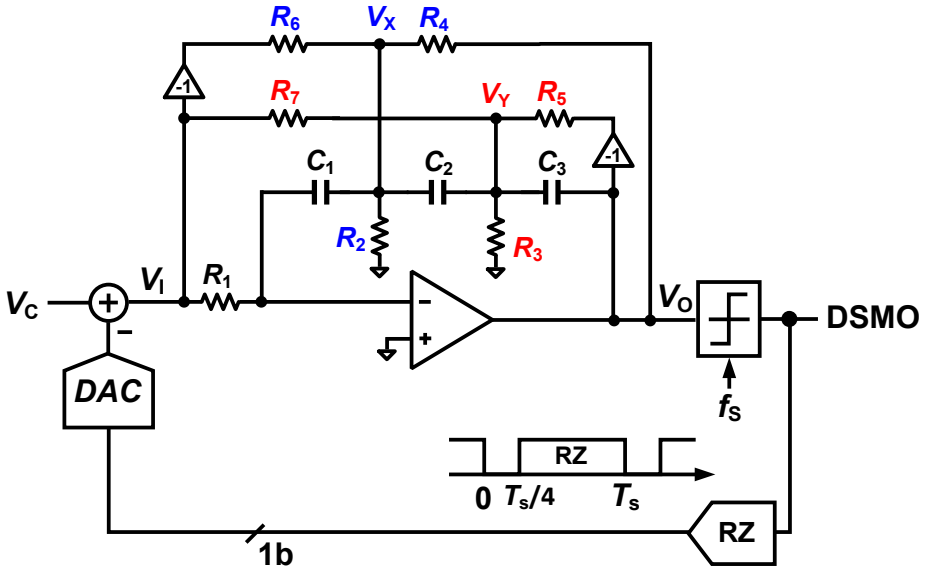

Figure 6. Single op-amp third-order DSM.

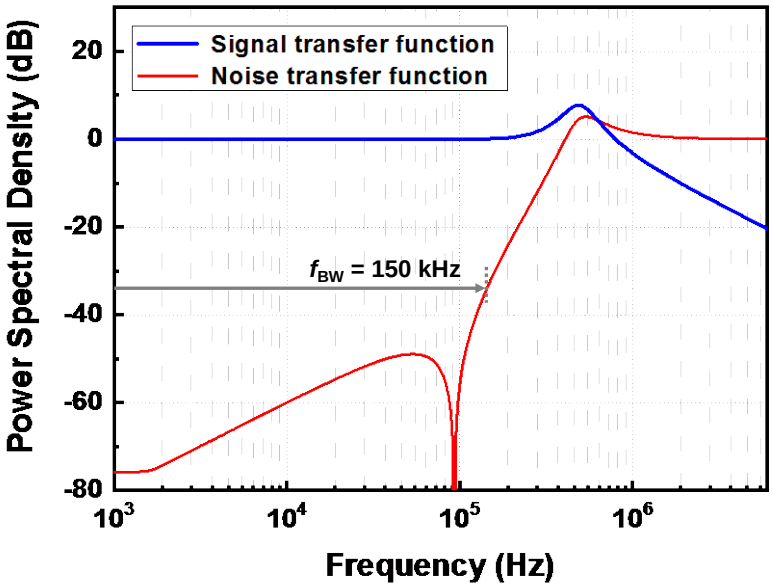

Figure 7. Signal and noise transfer functions of the single op-amp loop filter.

3.3. Type-III Controller

Because the right-half-plane zero (RHPZ) shifts to a lower frequency as the load current increases, a type-III compensator was adopted to overcome the reduced phase margin due to the RHPZ, as shown in Figure 8. An error amplifier with a feedback network (C_1, C_3, and R_2) is the on-chip component and

an input network (C_2, R_1, and R_3) is the off-chip component. The transfer function of the compensator is expressed as

$$G_C(s) = \frac{(sC_1R_2 + 1)(sC_2(R_1 + R_3) + 1)}{s \cdot (sC_1C_3R_2 + (C_1 + C_3))(sC_2R_1R_3 + R_1)} \quad (3)$$

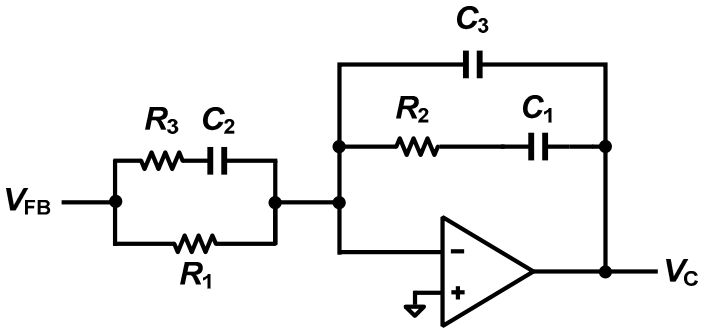

Figure 8. Type-III compensator.

The compensator produces three poles and two zeros to improve the system stability by compensating the phase delay caused by the external L and C, equivalent series resistance zero, and RHPZ.

4. Measurement Results

The proposed boost converter was implemented in a 180 nm complementary metal–oxide–semiconductor process. Figure 9 shows the chip micrograph. The converter occupies an active area of 0.76 mm^2, which is one of the smallest among the reported step-up converters [5–8,13].

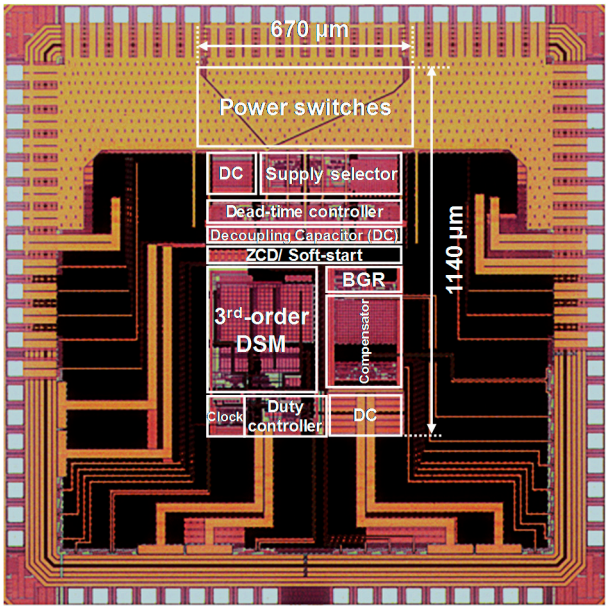

Figure 9. Chip micrograph.

The proposed step-up converter can adjust the output voltage dynamically by changing the reference voltage, as shown in Figure 10. For a V_{IN} of 2.0 V and I_L of 125 mA, V_{OUT} changes from 2.5 to 5.0 V. A wide-range scalable output voltage was produced by virtue of the maximum duty cycle limiter, which enables stable and robust operation of the converter.

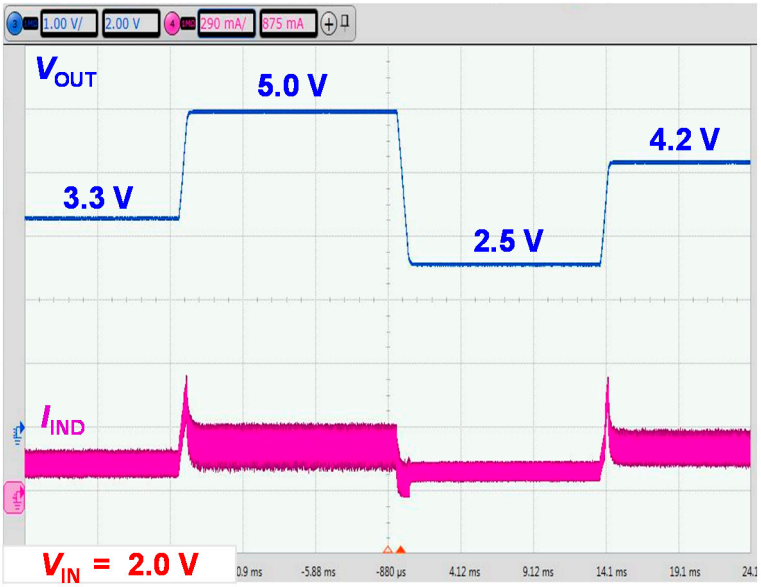

Figure 10. Measured dynamic output voltage scaling.

Figure 11 shows the measured output spectrum of the proposed DSM-based step-up converter. The spurious tones were suppressed effectively, as predicted. A first spurious peak located at −91 dBc below the DC signal was achieved. Although the rejection of the switching noise was not as good as that for the buck converter [11], the proposed converter demonstrated significantly reduced switching harmonics compared with a conventional PWM-based boost converter [8] and DSM-based boost converters [6,13].

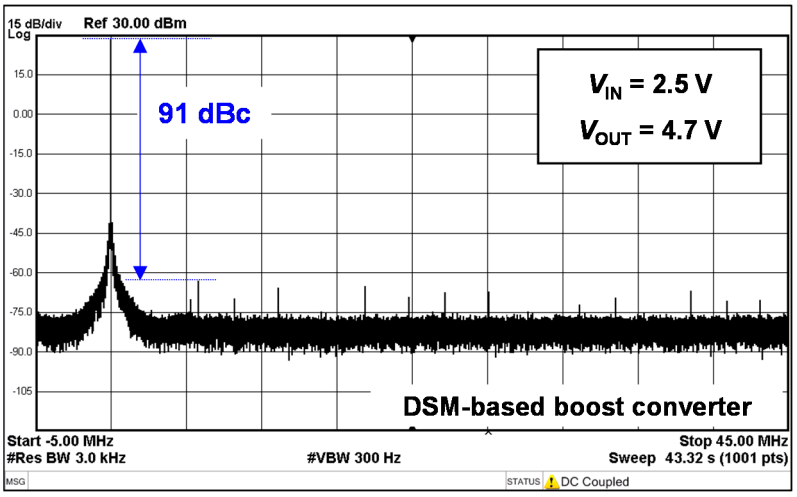

Figure 11. Measured output voltage spectrum.

Figure 12 shows the transient waveforms with respect to the load current at V_{IN} = 3.7 V and V_{OUT} = 5.0 V. When I_L = 1 mA, the reverse inductor current is controlled effectively by the ZCD. As the load current increases, the output voltage ripple worsens; however, it is controlled within 25 mV at a 450 mA load. Moreover, the body diode did not conduct, owing to the deadtime controller in the CCM operation where the ZCD was not enabled (Figure 12b,c).

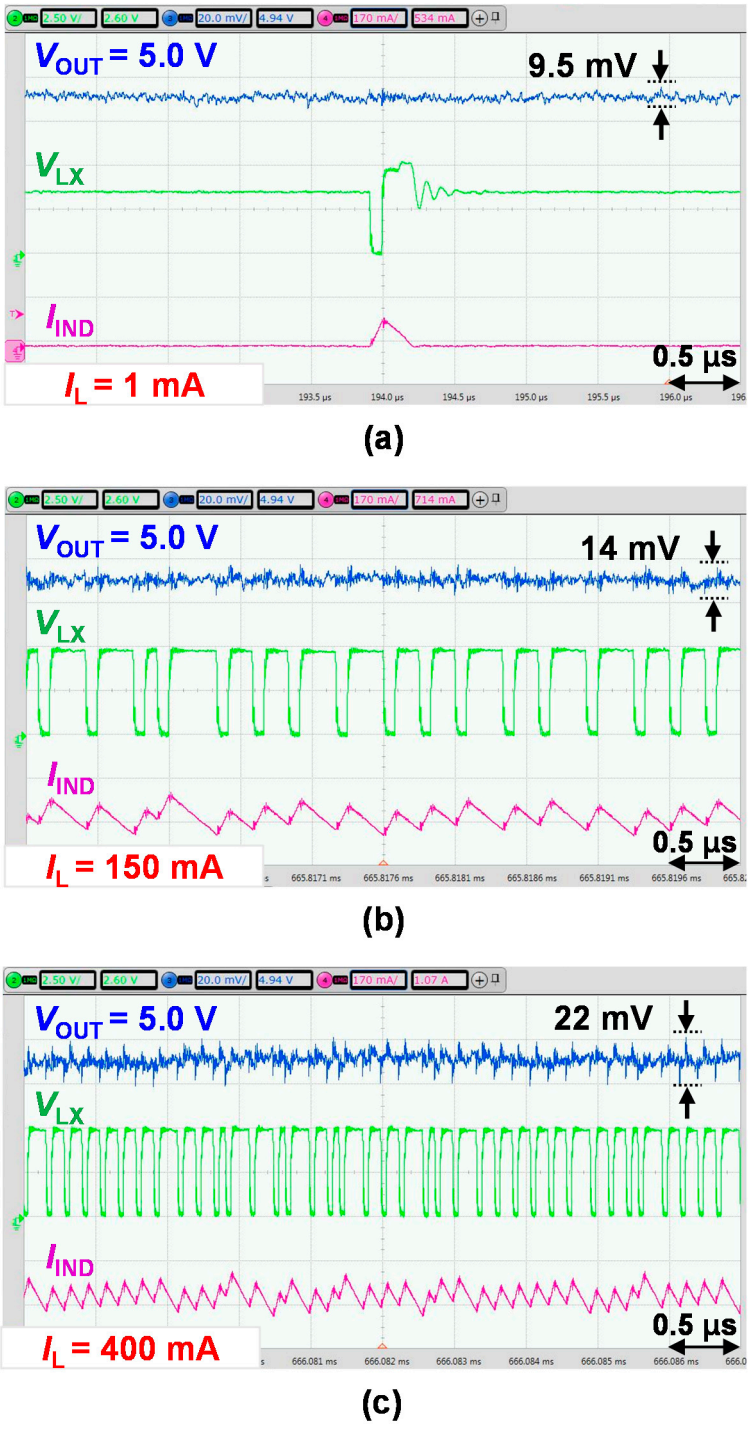

Figure 12. Measured transient waveforms with respect to the load current at V_{IN} =3.7 V. (**a**) I_L = 1 mA. (**b**) I_L = 150 mA. (**c**) I_L = 400 mA.

Figure 13 shows the load transient response with V_{IN} = 3.7 V when I_L changes between 10 and 350 mA. The transient recovery times and undershoot voltages were less than 60 µs and 92 mV, respectively. These measurements indicate that the proposed step-up converter produces a good transient response with robust stability.

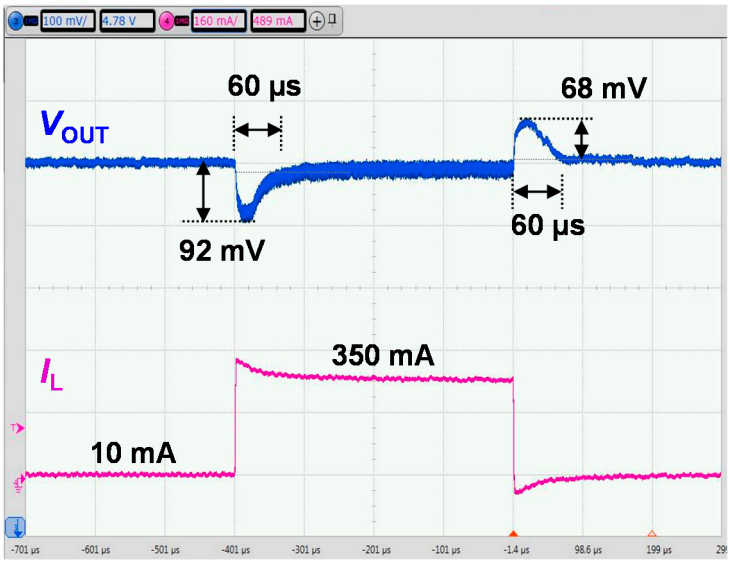

Figure 13. Load transient response.

Figure 14 shows the measured efficiency with different input voltages at V_{OUT} = 5 V. The converter exhibited a peak efficiency of 95.5% when V_{IN} = 4.5 V and I_L = 150 mA. For the targeted load current range from 50 to 450 mA, the converter efficiency was maintained over 80% regardless of the input voltage. Table 1 summarizes the performance of the boost converter and compares it with that of the state-of-the-art boost converters.

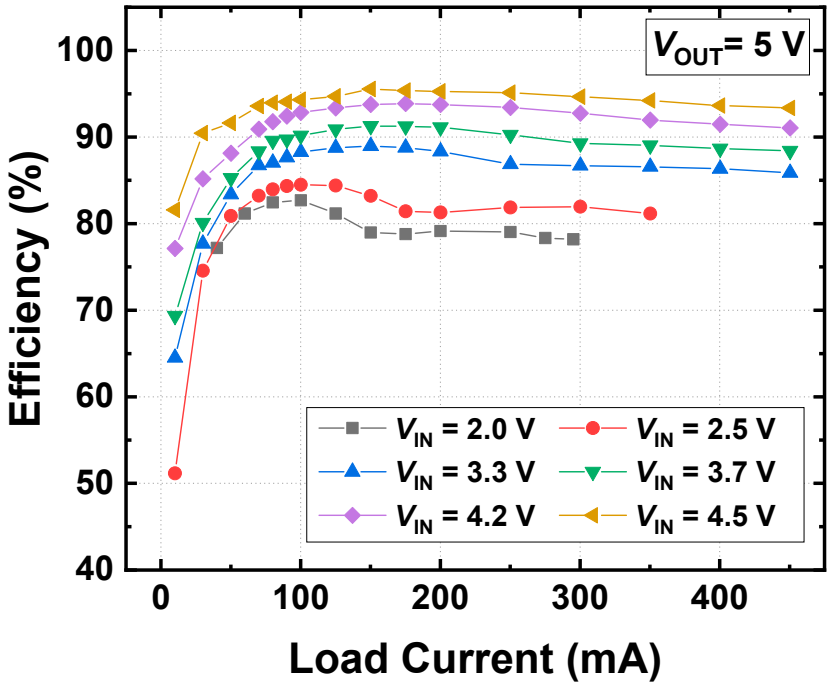

Figure 14. Measured efficiency of the boost converter.

Table 1. Performance summary of the proposed converter and comparison with state-of-the-art boost converters.

ref.	V_{IN} (V)	V_{OUT} (V)	Controller		L (µH)	C (µF)	Load Current (mA)		Efficiency	Max Ripple V_{OUT} (mV)	Output SFDR (dBc)	Size (mm^2)	Process (nm)
			Type	f_S (MHz)			min	max	Peak η (%)				
This work	2.0–4.5	2.5–5.0	DSM	12	2.8	20	1	450	95.5	25 @500 mA	91	0.76	180
[5]	0.8–1.4	1.8	MRAOT	1	1	6.8	10	400	92.4	42.5 @400 mA	-	0.88	180
[6]	0.8–1.2	1.8	DSM	1–2	3.3	10	1	100	90	45 @100 mA	70	0.85	180
[7]	2.5–4.2	5	Current-Mode Synthetic	2–5	1	10	10	500	90	50 @400 mA	-	1.90	300
[8]	1.8–3.2	3.0–4.2	Adaptive On Time	$1/2^N$ N = 0–5	1	10	2	800	94.8	80 @800 mA	~50 *	2.25	350

* extracted from graph.

5. Conclusions

A low-switching-noise boost DC–DC converter with improved transient responses was presented. The proposed converter produced a wide range of dynamic output voltages from 2.5 to 5.0 V at V_{IN} = 2.0 V and achieved a conversion efficiency of higher than 80% over the input voltage and load current ranges of 2.5–4.5 V and 50–450 mA, respectively. Its output voltage ripples were maintained below 25 mV. Moreover, the switching harmonics were reduced by the noise-shaped DSM controller. The proposed converter's active area of 0.76 mm^2 is highly competitive among the previously reported step-up converters. Therefore, it is expected to be a desirable solution for battery-powered and noise-sensitive applications.

Author Contributions: Y.-K.C., S.-B.H. and B.H.P. conceived the idea and co-wrote/edited the manuscript. Y.-K.C. suggested the initial idea of a delta-sigma modulator-based step-up converter. Y.-K.C. designed the circuits. Y.-K.C. and S.-B.H. measured the electric characteristics of the fabricated boost converter. Y.-K.C., S.-B.H. and B.H.P. analyzed the experimental data. All authors discussed the results and commented on the manuscript. B.H.P. was in charge of project administration. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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