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In situ implementation of silicon epitaxial layer on amorphous SiO_2 using reduced-pressure chemical vapor deposition

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ABSTRACT

With the increasing power demand of system-on-chip structures, an ultrathin body is increasingly important owing to its low power leakage; silicon-on-insulator (SOI) technology is used to fabricate such ultrathin platforms. However, the contemporary SOI process and the wafer itself are complex and expensive. In this study, we developed an easy SOI fabrication process that can be implemented on any desired local area of a bulk silicon wafer using the commercially implemented reduced-pressure chemical vapor deposition technique. A local SOI was fabricated through the selective epitaxial growth of silicon, which can also be grown laterally on top of amorphous SiO_2 patterned with a 1 μm-wide silicon seed zone and an etch stopper with dimensions of 20 $\times$ 100 μm. The local SOI, processed to a thickness of 100 nm or less by chemical mechanical polishing, exhibited a highly crystalline state, as confirmed by cross-sectional imaging and diffraction pattern analysis, surface roughness analysis, and wide-range epitaxy analysis. The local SOI exhibited a surface roughness of 0.237 nm and maintained a perfect (100) crystal plane, identical to that of the silicon wafer, under optimized process conditions. We successfully fabricated reconfigurable transistors on the present local SOI, which implies that contemporary silicon electronics can take advantage of SOI devices on its own platform.

1. Introduction

The manufacturing of high-performance semiconductor devices and their integrated circuits became possible owing to the application of advanced growth engineering like heteroepitaxy process [1–15]. III-V compound semiconductors and silicon have been extensively studied using novel processes like molecular beam epitaxy (MBE) and ultra-high vacuum chemical vapor deposition (UHVCVD) [16–25]. Some of the most successful heterostructure-related technologies have reached the commercialization stage, although significant issues, such as strain-limited critical height, are still encountered in the fabrication process. Even multiple heteroepitaxial layers can be grown, although special care must be taken in the case of the existence of large lattice mismatch between growing layer and substrate. If semiconductor can be epitaxially grown on dielectric materials, in particular, a lot of innovative opportunities will arise in semiconductor industries by fabricating devices and even circuits there.

Nonetheless it has not been reported yet that the growth of epitaxial silicon succeeds over a wide area of amorphous dielectric SiO_2 because imperfect lattice and crystalline defects on the surface of the amorphous substrate interfere with the epitaxial growth making the growing silicon amorphous or at most polycrystalline phase. Although some of successful epitaxial growth on SiO_2 have been reported according to References [2,4,8,26–28], the epitaxial area is not large enough to afford unit devices like FET (field effect transistor), a building block of contemporary semiconductor technology. Furthermore, most of the efforts are focused on epitaxial growth right atop of crystalline seed zone or over a short lateral range. Thereby semiconductor industries can't fully take advantage of this kind of technology that enables power-efficient devices, programmable device like reconfigurable FET, and/or their integrated circuits to be monolithically integrated. If local SOI (silicon-on-insulator) is implemented on a bulk silicon wafer, combined electronics of CMOS (complementary metal oxide semi-

Abbreviations: SOI, silicon-on-insulator; MBE, molecular beam epitaxy; CVD, chemical vapor deposition; ELO, epitaxial lateral overgrowth; CMP, chemical mechanical polishing; RPCVD, reduced-pressure chemical vapor deposition; IC, integrated circuit; EBSD, electron backscatter diffraction; SEM, scanning electron microscopy; TEM, transmission electron microscopy; AFM, atomic force microscopy; BOX, buried oxide; FIB, focused ion beam; RMS, root mean square.

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conductor) and SOI architecture could be realized in single chip eventually.

Recently, with the application of artificial intelligence technologies to various scientific fields, a demand for computer chips with more than hundreds of millions of transistors operating at low power level has emerged owing to tremendous volume of data generated and the high speed of the cutting-edge processors [29–34]. Accordingly, diverse approaches to materials and device processes are employed to ease the power burden by adopting the expensive SOI wafer. As one of the approaches we tried to develop the local SOI technology and successfully achieved it. In this paper, we report not only experimental results on growth process using conventional CVD but also analysis results on limiting factors that prevent growing silicon from keeping epitaxy over a large area more than hundreds of square micrometers. Particularly, we scrutinized the interface between the growing silicon and SiO_2 substrate in terms of electron microscopy and diffraction analysis. Finally, we proved our work is meaningful from the device point of view by showing the good electrical properties of reconfigurable FET that is fabricated on the lateral overgrown silicon epilayer.

2. Materials and methods

A silicon epilayer was grown on an amorphous solid by initially forming a 200 nm or 400 nm-thick silicon thermal oxide layer on a 6" *p*-type (100) silicon wafer. Subsequently, the active region became the local SOI, and a silicon seed zone, exposing the silicon substrate for a selective epitaxial growth, was formed near the active region through a two-step dry etching process followed by a final wet etching process. The edge of the active region had a stepped structure, which acted as an etch stopper that determined the thickness of the local SOI layer. The epitaxial lateral overgrowth (ELO) of silicon, which started to grow in the silicon seed zone, covered all the active regions of oxide in the lateral direction and formed a thin silicon epitaxial film. The silicon epilayers could be selectively grown on the silicon seed zones through the reduced-pressure chemical vapor deposition (RPCVD) technique (ASM Epsilon One model) under specific growth conditions using a gas mixture of $SiH_2Cl_2/HCl/H_2$ at 1000 °C and 40 Torr. These silicon epilayers could not be grown on any other field oxide layer.

Silicon seed surfaces, exposed within the SiO_2 layer, were wet cleaned before loaded into a quartz chamber and *in situ* H_2-baked at 1000 °C for 90 s to remove the residual native oxide. After growing the selective silicon epilayer using RPCVD, the samples were precisely planarized via CMP (G&P Technology, POLI-500 model); the polishing pressure, whereby the wafer was pushed against a polishing pad, was 200 g/cm^2. We investigated the mechanical stability of the grown epilayer after CMP, which is necessary for the fabrication of integrated circuits (ICs). We also investigated the crystalline quality of the silicon epilayer grown on the amorphous SiO_2 at three phase levels, namely the grain, subgrain, and lattice scales, through image analysis techniques, such as electron backscatter diffraction (EBSD), scanning electron microscopy (SEM), and transmission electron microscopy (TEM), respectively. Using the electron diffraction patterns, we investigated the crystalline defects induced during the crystalline silicon growth in the lateral direction on SiO_2. The surface morphology after CMP was analyzed using atomic force microscopy (AFM).

3. Results and discussion

The epilayer on SiO_2 can be used as a co-platform in an IC chip when the area of the grown layer is large enough to embed devices, such as logic gates. We optimized the process conditions so that a wide silicon epilayer can be grown while maintaining the optimal crystallinity. The selectivity between the silicon seed layer and the SiO_2 layer was strongly influenced by the process temperature, pressure, growth rate, and, in particular, the additional HCl gas used to etch the silicon clusters formed on the SiO_2 layer. The selective epitaxial growth of silicon was possible only under a specific ratio of SiH_2Cl_2 (the source gas used for the silicon growth) to HCl gases that were injected to increase the selectivity. Under the optimized growth conditions of the present epilayer, representative samples are summarized with respect to key parameters in detail in Table 1. We compared three important parameters from the point of view; (a) substrate configuration with the thickness of BOX and local SOI, (b) growth conditions with gas flow rate, and (c) preferred growth direction with growth rate that implies the degree of resistance for lateral growth. Although the difference of growth conditions of each sample seems to be small, epitaxial growth is so sensitive process that small difference makes big difference in crystallinity of grown layer and device performance fabricated on it. In addition, the thicknesses of both the BOX and local SOI layers of each sample were determined by the depth of the active area patterned by the etching of the initially formed SiO_2 layer. For instance, if the active region is etched to a depth of 200 nm on a 300 nm-thick SiO_2 film, the BOX and local SOI layer thicknesses will be 100 nm and 200 nm, respectively.

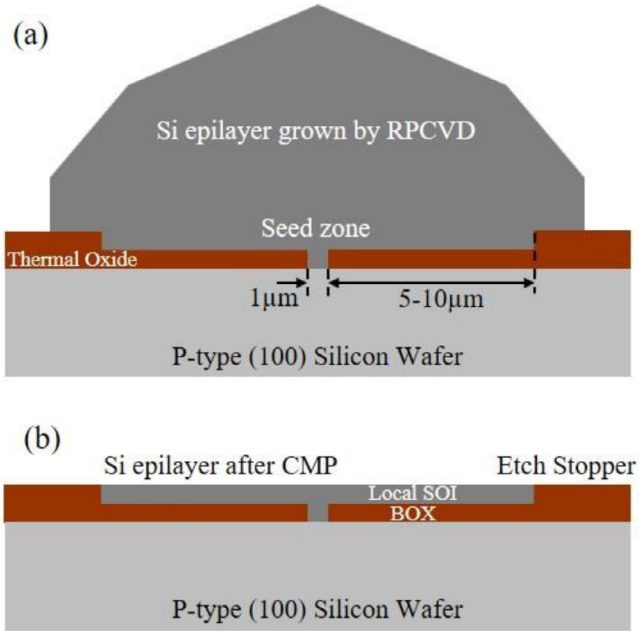

Fig. 1. Schematic cross-sections of (a) as-grown silicon epilayer starting from the seed zone along the thin thermal oxide region and eventually over the thick thermal oxide layer, and (b) the grown layer after undergoing the CMP process, in which the thick thermal oxide layer acts as the etch stopper.

Fig. 1 shows the schematic cross-section of the silicon epitaxial layer grown on SiO_2 as proposed in this study. In this work, the silicon seed zone (1.0 × 100 μm) for the silicon ELO was opened at the center of the active region by a two-step etching process, and the width from the silicon seed tip to the end of the active region was 5 μm or 10 μm in both directions. The silicon seed zone, which was the starting point for the selective growth of silicon, was initially formed by dry etching before being wet etched to prevent surface damage. While silicon grows vertically filling the inside of the seed zone, it begins to grow in all directions immediately after it comes out of the hole, growing over first the thin and subsequently the thick SiO_2 regions (Fig. 1(a)). From the silicon seed zone, the silicon layer is selectively and epitaxially grown over the SiO_2 layer up to 20 μm, while maintaining the lateral

Table 1
Properties of the samples fabricated under optimized growth conditions for the present silicon epilayer, while maintaining the selectivity and rapid growth rates, including the thickness of the buried oxide (BOX)/local SOI layer, SiH_2Cl_2/HCl gas ratio, and growth rates in the vertical and lateral directions.

ID	BOX (Thin SiO_2) [nm]	Local SOI (Si after CMP) [nm]	Gas flow rate (SiH_2Cl_2/HCl) [sccm]	Directional growth rate [nm/min]		
				Lateral (L)	Vertical (V)	L/V
Sample #1	200	200	20/100	130.2	140.8	0.925
Sample #2	200	200	10/100	54.5	67.6	0.806
Sample #3	100	100	10/100	57.7	68.8	0.839

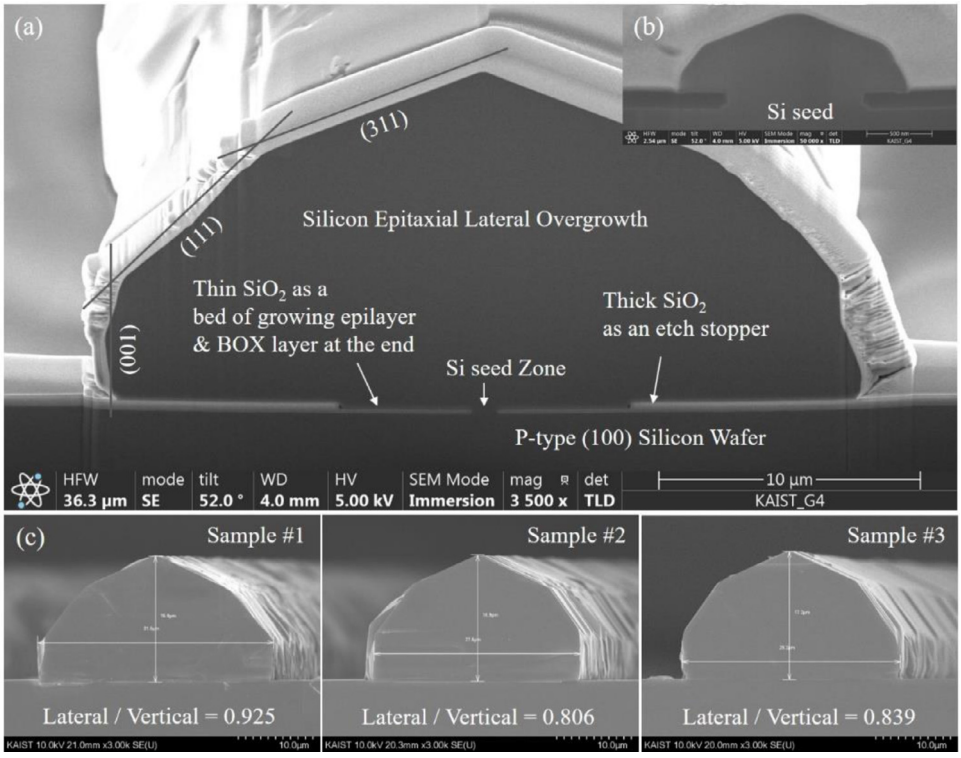

Fig. 2. Cross-sectional images of the silicon ELO layer in Sample #1: (a) 52°-tilted FIB-SEM image showing the (001), (111), and (311) planes of the dominant growth directions, (b) early stage of the silicon epilayer growth, (c) variation in the cross-sectional shape according to the growth rate ratio in the vertical and lateral directions, more specifically, the growth rate of the crystalline planes based on the growth conditions. Notably, a sufficiently wide epilayer can be grown on amorphous SiO_2 using the present RPCVD process.

growth. The grown silicon epitaxial layer was planarized to a thickness of 200 nm or less using CMP. With the silicon epilayer on SiO_2 as a co-platform on the IC chip, silicon devices can be fabricated in the thin SiO_2 region, whereas the thick SiO_2 layer plays the role of an etch stopper during the CMP process (Fig. 1(b)).

Under the optimized growth conditions and the SiH_2Cl_2/HCl/H_2 mixture described above, we achieved fully selective epitaxial growth of a single silicon crystal in the SiO_2 pattern, even when the silicon ELO lateral growth exceeded 20 μm. Fig. 2(a) shows a 52°-tilted focused ion beam (FIB)-assisted SEM cross-sectional image of the silicon grown approximately 15 μm laterally on the thin SiO_2 layer in Sample #1. The silicon layer started to grow in the 1 μm wide silicon seed region and grew in all directions on the thin SiO_2 layer. Three representative facets were observed: (311), (111), and (001), which can also be observed in the initial stage of the silicon ELO groth (Fig. 2(b)), indicating that the stable growth of the (311), (111), and (001) planes was maintained throughout the growth. In addition, the same dominant facet group can be observed in each sample even under different growth conditions (Fig. 2(c)). However, each facet seen in the SEM image shows a shape that is not sufficiently straight. This seems to be due to the stress induced when the silicon begins to grow laterally as the silicon ELO passes through the silicon seed zone or etch stopper step, or due to defects introduced when the single-crystal silicon bonds with the thin SiO_2. This is discussed in more detail later in the TEM and EBSD analyses for comparing the crystallinity of each sample. Moreover, this phenomenon occurs in the ELO because of the deviations in the fabrication processes, such as photolithography, adhesion between the photoresist and SiO_2 layer, and etching [35].

A remarkable feature of the silicon ELO in this experiment is that the ratio of silicon growth in the lateral direction to that in the vertical direction depends on the ratio of the SiH_2Cl_2/HCl gas injected during the growth in the RPCVD process and the heights of both the BOX and the etch stopper. The growth rate in each direction was measured as the height of the silicon ELO in the vertical direction from the top of the silicon seed zone and the distance grown laterally from the edge of the silicon seed zone. In all the silicon ELO samples, the growth rate in the lateral direction tended to be lower than that in the vertical direction. Comparing Sample #1 and #2, where the HCl gas flow rate was fixed at 100 sccm and SiH_2Cl_2, as a source gas, was injected at flow rates of 20 sccm and 10 ccm, respectively, with a fixed HCL gas flow rate of 100 sccm, the Si ELO growth rate increased lin-

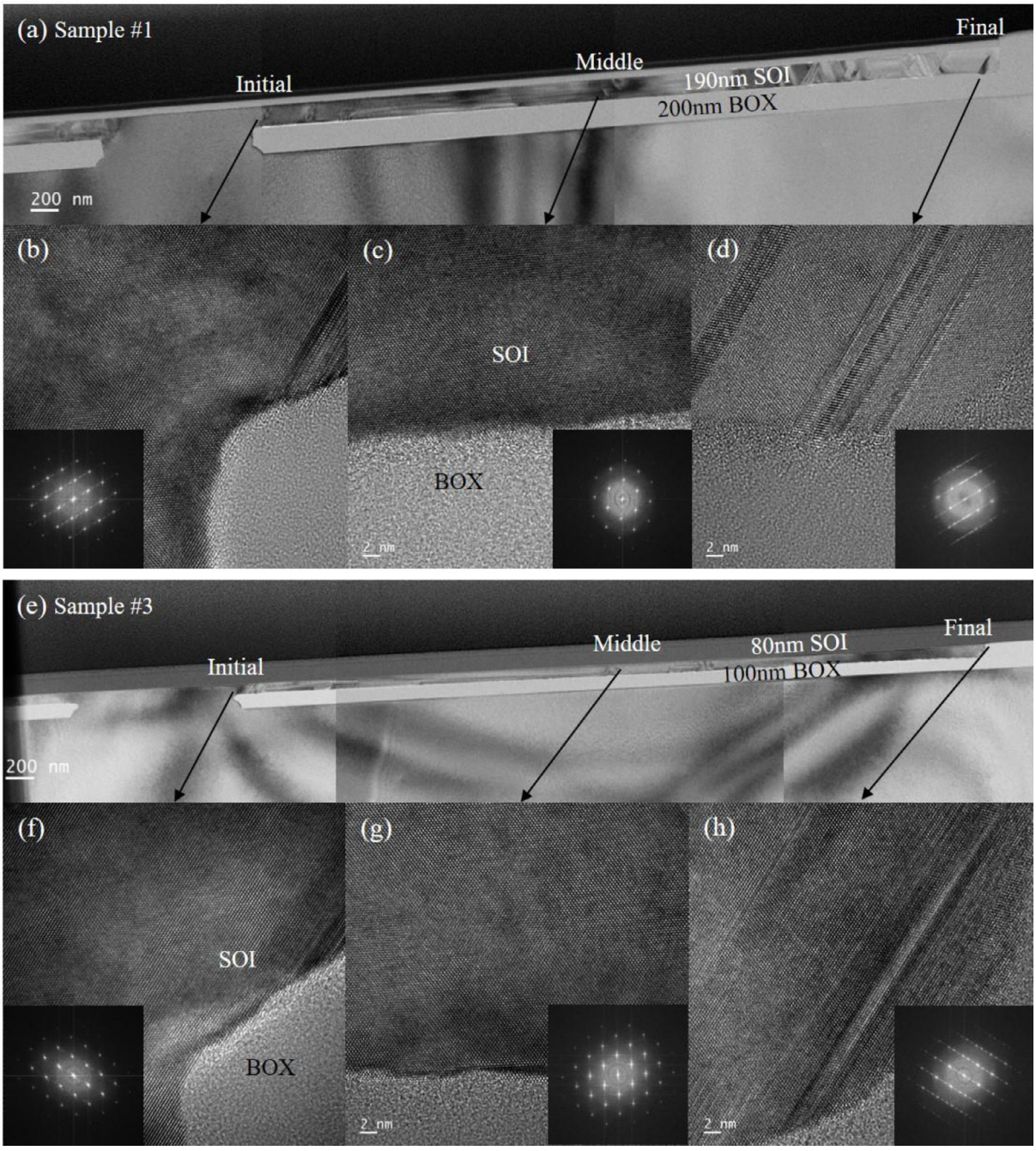

Fig. 3. Cross-sectional high-resolution TEM images of Sample #1 and Sample #3: (a) and (e) Bright field TEM images of silicon grown on thin SiO_2 by microsampling with FIB and seed zone where the silicon remains flat and uniform after CMP. (b)–(d) and (f)–(h) High-resolution TEM images with the insets showing the diffraction patterns in the initial, middle, and final stages of growth on the upper-side silicon on thin SiO_2.

early with the increasing SiH_2Cl_2 flow. However, the growth ratio in the lateral direction to the vertical direction was 0.925 in Sample #1 with a SiH_2Cl_2/HCl ratio of 0.2 and 0.806 in Sample #2 with a SiH_2Cl_2/HCl ratio of 0.1; a difference of more than 12 %. In addition, in Sample #3, in which the heights of the silicon seed zone and etch stopper were both 100 nm, the growth ratio in the horizontal and lateral directions was 0.839, slightly higher than that in Sample #2 in which the aforementioned heights were set to 200 nm each. A faster growth in the lateral direction than in the vertical direction is beneficial for the silicon ELO in terms of monetary and time cost associated with the local SOI fabrication proposed herein. However, the crystallinity of the local SOI layer is the most important factor in terms of the platform used for device fabrication. Therefore, it is necessary to analyze the crystallinity or the surface state of the local SOI layer of each sample.

The selectively grown silicon ELO layer forms a flat shape on the front surface of the wafer after the CMP process, enabling its use it as a common platform for IC chips. The thickness of the local SOI layer is determined by the etch depth, determined by forming an etch stopper on the thick SiO_2 layer. The etch stopper layer serves to prevent excessive silicon polishing of the silicon ELO layer during the CMP process for the silicon ELO layer and provides complete isolation between the chips fabricated on the local SOI. All the silicon ELO samples were polished under the same CMP conditions described before, and the CMP process was

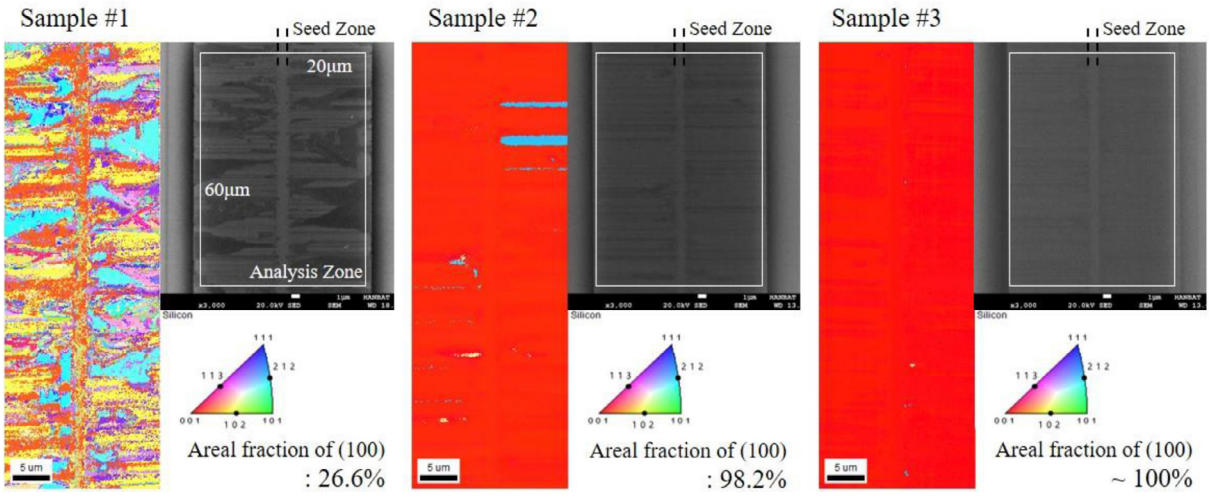

Fig. 4. EBSD and 60°-tilted SEM images of the local SOI layer fabricated on amorphous SiO_2, including seed zone, as indicated by a black dotted band in Samples #1, #2, and #3 (inset of inverse pole figure of silicon). The total fraction of the (001) plane, which is the crystal plane of the silicon wafer, is significantly different in each sample.

stopped when SiO_2 was detected and the etch stopper line began to be exposed. To analyze the crystallinity of the local SOI layer using TEM, an area 5 μm away from the silicon seed zone and the etch stopper was designated as a cross-sectional specimen using FIB-assisted SEM.

The crystallinity of the silicon grown in Samples #1 and #3 was scrutinized by cross-sectional high-resolution TEM and the diffraction patterns corresponding to the initial, middle, and final stages of growth are shown in the insets of Fig. 3. The cross-sectional TEM image of Sample #1 (Fig. 3(a)) shows that the silicon single crystal layer located on top of the silicon seed zone is clean without noticeable defects, such as short-range disorders. However, in the localized SOI layer above the BOX layer, several straight lines can be observed indicating twins - a type of plane defect that is formed under mechanical stress. Typically, a twin can be recognized by the many parallel straight lines observed inside a single crystal. We were careful of twins by avoiding mechanical thinning process during sample preparation. The TEM image of Sample #3, which was grown at a lower growth rate and had a thinner BOX layer, also shows twins only in the local SOI layer; however, the defect frequency is lower than that in the case of Sample #1. In the initial stage, silicon starts to gradually change its main mode of growth, i.e., from vertical to both lateral and vertical, when it passes the SiO_2 aperture of the silicon seed zone. When the growing silicon reaches the aperture, the incoming atoms are exposed to different environments owing to the presence of amorphous SiO_2. Consequently, this change can affect the lattice stability, built-up stress, bonding with SiO_2, and the growth rate of the silicon layer, resulting in the formation of twins, as shown in the cross-sectional high-resolution TEM images in Fig. 3. Twins can also be formed by stresses that develop during cooling after growth at a high temperature (e.g., 1000 °C). The linear thermal expansion coefficient of crystalline silicon is in the range of 2.7 – 4.5 $\times$ 10^{-6}/K from room temperature to 1000 °C, whereas that of SiO_2 is in the range of 0.55–0.75 $\times$ 10^{-6}/K at the same temperature. Therefore, stresses may be induced at the interface during the cooling process after silicon ELO growth owing to the significant difference in the thermal expansion coefficients. The high-resolution TEM images of Sample #1 (Fig. 3(a) and (d)) show that one black line in the final stage comprises several twins. Additionally, TEM diffraction patterns showed the coexistence of a typical silicon pattern with dotted line patterns passing through the main reciprocal lattice points on the Ewald sphere—a characteristic of twins. Similarly, the final stage is likely to experience environmental change because the thick SiO_2 etch stopper prevents lateral growth, causing more twin layers to appear than that in the initial stage. A thick, amorphous thick SiO_2 layer is reflected in the diffraction pattern as a blurred circular shape (Fig. 3(b)). In contrast, the middle stage shows higher crystallinity than both the initial and final stages. This result implies that once lateral growth begins after the transient time of the initial stage, silicon epitaxy can be maintained on the amorphous SiO_2 in the lateral direction, with good crystallinity. In addition, Sample #3 exhibited higher crystallinity than Sample #1, as reflected by the more defined circular shape in the TEM diffraction analysis, in all regions of the SOI layer.

To determine whether the silicon layer grows into an epitaxial, polycrystalline, or amorphous phase, we investigated the grown silicon layer by EBSD equipped with SEM. The present EBSD analysis can analyze specific regions and provide information on the surface lattice in different colors using X-ray diffraction. Because the electron range of the EBSD is narrow enough to exclude the interference by the silicon substrate, we can acquire crystalline information on the crystallinity of the pure grown layer. We obtained an EBSD color maps of Sample #1, #2, and #3, showing the major crystal planes of the grown silicon layer, with an area of 20 $\times$ 60 μm (Fig. 4), using the inverse pole figure method, which involves projecting the lattice planes on the upper hemisphere of the diffraction pattern. The SEM image of Sample #1, which has a higher growth rate and a thicker seed zone height, shows that the grown silicon layer, starting from the seed zone of the black dotted band, comprises dark and light gray parts. The seed zone (shown in light gray) is epitaxially grown, spreading over the entire region. In comparison, discontinuous layered shapes along the lateral growth direction (shown in dark gray) seem to deviate from the epitaxial growth track. This was also confirmed by EBSD analysis, which showed that the silicon thin film, epitaxially grown on the amorphous SiO_2 layer of Sample #1, contained the crystal plane of the silicon substrate, i.e., the (001) plane, as well as several crystal planes of the silicon lattice. The (001) planes in the area analyzed by EBSD in Sample #1 constituted only 22.6 %. However, as the facet planes are clearly seen in the silicon ELO, this does not mean that the local SOI layer is polycrystalline, and the EBSD map differs entirely in terms of the polycrystalline grain boundary. In the silicon ELO layer, grown at 1000 °C, the generation of a built-up stress is expected at the interface owing to the high growth rate

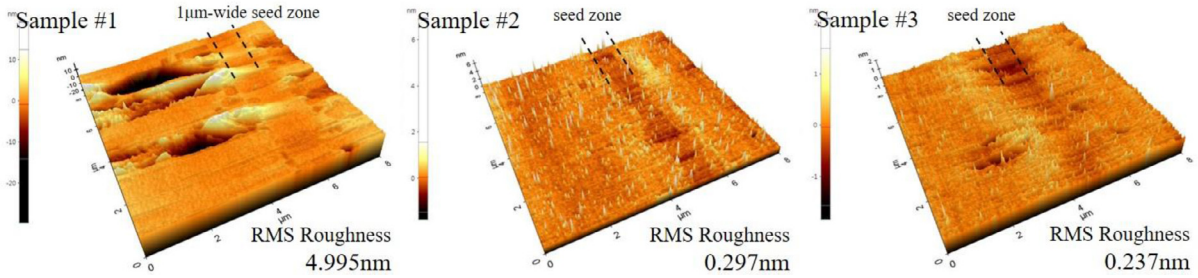

Fig. 5. AFM surface roughness analysis of an 8 × 8 μm area of the samples. Note that the silicon seed zone and the local SOI in Sample #3 show a smooth surface at the bulk silicon wafer level, in Sample #3.

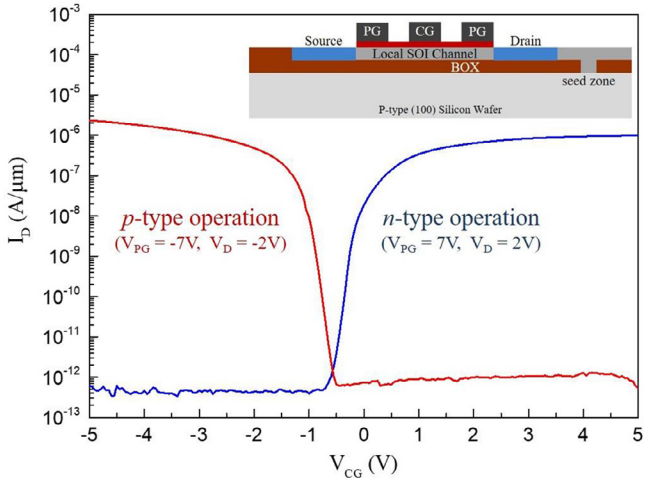

Fig. 6. Current-voltage properties of reconfigurable MOSFET fabricated on the present local SOI wherein single device can behave either as *n*-type or *p*-type MOSFET according to the bias conditions (inset of the schematic cross-section of RFET).

and the difference in the thermal expansion coefficients of silicon and SiO_2. These factors induced planar defects, such as twins, and resulted in the appearance of multiple crystal planes. In Sample #2, which had a low growth rate, the total fraction of the (001) plane increased dramatically to 98.2 %, and the sharpness in contrast between the dark and light gray parts in the SEM image is even lower (Fig. 4). This trend is more pronounced in Sample #3, which had a smaller ratio of BOX/etch stopper height, and the total fraction of the (001) plane, which is the crystal plane of the silicon wafer, was 100 %. The EBSD results demonstrate that that silicon ELO exhibited higher crystallinity than others when grown on a thin BOX, while maintaining a low silicon growth rate.

The surface morphology of the samples was analyzed by AFM, with a scanning area of 8 × 8 μm, including the silicon seed zone (Fig. 5). The vertical scale is enhanced by 4–50 nm to emphasize the surface undulations. The AFM results show largely the same trend as the EBSD analysis, with the root mean square (RMS) surface roughness decreasing sharply from 4.995 nm in Sample #1 to 0.297 nm in Sample #2 with a low silicon ELO growth rate. The RMS roughness of Sample #3, which has a lower BOX/etch stopper height, was further reduced to 0.237 nm, resulting in a smooth surface similar to that of the bulk silicon wafer.

To ascertain the crystalline quality of the present ELO silicon, we fabricated reconfigurable metal-oxide-semiconductor field effect transistors (MOSFETs) on the present local SOI, which can be either an n-type or p-type MOSFET that is usually implemented on intrinsic type SOI wafers. Fig. 6 shows the current-voltage characteristics of the present reconfigurable MOSFET with two polarity gates (PG) and a control gate (CG) wherein the PGs control the energy barrier between the swappable source/drain and the CG as a conventional MOSFET gate. Because of the limited process technology, the gate length of PG, CG, and the spacing between them is as large as 0.8 μm, resulting in a small normalized current in the order of a few ~μA/μm. Nonetheless, the device clearly shows reconfigurable features that behave as an n-type MOSFET when a positive bias is applied to all the gates and as a p-type MOSFET when a negative bias is applied.

4. Conclusions

We successfully grew a large silicon epitaxial layer over an amorphous SiO_2 using a small seed window. A local SOI layer, processed to less than 100 nm through an etch stopper, was formed over a large area covering a few hundreds of square micrometers, at which scale even complex logic gates can be fabricated. The high crystallinity of the local SOI layer was closely related to the growth rate of the silicon ELO layer and the thickness of the underlying SiO_2 layer. Under optimized growth conditions, the formation of a local SOI layer exhibiting a surface roughness equal to that of the bulk silicon wafer and a (100) plane same with the crystal plane of the substrate was confirmed by TEM, EBSD, and AFM analyses. Plane defects, such as twins, were also found in the silicon seed zone and near the etch stopper; nevertheless, once lateral growth started after the transient time of the initial stage, silicon epitaxy on amorphous SiO_2 could be maintained in the lateral direction, with good crystallinity. Owing to the surface properties of the underlying SiO_2 and the difference in the thermal expansion coefficients of the crystalline silicon and SiO_2, the formation of twins in the local SOI layer was attributed to the built-up stress at the interface. This aspect will be further investigated in future work to understand the underlying mechanism. This type of epilayer is widely applicable to the present and prospective IC fabrication techniques, some of which rely on expensive SOI technologies. We successfully fabricated reconfigurable MOSFETs on the reported local SOI layer. Future work will focus on the fabrication of NAND and XOR logic gates.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Sang-Hoon Kim: Investigation, Methodology, Data curation, Writing – original draft. **Seong Hyun Lee:** Methodology, Data curation. **Jeong-Woo Park:** Formal analysis, Validation. **Tae Moon Roh:** Methodology, Formal analysis. **Dongwoo Suh:** Conceptualization, Funding acquisition, Project administration, Writing – original draft, Writing – review & editing.

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