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Three-dimensional wavelength-division multiplexing interconnects based on a low-loss Si_xN_y arrayed waveguide grating

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Abstract: We fabricate three-dimensional wavelength-division multiplexing (3D-WDM) interconnects comprising three Si_xN_y layers using a CMOS-compatible process. In these interconnects, the optical signals are coupled directly to a Si_xN_y grating coupler in the middle Si_xN_y layer and demultiplexed by a 1×4 Si_xN_y array waveguide grating (AWG). The demultiplexed optical signals are interconnected from the middle Si_xN_y layer to the bottom and top Si_xN_y layers by four SiO_xN_y interlayer couplers. A low insertion loss and low crosstalk are achieved in the AWG. The coupling losses of the SiO_xN_y interlayer couplers and Si_xN_y grating coupler are ~1.52 dB and ~4.2 dB, respectively.

1. Introduction

High-density integrations with compact photonic devices based on silicon, silicon nitride (Si_xN_y), InP, and $LiNbO_3$ photonics have attracted considerable attention for applications in 5G/6G, quantum optics, and neuromorphic photonics [1–9]. Recently, the number of photonic components in complex photonic integrated circuit (PIC) systems has been rapidly increasing. However, this high-density integration of the PIC is limited by the relatively large size of the photonic components and the minimum distance between optical waveguides (WGs) required to suppress crosstalk [10]. It has become increasingly difficult to integrate all the necessary photonic components into a two-dimensional (2D) structure. Thus, the three-dimensional PIC (3D-PIC) is an excellent candidate for solving the above limitations associated with integration in the 2D-PIC. Moreover, various studies have demonstrated the increase in integration density in a 3D-PIC structure [10–16]. On the other hand, wavelength division multiplexing (WDM) is a key technology that can enlarge the data transmission capacity. Various WDM devices fabricated on a 2D plane such as Si, Si_xN_y, InP, and SU8 based AWGs have been reported [17–24]. Furthermore, the incorporation of WDM devices into 3D structures increases the data capacity and offers a high integration density in the 3D-PIC, while maintaining a compact size. Several WDM devices embedded in 3D structures have been reported, but there are no optical interconnections between vertical layers within 3D structures or only simulation results [25–26].

This paper reports a 3D-WDM interconnect based on three Si_xN_y layers, which includes a four-channel Si_xN_y AWG, a Si_xN_y grating coupler, and four SiO_xN_y interlayer couplers. In the fabricated 3D-WDM interconnect device, the input multiplexed optical signal is vertically coupled to the middle layer by the Si_xN_y grating coupler and is then demultiplexed by the Si_xN_y AWG. The demultiplexed signals travel from the middle Si_xN_y layer to the lower and upper Si_xN_y layers through a SiO_xN_y interlayer coupler. A low insertion loss for the embedded Si_xN_y AWG is achieved in the 3D-WDM interconnects by incorporating the Si_xN_y grating coupler and SiO_xN_y

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interlayer couplers. The fabricated 3D-WDM interconnects show that the Si_xN_y AWG can play a role in the 3D structure with low loss.

2. Design and fabrication

Figure 1 shows a schematic of the 3D-WDM interconnects consisting of three Si_xN_y layers, which includes a grating coupler, a 1×4 Si_xN_y AWG, and four SiO_xN_y interlayers couplers positioned between the Si_xN_y layers. First, a multiplexed optical signal is coupled into a Si_xN_y grating coupler in the Si_xN_y layer 2 and demultiplexed by a 1×4 Si_xN_y AWG. By using the SiO_xN_y interlayer couplers, the two output signals of the Si_xN_y AWG are interconnected to the WGs (D1 and D2) in the Si_xN_y layer 1, and the other two signals are interconnected to the WGs (U1, U2) in the Si_xN_y layer 3.

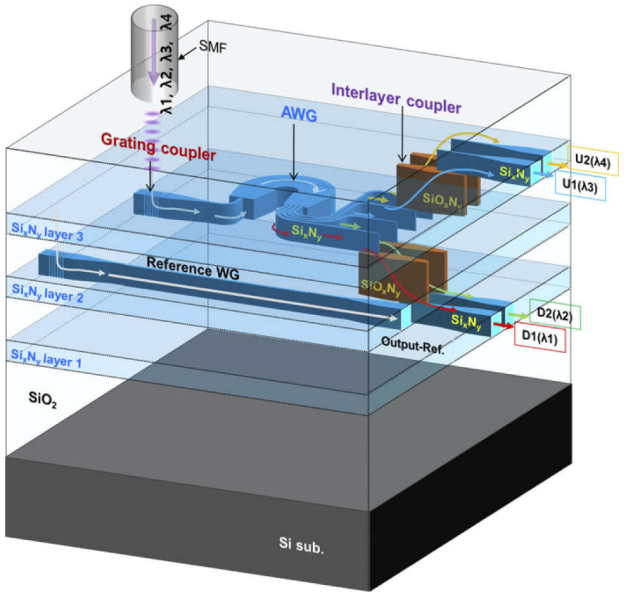

Fig. 1. Schematic illustration of 3D-WDM interconnects consisting of three Si_xN_y layers, which includes a grating coupler, four-channel Si_xN_y AWG, and four SiO_xN_y interlayer couplers positioned between Si_xN_y layers.

The single-mode conditions in the Si_xN_y WG are calculated as a function of the cross-sectional area ($W \times T$), and the height of the Si_xN_y WG is set to 0.5 μm for the single-mode operation of the 3D-WDM interconnect device, as shown in Fig. 2(a). Figure 2(b) illustrates the schematics of the Si_xN_y grating coupler. To achieve a high coupling efficiency for the Si_xN_y grating coupler, simulations are performed with various grating periods (P), etch depths (D), and incident angles of a single-mode fiber (θ) using Lumerical FDTD [27] under the condition of applying index-matching oil. For a fixed thickness (T_g) of 0.5 μm, Figs. 2(c) and 2(d) show the coupling efficiency as a function of P and D, respectively. Optimal design parameters, $P = 960$ nm, $D = 360$ nm, and $\theta = 3.68°$, are obtained with a coupling efficiency of 55.6% using a parametric sweep.

In 3D photonic interconnects using vertically stacked Si_xN_y layers, crosstalk between Si_xN_y layers needs to be as small as possible to achieve the best performance for each photonic component within the 3D-PIC. An interlayer coupler connecting two Si_xN_y WGs with a large spacing layer is required to achieve a low-crosstalk condition. Simulations for the interlayer coupler are performed via Lumerical eigenmode analysis [27]. The SiO_xN_y material, which

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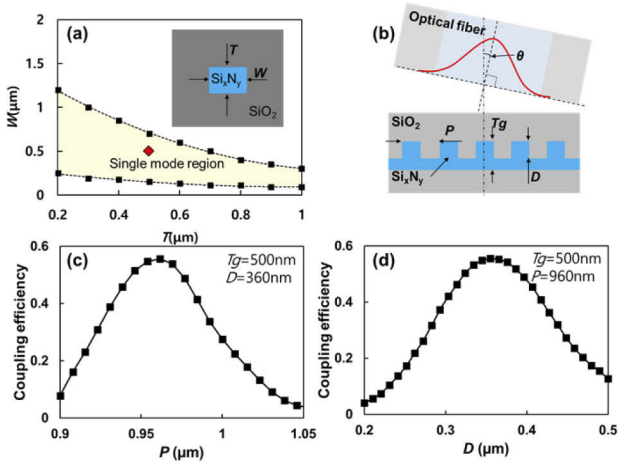

Fig. 2. (a) Calculated single-mode conditions in the Si_xN_y WG as a function of cross-sectional area ($W \times T$). (b) Schematic diagram of the Si_xN_y grating coupler used in the simulation. Coupling efficiency of the Si_xN_y grating coupler as a function of (c) P and (d) D.

has a lower refractive index compared to Si_xN_y WGs, was chosen for the fabrication of the interlayer coupler because the optical modes that propagate the lower refractive index WG can easily recombine into an optical WG with a higher refractive index. In addition, since the mode size increases in the interlayer coupler having a low refractive index, the spacing between the Si_xN_y layers can be made larger and noise generated between the Si_xN_y layers can be minimized. Figure 3 shows a schematic illustration and the calculated coupling efficiency of the SiO_xN_y interlayer coupler. The Si_xN_y WG with a cross-sectional area of $0.5 \times 0.5\ \mu m^2$ in layer 1 is positively tapered and overlaps with a SiO_xN_y bidirectional taper structure whose cross-sectional area ($W_{SiON} \times T_{SiON}$) is tapered in both directions for length L_t. In addition, the SiO_xN_y bidirectional taper structure overlaps with the inversely tapered Si_xN_y WG of layer 2. The Si_xN_y and SiO_xN_y structures have a tapered tip width of 0.2 μm. The refractive index of SiO_xN_y is 1.862 at $\lambda = 1.55$ μm. The efficiency of coupling between the Si_xN_y WGs, located in layers 1 and 2, by the SiO_xN_y interlayer coupler with a fixed W_{SiON} of 1 μm and various T_{SiON} is calculated as a function of L_t. For T_{SiON} of 1 μm, 1.5 μm, and 3 μm, coupling efficiencies of more than 95% are obtained when L_t is above 20 μm, 40 μm, and 130 μm, respectively.

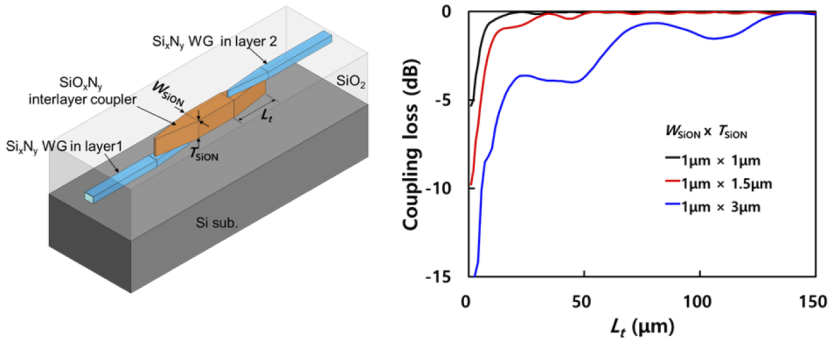

Fig. 3. Schematic illustration and calculated coupling efficiency as a function of L_t of the SiO_xN_y interlayer coupler.

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Light scattering at the star coupler boundary in the AWG causes an increase in the insertion losses and crosstalk. A Si_xN_y AWG is designed using a double-etched structure that combines a shallowly etched inverse-tapered WG and a deeply etched channel WG to suppress scattering at the star coupler boundary, as shown in Fig. 4(a). The adiabatic mode conversion from a slab WG to an arrayed WG is simulated with optimal design parameters such as slab WG thickness (0.5 μm), inverse taper length ($d_t = 5$ μm), distance ($r = 9$ μm) from slab WG to channel arrayed WG, shallow etch depth (0.3 μm), and arrayed WG thickness (0.8 μm). Figure 4(b) shows the optical mode field profiles and cross-sectional images at positions ①–⑤ in Fig. 4(a). A simulation of the optical mode field profiles is performed using the Lumerical eigenmode analysis [27]. The simulation results indicate that the slab mode was converted adiabatically to the fundamental mode of the arrayed WG. The designed Si_xN_y AWG consists of 1×4 channels with a 5-nm-channel spacing, and a wide free spectral range of 40 nm is applied to improve the uniformity of the insertion loss. A compact device with a size of 500×650 μm^2 is achieved with a star coupler focal length of 85.93 μm and a length difference of 27.19 μm between adjacent arrayed WGs.

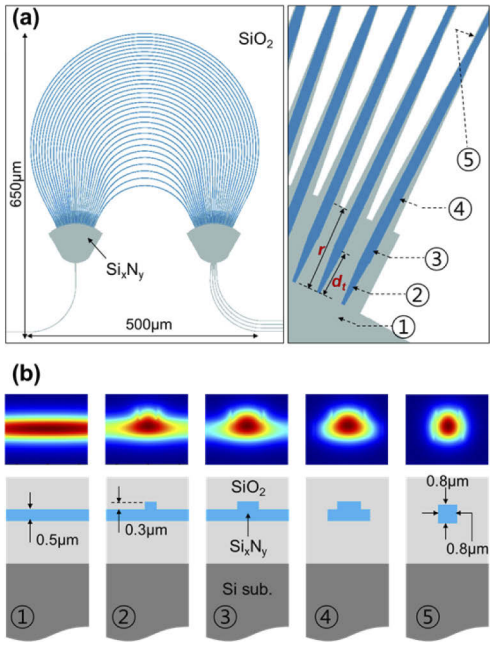

Fig. 4. (a) Schematic diagram of Si_xN_y AWG and star coupler boundary and (b) optical mode fields at each point in the star coupler boundary.

Based on the aforementioned simulation results, the 3D-WDM interconnects including the Si_xN_y grating coupler, Si_xN_y AWG, and SiO_xN_y interlayer couplers were fabricated. Figure 5 shows the fabrication process of the 3D-WDM interconnect device. Layer 1, layer 2, and layer 3 of the Si_xN_y, with thicknesses of 0.5 μm, 0.8 μm, and 0.5 μm, respectively, were deposited via plasma-enhanced chemical vapor deposition (PECVD) and etched to fabricate the grating coupler, AWG, and vertically interconnected WGs. Before layers 2 and 3 were deposited, the SiO_2 spacing layer was covered and flattened via chemical–mechanical polishing (CMP). To fabricate the interlayer coupler, SiO_2 was etched into a vessel with a bidirectional tapered structure. Subsequently, the SiO_xN_y was filled into the vessel structure, and the SiO_xN_y layer was planarized via CMP. The SiO_2 etch rate is carefully controlled to protect the Si_xN_y waveguide from over etching.

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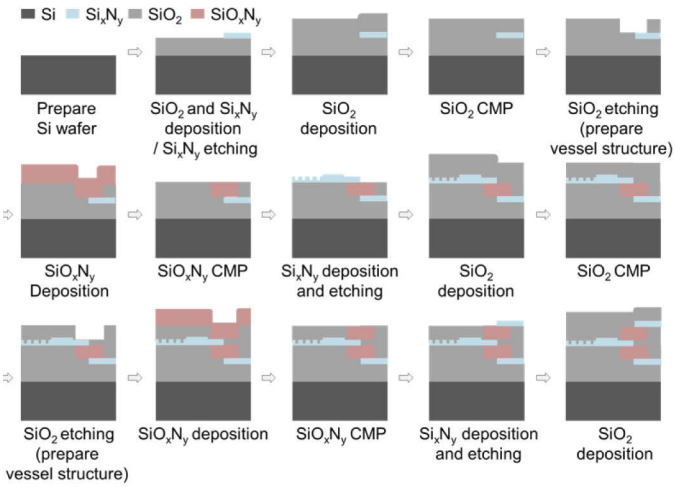

Fig. 5. Fabrication process of the 3D-WDM interconnect device.

Figure 6 shows microscopic images and an SEM image of the fabricated 3D-WDM interconnect device. The top view of the microscopic image in Fig. 6(a) shows the 3D-WDM interconnect device consisting of a Si_xN_y grating coupler, a 1×4 Si_xN_y AWG, and SiO_xN_y interlayer couplers. The reference WG consists only of a Si_xN_y grating coupler and a single-mode Si_xN_y WG. The cross-sectional microscopic image in Fig. 6(b) shows the output waveguides (D1, D2, U1, and

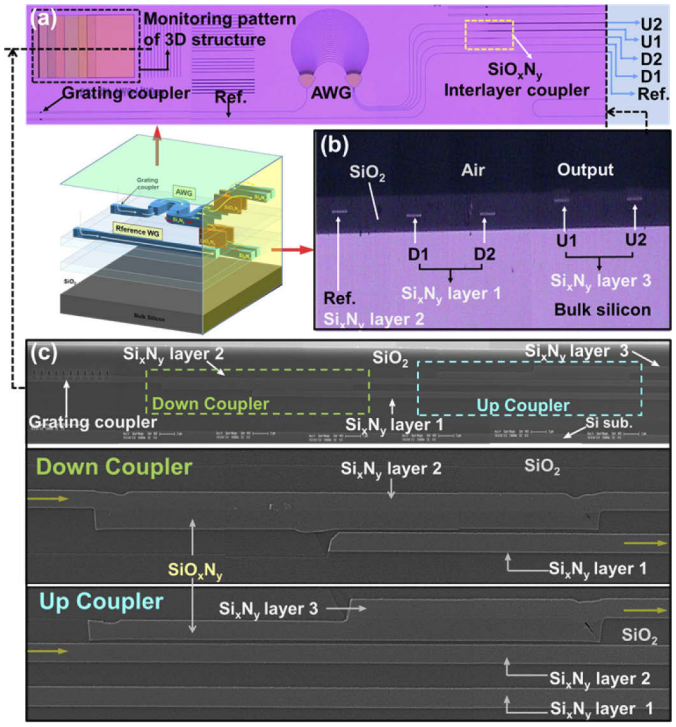

Fig. 6. Microscopic images ((a) Top view, (b) side view) and (c) cross-sectional SEM images of the fabricated 3D-WDM interconnect device.

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U2) and the reference WG of the fabricated 3D-WDM interconnect device. The SEM image in Fig. 6(c) shows the cross-section of the monitoring pattern of the 3D structure in Fig. 6(a) consisting of a Si_xN_y grating coupler, three Si_xN_y layers, and two SiO_xN_y interlayer couplers. The Si_xN_y grating coupler was fabricated with a period of 960 nm, a Si_xN_y thickness of 491 nm, and an etch depth of 373 nm. In the interlayer coupler, the SiO_xN_y thickness was 0.5 μm. The measured refractive indices of the Si_xN_y and SiO_xN_y layers at $\lambda = 1.55$ μm were 2.11 and 1.862, respectively. To improve the roughness of the surface after the CMP, wet etching using a buffered oxide etch (BOE) (30:1) was performed for 5 seconds. The wafer was annealed at 600°C for 30 min to improve the adhesion between the vertically stacked layers. A CMOS-compatible process using I-line photolithography was used to fabricate the devices.

3. Experiments and discussions

The output facet of the fabricated 3D-WDM interconnect device was polished to couple the output optical signal to the cleaved single-mode fiber. The optical spectra of the fabricated 3D-WDM interconnect devices were measured using an optical spectrum analyzer (Agilent 86143 B) and a broadband light source (EDFA). The measured optical spectra of the fabricated 3D-WDM interconnect devices were normalized using a reference WG. The propagation loss was measured by the cutback method, and the measured propagation loss of the Si_xN_y WG using the CMP process was 0.2 dB/mm.

Figure 7 shows the calculated and measured coupling efficiencies of the Si_xN_y grating coupler fabricated in the 3D-WDM interconnect device. The dimensions of the grating coupler were obtained, and the void (air gap) was determined via the SEM image. The period of the grating couplers was 960 nm. The Si_xN_y thickness, etch depth, and duty cycle measured on the grating coupler were 491 nm, 373 nm, and 0.42, respectively. To measure the coupling loss, the measured transmission spectrum of the grating coupler was normalized by the spectrum of the input light. The measured coupling loss was 4.2 dB with a 1-dB bandwidth of ~62 nm. The simulations of the fabricated grating coupler structure with the void (GC_w_void) and without

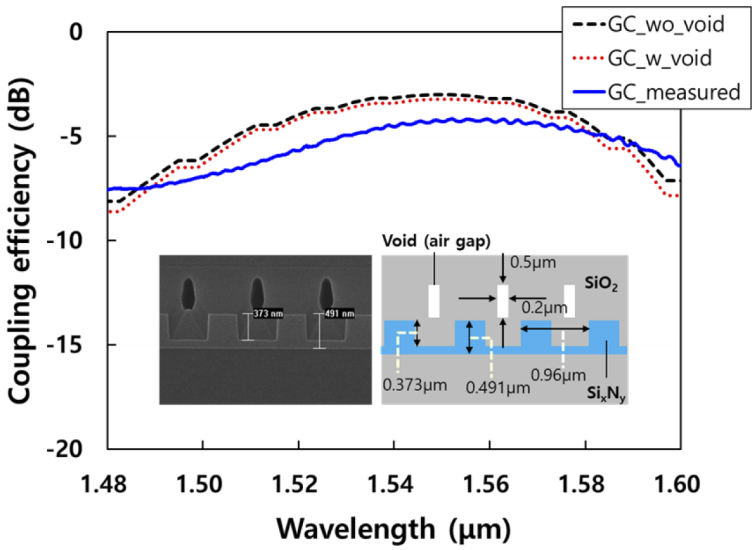

Fig. 7. Calculated and measured coupling efficiency of the Si_xN_y grating coupler fabricated in the 3D-WDM interconnect device. The inset shows the SEM image and schematic diagram of the fabricated grating coupler.

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void (GC_wo_void) were performed using the Lumerical FDTD [27]. The calculated coupling losses for the GC_w_void and GC_wo_voids were 3.2 dB and 3.0 dB, and the 1 dB bandwidths were 57 nm and 58 nm, respectively. Calculations indicate that the void does not significantly affect the coupling loss and 1 dB bandwidth. Therefore, the measured loss is relatively large compared to the calculation result due to the surface reflection between the air and the SiO_2 upper cladding of the grating coupler, sidewall roughness, and the imperfections of the measurement such as the fiber angle and polarization. In addition, the Si_xN_y grating coupler was fabricated in a 2D structure, and a coupling loss of 3.7 dB was measured with a 1 dB bandwidth of ~70 nm. The performance degradation in the grating coupler in the 3D interconnect device compared to that in the 2D structure may result from the different cladding thickness.

Figure 8 shows the measured and calculated coupling losses of the fabricated SiO_xN_y interlayer coupler with a thickness (T_{SiON}) of 0.55 μm and a width (W_{SiON}) of 1 μm. Figure 8(b) shows the calculated coupling loss of the proposed SiO_xN_y interlayer coupler, as shown in Fig. 8(a). Figures 8(d)–(f) show the measured coupling loss of the fabricated SiO_xN_y interlayer coupler and the calculated coupling loss for the SiO_xN_y interlayer coupler including the voids, as shown

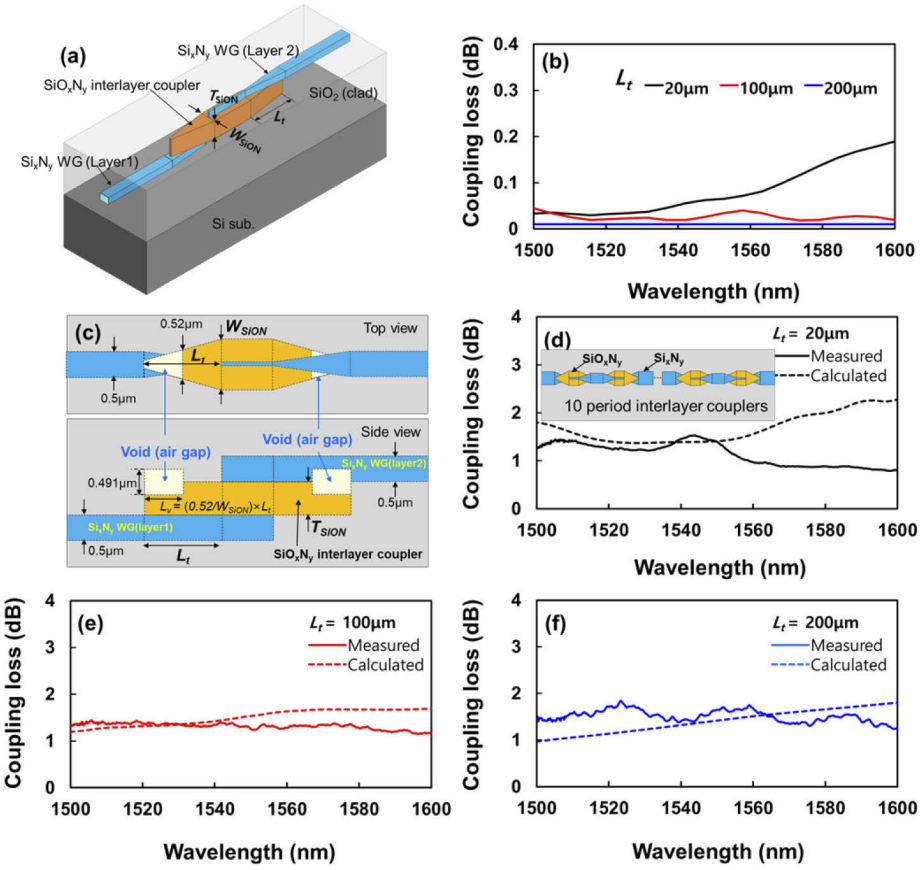

Fig. 8. (a) Schematic of the proposed SiO_xN_y interlayer coupler. (b) Calculated coupling efficiency of the SiO_xN_y interlayer coupler in Fig. (a). (c) Schematic of the SiO_xN_y interlayer coupler including voids. (d)-(f) Measured coupling loss of the fabricated SiO_xN_y interlayer coupler, and the calculated coupling loss for the SiO_xN_y interlayer coupler including the voids in Fig. 8(c). Illustration in Fig. 8(d): schematic diagram of 10 period SiO_xN_y interlayer couplers.

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in Fig. 8(c). In order to measure the coupling loss of the SiO_xN_y interlayer coupler, the measured transmission spectrum for 10 period SiO_xN_y interlayer couplers as shown in the illustration of Fig. 8(d) were normalized by the transmission spectrum of the straight waveguide. A simulation of the SiO_xN_y interlayer coupler, including the voids, was performed using the Lumerical eigenmode analysis [27]. Simulations were performed for various void dimensions and compared with experimental results. When fabricating the SiO_xN_y interlayer couplers, a SiO_xN_y layer was deposited via the PECVD on a pre-etched SiO_2 vessel structure with a bidirectional tapered pattern. At this time, it was difficult to fill the SiO_xN_y into a narrow taper structure, and voids were produced during this process. The measured coupling losses were within the range of 0.8–1.7 dB for the interlayer coupler with an inverse taper length (L_t) of 20, 100, and 200 µm. The experimental and calculated results were mutually consistent implying that the measurement loss increases as a result of the mode mismatch between the Si_xN_y WG, and SiO_xN_y interlayer couplers caused by the voids generated in the interlayer coupler. This problem can be solved by correcting the fabrication process of the interlayer coupler or using other methods, as reported in [15].

For a spectral measurement of the fabricated 3D-WDM interconnect device, the optical signal was combined with a Si_xN_y grating coupler in the Si_xN_y layer 2. Then the demultiplexed spectra of the 1 × 4 Si_xN_y AWG were measured at the outputs of the Si_xN_y layer 1 (D1 and D2) and outputs of the Si_xN_y layer 2 (U1 and U2). Figure 9(a) shows the measured insertion loss in more than ten 3D-WDM interconnect devices. The average insertion loss was 3.03 dB, which includes the losses of the Si_xN_y AWG and SiO_xN_y interlayer couplers. The standard deviation of the insertion loss was 0.401 dB. By correcting the average loss of the interlayer coupler, 1.52 dB, from the average loss of the 3D interconnect devices, a low average loss of 1.51 dB was

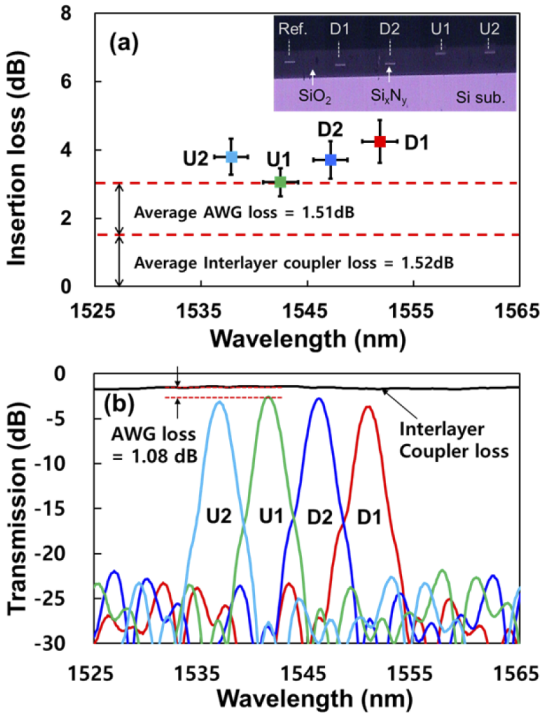

Fig. 9. (a) Average insertion loss measured on more than ten 3D-WDM interconnect devices. (b) Measured normalized transmission spectra of the best device among the fabricated 3D-WDM interconnect devices.

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obtained for a Si_xN_y AWG with a loss non-uniformity of 1.19 dB. In addition, the standard deviation of the peak position was approximately 1.625 nm, owing to the sidewall roughness and the non-uniformity of the thickness of the Si_xN_y WG based on the CMP process. Figure 9(b) shows the measured normalized transmission spectra of the best device among the fabricated 3D-WDM interconnect devices. The measured insertion losses of the 3D-WDM interconnect devices were within 2.54–3.67 dB with a crosstalk within the range of −22.61 to −25.06 dB. The insertion loss of the Si_xN_y AWG with a loss correction using the transmission spectrum of the SiO_xN_y interlayer coupler was within 1.08–2.01 dB. The reported low-insertion losses of the Si_xN_y AWGs fabricated with 2D structures operating at C-band were 0.9 dB [21], and 1.5–2.7 dB [28], respectively. The results indicated that the low-loss operation of the Si_xN_y AWG was possible in 3D structures, even though the CMP process increased the propagation loss and non-uniformity. The insertion loss and uniformity of the 3D-WDM interconnect device could be improved by optimizing the conditions of the fabrication process and the design parameters.

4. Conclusions

In this study, 3D-WDM interconnects consisting of three Si_xN_y layers with a Si_xN_y grating coupler, a 1×4 Si_xN_y AWG, and SiO_xN_y interlayer couplers were fabricated. The optical signal coupled with a Si_xN_y grating coupler at the Si_xN_y layer 2 was demultiplexed by a 1×4 Si_xN_y AWG and then interconnected to the output Si_xN_y WGs at the Si_xN_y layer 1 and Si_xN_y layer 3 by the SiO_xN_y interlayer couplers. In the fabricated 1×4 channel Si_xN_y AWG within the 3D structure, a low insertion loss within 1.08–2.01 dB was achieved with a low crosstalk within −22.61 to −25.06 dB. The coupling loss of the SiO_xN_y interlayer couplers was ∼1.52 dB and that of the Si_xN_y grating coupler was ∼4.2 dB. The results show that the Si_xN_y AWG embedded in the 3D structure performed accurately with low insertion loss. Moreover, the 3D-WDM interconnects can be improved to the application level by improving the performance of the Si_xN_y AWG and SiO_xN_y interlayer couplers and optimizing the design parameters and fabrication process. The 3D WDM interconnect device can be applied to complex integrated photonics systems that require large-capacity data transmission such as data center, 5G/6G, and high-performance computing. By assigning different wavelengths to each of the vertically stacked layers and giving them various functions, complex photonics systems can be systematically and compactly integrated.

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Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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