Analysis of temporal carrier build-up in reconfigurable field-effect transistor

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Based on the analysis of the carrier density change of a symmetric gate reconfigurable field-effect transistor that can operate p- or n-type transistors in an integrated circuit (IC), its unique limiting factor, carrier build-up time, is quantitatively derived for operating speed in addition to conventional resistance and capacitance (RC) and transit time effect. Originating from the characteristic of carrier confinement in a channel between two Schottky potential barriers, the carrier build-up time for the operation could take up to ∼1000 times longer than the transit time across the channel.

Introduction: Given that tremendous transistors are required for contemporary machine learning processing and cutting-edge ICs, there is an urgent need to find solutions that address the issue of power consumption of semiconductor chips. To achieve this, several attempts have been made to find a new device such as a reconfigurable field-effect transistor (RFET) that can play either a n- or p-type metal-oxide semiconductor field-effect transistor(MOSFET) by a single transistor [1–5]. If an RFET can be realized and ideally incorporated in integrated circuits, the issue of chip density and power consumption can be substantially addressed because the number of transistors can be reduced, even not completely replaced. Furthermore, the application area of RFETs has recently expanded to neural networks owing to time-modulated multi-value features, which are key features necessary for the realization of a binarized neural network [4, 6]. Because of these advantages, many aspects of RFET have been studied with respect to static device properties [1, 2], logic operation [3], and applicability to neural networks [4]. Nonetheless, previous studies rarely cover the dynamic behaviours of RFETs, which must be preliminarily established for the aforementioned applications. The RC effect and velocity of charge carriers in the channel are speed-limiting factors that they are in the MOSFET. However, the RFET has one more point to be considered owing to the structural feature of the potential barrier. Although the observation of the transient behaviours of carrier density is important, understanding the carrier dynamics of fabricated 3-gate RFETs can be meaningful guidance for the application of RFET. In the present study, we investigated device factors that limit the speed of the RFET in the time domain.

Modelling: In addition to the RC effect and channel transit time of carriers, the RFET has one more parameter affecting its operation speed, and that is the Schottky junction inevitably formed at both ends of the channel. Therefore, carriers travelling through the channel experience a potential barrier near the end region such that only a part of the carriers arrive at their destination, either by overcoming the barrier or by quantum tunnelling; the probability of arrival is less than unity. This type of potential structure results in the confinement of travelling carriers in the channel region and, in turn, delays the formation of a steady-state in terms of carrier density. Therefore, the build-up time for the stabilization of carrier density must be considered for the analysis of the transient response.

A schematic of the 3-gate RFET is shown in Figure 1 where two polarity gates (PG1 and PG2) and control gate (CG) are placed on a channel including thermally grown thin SiO_2 as the gate oxide. Basically, we can apply preliminarily P1 and P2 bias and leave CG off state. Thereby we can operate 3-gate RFET with CG only, which makes the operation speed increase due to the reduced channel effect. Although the 2-gate structure can function as an RFET, we adopted the present structure to determine the pristine characteristics of the RFET under the symmetrical profile of the energy diagram in the channel. The gate configuration of simple 2-gate or multi-gate structure has different pros and cons in comparison with 3-gate structure. For instance, 2-gate structure is simple while multi-gate has flexibility in biasing the gates. Nonetheless, the switching speed of all the structures is greatly affected by carriers occupying the channel. So, we chose a 3-gate structure in which the symmetric configuration of energy barrier is suitable for explainable analysis. Both source and drain metal can be made of silicides such as $TiSi_2$ and $NiSi_2$, and located at the metallurgical interface with an intrinsic silicon channel, playing the role of a Schottky junction and interconnection.

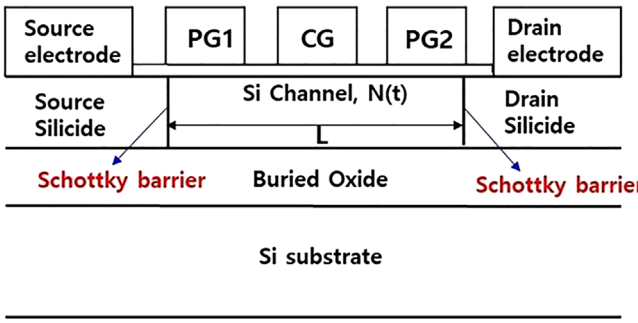

Fig. 1 *Cross-sectional schematic of the analyzed reconfigurable field-effect transistor (RFET) consisting of a single control gate (CG), two symmetrical polarity gates (PGs), silicide both at source and drain sides, and buried oxide on silicon substrate. Total channel length and carrier density of channel are designated as* L *and* N*(t), respectively*

For the nMOS and pMOS operations of the RFET, positive and negative bias voltages are applied to both PGs and CG, respectively. To simplify the analysis, it was assumed that all the gates were electrically synchronized by making them have the same signalling conditions in terms of voltage value and polarity. With these considerations, the carrier density in the channel, $N(t)$ can be regarded as uniformly distributed over the entire channel. Based on the assumption of the synchronized gates, we can wipe out preparation steps such as waiting time for scheduling gate signals extraneous to intrinsic characteristics in this study, such as a feature of carrier transport limited by build-up time.

Given time-varying carrier density $N(t)$ responding to input gate voltage, we can derive the tunnelling current at the junction between the channel and drain and, in turn, determine the transient behaviour of the RFET. From the principle of rate balance, $N(t)$ can be expressed in an analytic form as in the following Equation (1) [7]

$$\frac{dN(t)}{dt} = (\text{carrier influx rate}) - (\text{carrier outflux rate}) = \left(\frac{I_{\text{source}}}{qV}\right) - \left(\frac{N(t)}{\tau} + \frac{I_{\text{drain}}}{qV}\right) \quad (1)$$

where q, V, I_{source}, and I_{drain} denote the elementary charge, channel volume, tunnelling current at source/channel junction and channel/drain junction, respectively. τ denotes the carrier lifetime in the channel representing the natural carrier decay rate. The values of I_{source} and I_{drain} can be obtained from the well-known tunnelling current density at a Schottky junction, $J_{\text{tunnelling}} = qv_R n\theta$ where v_R, n and θ denote the Richardson velocity, carrier density in the tunnelling starting side and tunnelling probability at the Schottky junction, respectively[8]. The Richardson velocity v_R, the average velocity at which electrons of the semiconductor near the Schottky junction approach the barrier, is obtained as in the following Equation (2) [9]

$$v_R = \sqrt{\frac{kT}{2\pi m}} \quad (2)$$

where k, T and m denote the Boltzmann constant, operating temperature and carrier effective mass, respectively.

Using these parameters, the derivative equation of $N(t)$ is expressed with specific parameters as written in the following Equation (3):

$$\frac{dN(t)}{dt} = \frac{v_{R1}N_{\text{silicide}}\theta_1}{L} - \left(\frac{1}{\tau} + \frac{v_{R2}\theta_2}{L}\right)N(t) \quad (3)$$

where L, N_{silicide}, $v_{R1,\,R2}$, and $\theta_{1,2}$ denote total channel length, the carrier density of silicide at the source side, Richardson velocities of silicide in the source region and silicon channel, and tunnelling probability at the source/channel and channel/drain junctions, respectively.

The solution of Equation (3) with an initial condition of $N(0) = 0$ is shown in Equation (4)

$$N(t) = \frac{v_{R1}N_{\text{silicide}}\theta_1/L}{\frac{1}{\tau}+\frac{v_{R2}\theta_2}{L}}\left[1-\exp\left(-\left(\frac{1}{\tau}+\frac{v_{R2}\theta_2}{L}\right)t\right)\right] \quad (4)$$

with which we can describe the temporal change of carrier density in the channel once the tunnelling of the Schottky junction is turned on. The falling of carrier density can be described by put $I_{\text{source}} = 0$ in Equation (1) as expressed in Equation (5):

$$N(t) = N_{\text{initial}}\ \exp\left(-\left(\frac{1}{\tau}+\frac{v_{R2}\theta_2}{L}\right)t\right) \quad (5)$$

where $N_{initial}$ denotes a carrier density at an initial point of falling time interval.

Results: From Equations (4) and (5), we note that a build-up time needs in order to reach a final state after the gate signal is applied, which is neither the RC effect nor the transit time effect. In addition, we observe the rising and falling of $N(t)$ have the same time constant, and thus, symmetric time-varying behaviour. The v_{R2} is a physical quantity of $\sim$2.5x10^4 m/s when the carrier is an electron in silicon. With this value, in Equations (4) and (5), order of magnitude of $1/\tau$ and $v_{R2}\theta_2/L$ are $\sim 10^4$ s^{-1} [10] and $\sim 10^9$ s^{-1}, respectively. The order of latter was derived from assumption of θ_2 as 1% and L as 250 nm. Consequently, we found that the time constants for build-up in a rising and falling are approximately $L/v_{R2}\theta_2$ for usual cases. In addition, this build-up time is proportional to the total channel length and inversely proportional to tunnelling probability at the drain Schottky junction.

To estimate the order of magnitude of the build-up time, we calculated the normalized $N(t)$. The dependence of $N(t)$ on the tunnelling probability at the drain Schottky junction is quantitatively compared in Figure 2a, in which it can be noted that a low tunnelling probability at the drain Schottky junction results in a slow rise of $N(t)$ by nanosecond-level increments. This result implies that the device could operate at a switching speed of gigahertz for a 250 nm long channel device. According to the WKB(Wentzel-Kramers-Brillouin) approximation [11], it is not easy for the tunnelling probability at Schottky junction to reach 10% or more. For instance, the tunnelling probability of a 1 nm wide tunnel barrier in a silicon Schottky junction is approximately 7% and it decreases exponentially as the barrier width increases linearly. Considering that the barrier width of the RFET could hardly be less than a nanometer with a conventional gate signal, the switching operation of the RFET could not be faster than the order of GHz as long as the device is limited by the build-up time.

The tendency of rising time for various channel lengths is shown in Figure 2b, in which the tunnelling probability at the drain Schottky junction is assumed to be 3%. We could expect that the switching speed is also limited to the order of GHz even for the $\sim$100 nm channel length.

The steady-state of $N(t)$ can be obtained from $dN(t)/dt = 0$ in Equation (2) and N_{steady} is shown in Equation (6) as follows:

$$N_{\text{steady}} = \frac{v_{R1}N_{\text{silicide}}\theta_1/L}{\frac{1}{\tau}+\frac{v_{R2}\theta_2}{L}} \cong \frac{N_{\text{silicide}}v_{R1}\theta_1}{v_{R2}\theta_2} \quad (6)$$

Consequently, we can derive the drain current density at a steady state as $J_{\text{drain, steady}} = qN_{\text{silicide}}v_{R1}\theta_1$, which is the same as the source current density. This is self-explanatory because the carrier density in the channel does not change and in turn the source current flows entirely out at the drain without carrier accumulation in the channel when it is in a steady-state.

The time constant for carrier transit of a MOSFET that has no tunnelling process is expressed as L/v_{sat}, where v_{sat} denotes the saturation velocity of 1 $\sim$ 2x10^5 m/s in silicon [12]. In contrast, the RFET shows that the time constant for carrier build-up is $L/v_{R2}\theta_2$, which could be a few hundred times larger than the carrier transit time of the MOSFET,

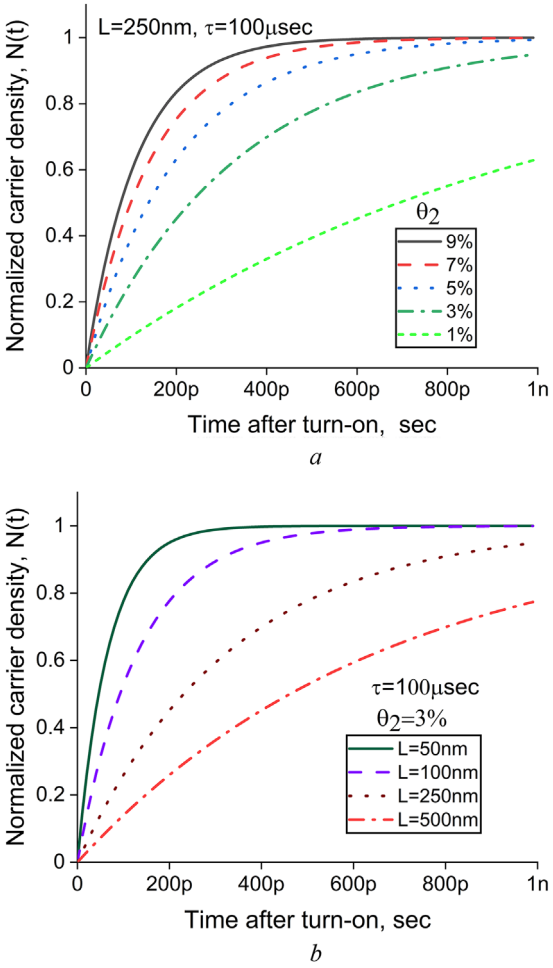

Fig. 2 *Characteristics of carrier rising time with respect to a tunnelling probability at drain Schottky junction b channel length*

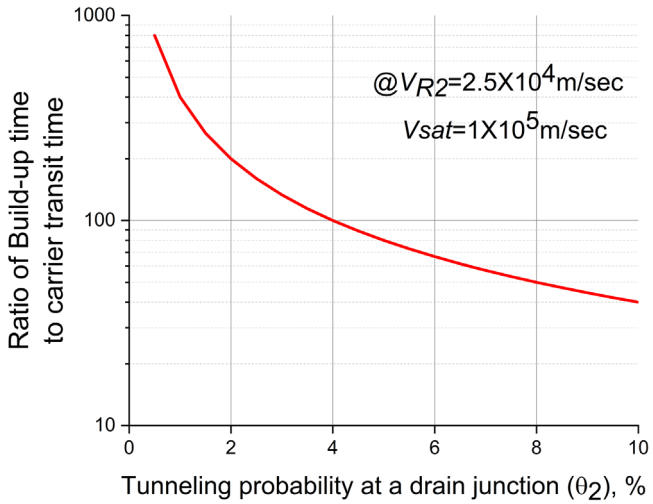

Fig. 3 *Ratio of build-up time to transit time*

resulting from a low tunnelling probability at a normal Schottky junction and a slower velocity of v_{R2} than v_{sat}. As shown in Figure 3, the ratio of build-up time to transit time strongly depends on the tunnelling probability at the drain junction. The tunnelling efficiency could be enhanced using lower bandgap materials such as Ge [13]. A smaller bandgap with a suitable metal silicide means higher tunnelling probability at Schottky junction because of reduced barrier height and width with the same voltage level. Tunnelling efficiency exponentially depends on barrier height and width.

Conclusion: In this study, we quantitatively investigated the temporal behaviour of carrier build-up in the channel of an RFET where both the source and drain sides are confined with a Schottky junction. We found from the analysis of the rate equation for carrier density that carrier build-up strongly depends on both the channel length and tunnelling probability of the drain Schottky junction before reaching a steady state. In comparison with MOSFETs whose performances are mainly limited by the RC effect and transit time across the channel, the operation speed of an RFET could be mainly limited by the carrier build-up time resulting in the restriction of the switching speed of gigahertzs.

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