A 19-GHz low-phase-noise frequency synthesizer for a K-band FMCW radar sensor of detecting micro unmanned aerial vehicles

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A 19-GHz low-phase-noise PLL-frequency synthesizer is presented in this letter that is intended to be used in a K-band FMCW radar which requires strict phase noise for detecting a small unmanned aerial vehicle. The 17.9 to 19.5-GHz PLL includes a Darlington cross-coupled capacitive-degeneration VCO which presents higher maximum attainable oscillation frequency (f_{trans}) and larger negative transconductance (g_m), thus resulting in low phase noise. Manufactured using the SiGe BiCMOS process, the K-band synthesizer demonstrates −114 dBc/Hz at 1 MHz offset and −138 dBc/Hz at 10 MHz offset from 19.456 GHz locking carrier frequency.

Introduction: Military or private sector has used unmanned aerial vehicles (UAVs) for surveillance and spy since the 1950s, and made much effort on implementing smaller radar cross section (RCS) of them which renders it difficult, specifically, for micro UAVs with −20 dBm RCS to be detected [1]. Detection of a puny UAV does necessarily accompany various interferences resulting from multipath effect and clutters surrounding it, which have been resolved by employing linear-distributed micro Doppler features [2]. The FMCW radar has been widely used to measure range as well as to extract velocity from Doppler frequency for hovering or moving targets [3]. The signal-to-noise ratio (SNR) of the FMCW radar system is directly impacted by PLL phase noise which is suppressed to some degree at close range but still required to be minimized at long range [4]. Therefore, phase noise at the out-of- PLL bandwidth must be reduced as low as possible to make sure that a tiny travelling target like drone at long range is captured by radar. This paper presents a low phase-noise 19 GHz PLL synthesizer with −114 dBc/Hz at 1 MHz offset and −138 dBc/Hz at 10 MHz offset which belongs in the beat frequency region corresponding to long range.

FMCW radar transceiver: Illustrated in Figure 1 is a K-band FMCW radar which is composed of a receiver, a transmitter with PLL VCO, an antenna, a circulator and FPGA. In order to achieve a maximum range of 1.5 km, GaAs low-noise amplifier (LNA) and GaN power amplifier (PA) are used off chip in the radar sensor while the transceiver including PLL VCO in the red line is implemented using the SiGe process. A series of saw-tooth chirp signals are transmitted through SiGe drive amplifier (DA) and off-chip PA coming from PLL VCO. Realized by using FPGA, the chirp generator outputs control bits to modulate PLL divide ratio and then cause VCO to produce chirp signals like saw-tooth wave. The K-band FMCW radar does continuously transmit microwave chirp signal whose carrier frequency step-up starts at 18 GHz and wraps up at 19.5 GHz every 250 μs pulse repetition interval (PRI) time. Beat frequency is obtained through the radio frequency (RF) mixer which multiplies transmitted signal and received one from radar target. Corresponding to frequency difference between the transmitted signal and the reflected one from target is the beat frequency from which both range and velocity of the flying object are calculated like (1) [4].

$$f_b = f_r \pm f_d = \frac{2R}{C_o} \cdot \frac{B}{T} \mp f_c \cdot \frac{2v}{C_o} \tag{1}$$

As shown in (1), beat frequency consists of the first term f_r which represents the time of flight of electromagnetic wave travelling with speed of light C_o from the radar to a target at range R and returning to the antenna, and the second term f_d which means the Doppler frequency caused by the moving object like drone flying back and forward from the radar. Note that f_d is positive when the target approaches the radar and negative for the opposite case. In (1), T represents PRI time, B frequency bandwidth, and f_c middle carrier frequency of chirp signal and v target velocity. The range-velocity ambiguity becomes resolved by making multiple measurements. Therefore, about 154 of saw-tooth wave bins are sampled and processed in the FPGA board including analog-to-digital converter (ADC). In homodyne FMCW radar where a time-delayed transmitted chirp signal is mixed with the received one, the phase noises coming from a primary radar system are correlated and partially cancelled out due to range correlation effects [4, 5]. However, it is desirable to minimize phase noise in order to make sure that a successful detection for a drone having small RCS of less than −20 dBm be achieved. As expressed in (2) and (3), phase noise of PLL has a direct impact on SNR of FMCW radar system and thus, on target range R [5].

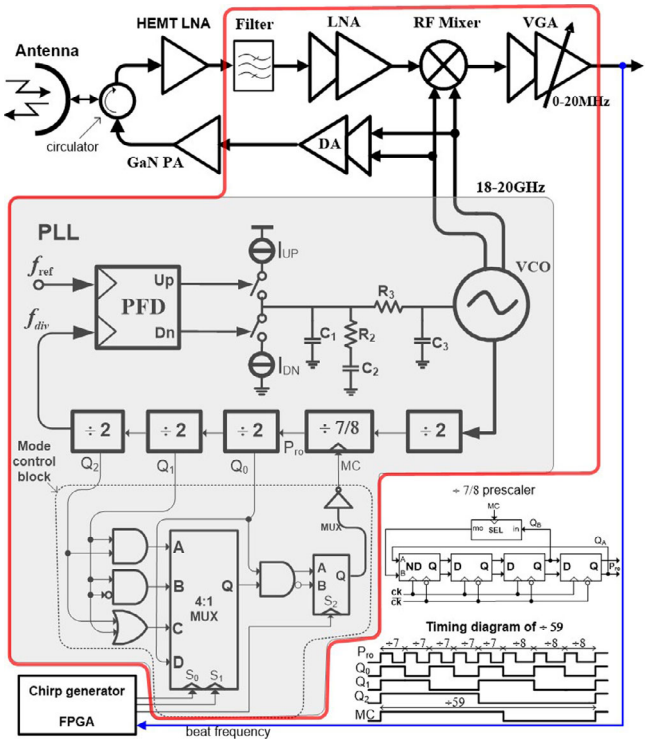

Fig. 1 *K-band FMCW radar transceiver for detecting tiny UAVs. UAV, unmanned aerial vehicle*

$$SNR_{dB} \propto 10log\left(\frac{T_s}{N_{th} + N_{pn} + N_{qn}}\right) \tag{2}$$

In (2), the thermal noise (N_{th}) is expressed by $N_{th} = k \cdot T_n \cdot B_n$ with $k = 1.38 \times 10^{-23}$ Ws/K, $T_n = 290$°K, and B_n = noise bandwidth. The mean noise power (N_{pn}) caused by phase noise is given by $N_{pn} = 2 \cdot (\pi \cdot A \cdot f_{IF} \cdot \sigma_{IF})^2$ with signal amplitude A, IF frequency f_{IF} and IF jitter noise σ_{IF} induced by phase noise. The system quantization noise (N_{qn}) is estimated by $N_{qn} = S_r/(6.02dB \cdot E_b + 1.76dB)$ with received power S_r and ADC effective number of bits E_b.

$$R = \left(\frac{P_t G^2 \lambda^2 \sigma n_p}{(4\pi)^3 L \cdot SNR}\right)^{1/4} \tag{3}$$

Here P_t is transmit power, G antenna gain, λ wavelength, σ RCS, n_p pulse number, L propagation loss. By (2) and (3), the SNR degradation by phase noise does primarily determine the bound for the range uncertainty [5].

PLL: In Figure 1, the PLL is composed of a phase-frequency detector (PFD), a charge pump, an on-chip third-order loop filter, a multimodulus divider, and a VCO. With having divide ratios between 57 and 63, the multimodulus divider consists of ÷2 dividers, ÷ 7/8 dual-modulus prescaler and modulus control block. Figure 1 illustrates the timing diagrams of the divide-by-59 operation where the ÷ 7/8 prescaler divides the differential input clock (CK) by 7 for the first five P_{ro} cycles and by

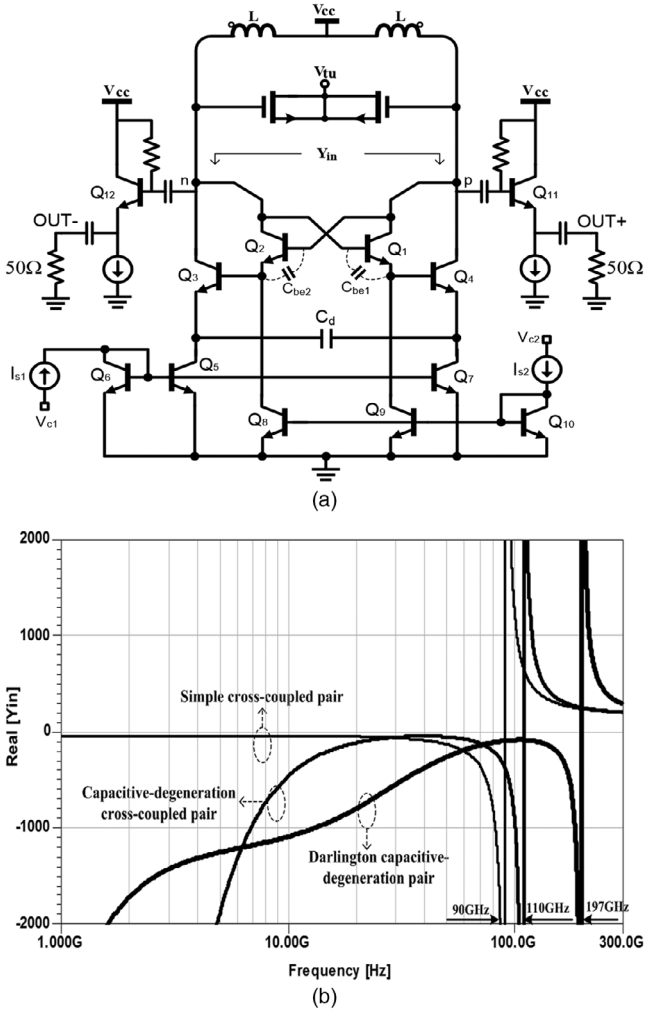

Fig. 2 *(a) Darlington pair VCO circuit. (b) Simulated* f_{trans}

8 for the remaining three P_{ro} ones. The ÷ 7/8 dual-modulus prescaler is configured with an NOR D-F/F (ND), three D-F/Fs, and an SEL. All D-F/Fs are implemented using current-steering emitter-coupled logic (ECL). The ÷7 is accomplished by the NOR operation of Q_A and Q_B with MC = 1 while the ÷8 achieved by signaling logic 'Low' to the B input of the NOR D-F/F with MC = 0. The SEL outputs the inverted Q_B or logic 'Low' signal, depending upon the MC value.

Low-phase-noise VCO: Since PLL phase noise affects SNR of FMCW radar system, it is very important to choose a suitable oscillator topology in order to accomplish as low phase noise as possible. Oscillator having higher maximum attainable oscillation frequency (f_{trans}) is preferred to be employed as the FMCW chirp generator in a higher frequency region above 10 GHz because phase noise is reduced in proportion to oscillator output power which can be much more increased for oscillator transistor having much larger f_{trans} [6]. With consuming the same power, the Darlington-pair transistor is reported to represent higher cut-off frequency (f_T) and larger g_m than single transistor [7, 8]. Figure 2 displays the proposed K-band VCO which is configured with Darlington cross-coupled pair with capacitive degeneration, varactor diode, and a symmetric spiral inductor. The positive feedback, which is formed by the path of Q_4 base → Q_4 collector (p) → C_{be2} → Q_3 base → Q_3 collector (n) → C_{be1} → Q_4 base, produces additional negative resistance and pushes its f_{trans} upwards into the higher operating frequency region. Each f_{trans} of both the simple capacitive-degeneration pair and the Darlington capacitive-degeneration cross-coupled pair are expressed as (4) and (5), respectively [9].

$$f_{trans\_cdcc} = f_{TS}\sqrt{\frac{r_e + \frac{1}{g_m} + \frac{1}{\omega_T C_d}}{r_b + r_e}} \tag{4}$$

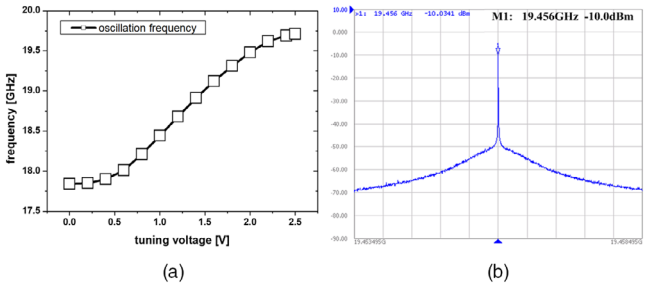

Fig. 3 *(a) VCO frequency tuning range. (b) Locked output spectrum*

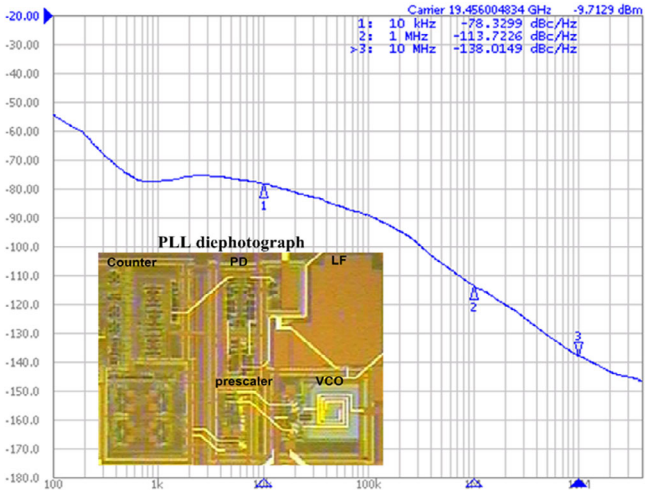

Fig. 4 *Measured phase noise and die photograph of the K-band PLL*

$$f_{trans\_dar} = f_{TD}\sqrt{\frac{r_e + \frac{1}{g_m} + \frac{1}{\omega_T C_d} + \frac{1}{\omega_T C_{be}}}{r_b + r_e}} \tag{5}$$

Here C_{be} is base-emitter capacitance, r_b base resistance, r_e emitter resistance, g_m transconductance. f_{TS} shows the cutoff frequency of a transistor while f_{TD} expresses that of the Darlington pair.

Comparing f_{trans_dar} with f_{trans_cdcc} manifests that the Darlington capacitive-degeneration pair accomplishes much higher f_{trans} than the simple capacitive-degeneration pair because the cutoff frequency of Darlington pair is larger than that of a single transistor [7]. Simulated in Figure 2b is each real part of input admittances of cross-coupled pair, capacitive-degeneration pair and Darlington capacitive-degeneration pair. The f_{trans_dar} of Darlington capacitive-degeneration pair is demonstrated to be highest among the three oscillators as 197 GHz which is very close to f_{max} of 220 GHz for npn bipolar transistor [10].

Measurement: Manufactured using 0.25 μm SiGe:C BiCMOS process technology as displayed in Figure 3, the K-band PLL frequency synthesizer achieves a locking output frequency of 17.9 to 19.5 GHz and −10 dBm output power. As shown in Figure 4, the PLL phase noise is measured as −113.7 dBc at 1 MHz and −138 dBc/Hz at 10 MHz offset, respectively, from 19.456 GHz when the 152 MHz clock is input to PFD. Included in the phase noise curve of Figure 4 is the PLL die photograph whose size is 0.8 × 0.6 mm^2. Compared to the state-of-the-art K- and Ka-band PLLs in Table 1, the frequency synthesizer obtains lowest phase noises at 1 and 10 MHz offset, respectively, while consuming 175-mW power.

Conclusion: This paper presents a low phase-noise frequency synthesizer of accomplishing −138 dBc/Hz at 10 MHz offset based on Darlington capacitive-degeneration VCO, which enables improving SNR and probability of detection of FMCW radar for a long-range target.

Author contributions: **Jayol Lee**: Conceptualization; data curation; formal analysis; investigation; methodology; resources; software;

Table 1. Comparison to the state-of-the-art PLLs using the SiGe process

	This PLL	[11]	[12]	[13]	[14]
f_o [GHz]	17.9 ∼19.5	16.0 ∼18.8	25.3 ∼28.0	15.6 ∼17.1	37.2 ∼40.0
Phase noise [dBc/Hz]	−114[a] −138[b]	−102[a] −126[b]	−107[a] −134[b]	−108[a] −134[b]	−101[a] −125[b]
Power [mW]	175	144	850	188	380

[a] 1 MHz offset.
[b] 10 MHz offset.

supervision; validation; visualization; writing—original draft; writing—review and editing. **Kyung Hwan Park and Bon Tae Koo**: Supervision; funding acquisition; project administration.

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